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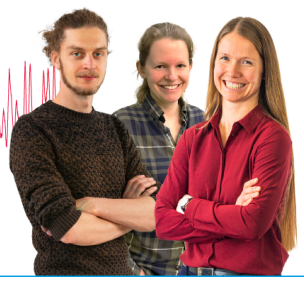

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ABSTRACT

Tellurium (Te) has recently emerged as a promising *p*-type semiconductor that can be processed at low temperatures, compatible with back end of line CMOS integration. Characterization of tellurium–dielectric interfaces is essential for further device advancements. Here, the interface quality of Te with ZrO_2 gate dielectric is studied in a metal-oxide semiconductor capacitor structure. The interface trap density (D_{it}) is measured as a function of atomic layer deposition (ALD) temperature, without the use of a seed layer. Given the low thermal budget of Te, the ALD temperature is shown to be particularly important. The lowest D_{it} of 5×10^{12} states/cm^2 eV is obtained at a low ALD process temperature of 120 °C. To further assess the impact of D_{it} on device performance, field-effect transistors (FETs) were fabricated. The subthreshold swing and effective hole mobility of the FETs were analyzed in relation to D_{it}, emphasizing the importance of a defect-minimized interface for enhancing Te transistor performance.

Tellurium (Te) is a *p*-type semiconductor that has emerged as a promising candidate for next-generation semiconductor devices due to its unique properties, including high hole mobility and a thickness-dependent bandgap, which ranges from 0.31 eV in bulk to 1.04 eV in the monolayer.[1–3] Notably, evaporated Te can be deposited over large areas at low temperatures, making it an attractive material for optoelectronics and flexible electronics as well as circuit integration.[4–8] Despite recent advancements, research on the Te/gate dielectric interface remains limited. Moreover, the high vapor pressure of Te above 250 °C constrains studies on its interface with gate dielectrics that require high processing temperatures, such as thermally oxidized SiO_2.[9,10]

As transistor channel lengths are scaled down, the oxide thickness must also be reduced to meet voltage requirements. However, this results in high levels of leakage currents in ultra-thin oxide layers. One approach to mitigate this issue is to use high-κ dielectrics, which maintain the same gate electrostatics with a thicker dielectric film.[11–13] ZrO_2 is a widely studied high-κ dielectric with low leakage current and suitability for deposition at low temperatures.[11,14,15] In this study, we focus on characterizing the interface between evaporated Te and atomic layer deposition (ALD)-grown ZrO_2 as a function of ALD temperature, without the use of a seed layer. Te-based capacitors with ZrO_2 gate dielectric were fabricated. Capacitance–voltage ($C–V_G$) and conductance-frequency (G/ω-f) measurements were performed to extract the interface trap density (D_{it}). D_{it} is found to increase at higher ALD temperature, with the lowest extracted value of 5×10^{12} states/cm^2·eV observed at 120 °C. Additionally, Te–ZrO_2 based field-effect transistors (FETs) were fabricated at various ALD temperatures and characterized using current–voltage ($I–V_G$) measurements to assess device properties corresponding to each D_{it} level.

A quartz substrate was used for fabrication of metal-oxide-semiconductor (MOS) capacitors to minimize parasitic capacitance. Figure 1(a) shows the schematic of a Te MOS capacitor with a bottom electrode contact and a top-gate with ZrO_2 as the gate dielectric. The fabrication process involves defining the bottom electrode area using standard photolithography at the first step, followed by deposition of 30 nm thick rhodium (Rh) via e-beam evaporation as the metal contact. The Te region was then patterned using photolithography to cover both the bottom electrode and the quartz surface. An 8 nm thick amorphous Te layer was thermally evaporated at −80 °C to achieve a uniform film.[16] Te undergoes an amorphous to crystalline phase transition near ambient conditions due to the low activation energy. A low

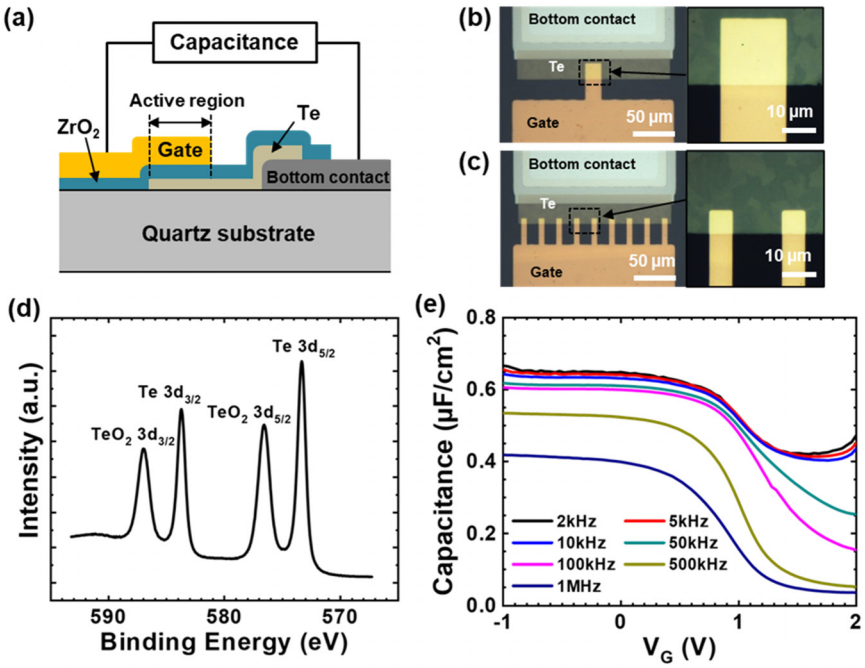

FIG. 1. (a) Cross-sectional schematic of the device structure and measurement setup used for C–V and G/ω-frequency measurements. (b) and (c) Optical microscope images of SB and MB capacitors, respectively. (d) XPS measurement results of an 8 nm Te layer on a Si substrate. (e) C–V characteristics at room temperature for an SB Te capacitor with an ALD temperature of 120 °C. The AC amplitude is 25 mV.

substrate temperature during crystallization limits the nucleation site formation and reduces grain boundaries. The substrate temperature was maintained below 5 °C during crystallization, to achieve crystalline Te with grain sizes exceeding several micrometers.[5] Afterward, the Te was lifted off, and a 10 nm thick ZrO_2 layer was deposited across the entire surface using ALD at temperatures of 120, 150, and 180 °C. Te spontaneously oxidizes upon exposure to air, forming a native oxide layer with a thickness of up to approximately 0.4 nm.[17] For the remainder of this study, we refer to the resulting Te–TeO_2–ZrO_2 interface as the Te–ZrO_2 stack. Next, the gate electrode was patterned on the Te–ZrO_2 stack, followed by the deposition of a 2 nm Ti/30 nm Au gate electrode via e-beam evaporation and subsequent liftoff. To ensure reliable probing, the ZrO_2 layer over the contact pad region was etched using a buffered oxide etchant. Finally, single-bridge (SB) and multi-bridge (MB) capacitors were fabricated to examine the impact of grain boundaries on interface trap density, with the MB structure divided into nine separate identical regions, as shown in Figs. 1(b) and 1(c). The total active areas of the SB and MB capacitors were 383 and 435 μm^2, respectively. The MB design minimized the influence of grain boundaries at the Te–ZrO_2 interface by segmenting the active area into smaller regions, with each bridge area smaller than an individual grain. C–V measurements were then performed, as shown in Fig. 1(a).

To promote ALD of ZrO_2 on the Te surface, a thin Te oxide layer is necessary to provide TeO_2–OH^* sites for the adsorption of Zr ALD precursors.[14,18] X-ray photoelectron spectroscopy (XPS) measurements on a representative 8 nm thick Te film confirmed the presence of TeO_2, as shown in Fig. 1(d). Figure 1(e) presents the frequency-dependent C–V_G characteristics at ambient temperature for the SB capacitor with a ZrO_2 gate dielectric deposited at an ALD temperature of 120 °C. TeO_2 is a p-type semiconductor with high hole mobility.[19,20] Therefore, any interface trap is likely to form at the interface between Te–TeO_2 and ZrO_2. To account for the influence of the thin interfacial oxide, the gate capacitance was extracted from the C–V_G characteristics at $V_G = -1.0$ V, yielding a value of 0.67 μF/cm^2. In the full depletion region ($V_G > 1.5$ V), frequency-dependent capacitance dispersion was observed, which is attributed to the reduced response of minority carriers (electrons) at high frequencies, consistent with the typical behavior of conventional *p*-type metal-oxide-semiconductor (MOS) capacitors in CMOS technology. However, at frequencies above 500 kHz, a substantial decrease in capacitance was observed across the entire C–V curve. This behavior is attributed to the presence of deep trap states at the Te–ZrO_2 interface, which hinder the ability of charges to respond to high-frequency signals.[21–25] As shown in Fig. S1, the C–V curves of all capacitors with ZrO_2 ALD temperatures of 120, 150, and 180 °C exhibited similar trends in frequency dispersion and a significant reduction in capacitance at high frequencies.

The conductance method was used to extract G/ω-f and calculate D_{it},[26–28] as shown in Figs. 2(a)–2(c). The measured conductance (G_m) was derived from the measured dissipation factor (D_m) and measured capacitance (C_m) as $G_m = D_m \omega C_m$.[29] The corrected capacitance (C_c) and corrected conductance (G_c) were obtained from the measured capacitance (C_{ma}) and conductance (G_{ma}) in the accumulation region. These values were then used to determine the sheet resistance (R_s) as follows:

$$R_s = G_{ma}/\left(G_{ma}^2 + \omega^2 C_{ma}^2\right). \quad (1)$$

Based on R_s, the series resistance factor (a) was calculated as $a = G_m - (G_m{}^2 + \omega^2 C_m{}^2)\, R_s$. Subsequently, the corrected capacitance and corrected conductance were determined using the following equations:

$$G_c = \left[\left(G_m^2 + \omega^2 C_m^2\right) a\right]/\left(a^2 + \omega^2 C_m^2\right), \quad (2)$$

$$C_c = \left[\left(G_m^2 + \omega^2 C_m^2\right) C_m\right]/\left(a^2 + \omega^2 C_m^2\right). \quad (3)$$

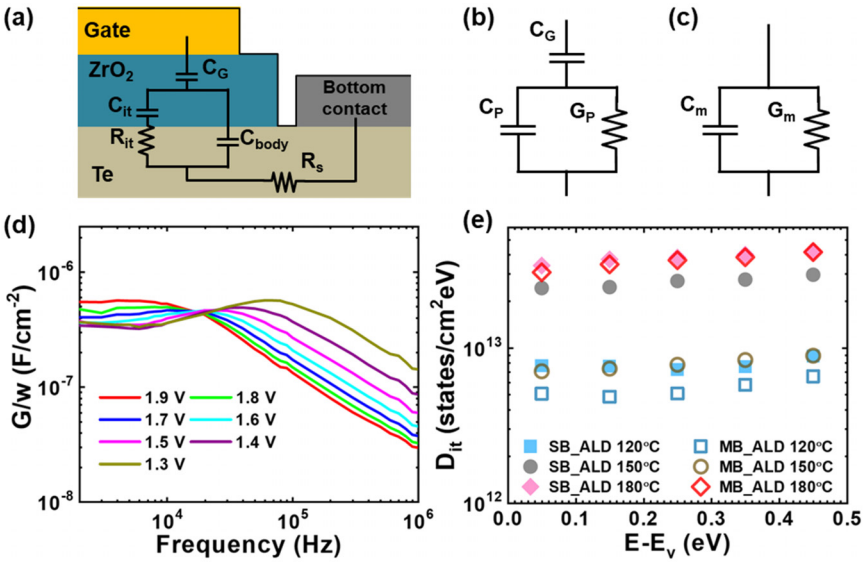

FIG. 2. (a) Equivalent circuit of a Te capacitor. (b) Simplified circuit layout of (a). (c) Equivalent circuit measured using the experimental setup, where C_{it} and R_{it} represent the interface trap capacitance and resistance, respectively, and C_p denotes the equivalent parallel substrate capacitance. (d) G/ω vs frequency for the SB capacitor with an ALD temperature of 120 °C. (e) D_{it} vs $E - E_V$, calculated from the peak of G/ω vs frequency.

Finally, the equivalent parallel conductance (G_p/ω) and D_{it} were expressed as

$$G_p/\omega = \omega G_c C_G^2/[G_c^2 + \omega^2(C_G - C_c)^2], \quad (4)$$

$$D_{it} = (2.5/q)\,(G_p/\omega), \quad (5)$$

where G_p represents the equivalent parallel conductance. Based on these equations, the G_p/ω–f of the SB capacitor with a ZrO_2 dielectric deposited at an ALD temperature of 120 °C was plotted as a function of V_G, ranging from 1.9 to 1.3 V, as shown in Fig. 2(d). The G_p/ω–f plots in the full depletion region for all capacitors at various ZrO_2 ALD temperatures are presented in Fig. S2. Subsequently, D_{it} was extracted using the maximum peak values in the G_p/ω–f curves. Figure 2(e) presents the D_{it} values for SB and MB capacitors with ZrO_2 gate dielectric deposited at ALD temperatures of 120, 150, and 180 °C. Considering that 8 nm-thick Te has a bandgap of approximately 0.5 eV,[6] the lowest D_{it} value observed in our measurements was 5×10^{12} states/cm^2·eV at the midgap for the MB capacitor with ZrO_2 deposited at 120 °C, while D_{it} increased at higher ALD temperatures. Under identical ALD conditions, SB capacitors consistently exhibited a higher D_{it} than MB capacitors. Notably, D_{it} of the MB capacitor with ZrO_2 deposited at 150 °C was reduced by approximately 71% compared to that of the SB capacitor at the same ALD temperature. This D_{it} reduction in MB capacitors is attributed to the mitigation of Te grain boundary effects at the Te–ZrO_2 interface, achieved by segmenting the active capacitor area. However, both SB and MB capacitors fabricated at an ALD temperature of 180 °C exhibited a significant degradation in interface quality, with D_{it} exceeding 3.6×10^{13} states/cm^2·eV.

To investigate the variation in D_{it} with ZrO_2 ALD temperature, the Te regions of the capacitors were examined using optical microscopy. The Te grain size showed no significant difference compared to the as-deposited films after the ZrO_2 deposition at a process temperature of 120 and 150 °C, as shown in Figs. 3(a)–3(c). However, Fig. 3(d) indicates recrystallized Te after ALD deposition at 180 °C, resulting in a substantial increase in grain boundaries, which led to the observed degradation in D_{it}. This trend is further supported by atomic force microscopy (AFM), which shows a gradual increase in mean surface roughness (R_q) with higher deposition temperatures. Raman spectroscopy of the Te regions revealed no significant shift in the vibrational mode peaks, but a reduction in the integrated intensity counts of the E_2 mode and broadening of its full width at half maximum (FWHM) were observed at elevated temperatures (see the supplementary material). The stable surface morphology of Te between 120 and 150 °C ALD temperatures, alongside a significant increase in D_{it} of the SB capacitor, confirms that higher ALD temperatures promote deep trap site formation at the Te–ZrO_2 interface. The notable reduction in D_{it} from SB to MB capacitors at 150 °C further indicates that these trap sites are particularly concentrated at Te grain boundaries. Additionally, in the MB capacitor, as the ZrO_2 ALD temperature increased from 120 to 150 °C, D_{it} increased by approximately 2.7×10^{12} states/cm^2·eV. This increase is attributed to the formation of additional interface trap sites due to the higher ALD temperature, even after minimizing the influence of grain boundaries.

To assess the impact of D_{it} on FET performance, we fabricated FETs using the same process as the capacitors, as shown in Fig. 4(a). The devices feature a metal (Rh) contact-first scheme for the source and drain, an 8 nm-thick Te channel, a 10 nm-thick ALD ZrO_2 gate dielectric, and Ti/Au gate electrodes. Figure 4(b) shows the fabricated FET with a Te channel width and length of 12 μm each. Figure 4(c) presents the I_{DS}–V_G characteristics at $V_{DS} = -0.1$ V for the fabricated FETs. Devices with ZrO_2 gate oxide deposited at ALD temperatures of 120, 150, and 180 °C exhibited subthreshold swings (SSs) of 264, 294, and 298 mV/dec, respectively, as illustrated by the steepest slope in Fig. 4(c). The corresponding maximum effective hole mobilities vs V_G were extracted to be 59, 33, and 27 cm^2 V^{-1} s^{-1}, respectively, as shown in Fig. 4(d). These results clearly demonstrate a direct correlation between D_{it} and device performance. However, the fabrication process in this study primarily focused on achieving a clean Te–ZrO_2 interface, and the Te/source-drain contact scheme was not optimized. Consequently, the SS increased by approximately ~160 mV/dec compared to previous

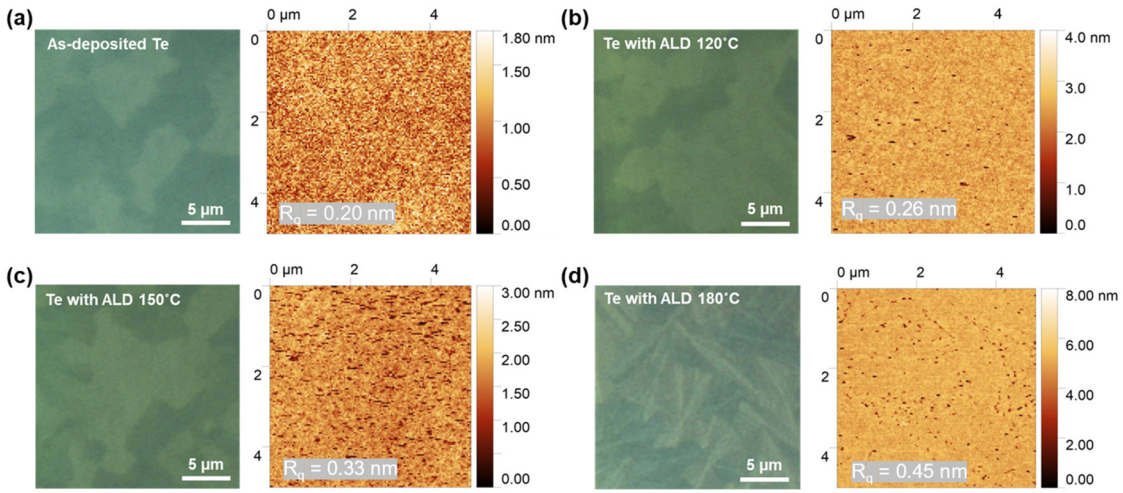

FIG. 3. (a) Optical image and AFM morphology scan of the as-deposited Te after crystallization in the capacitor. (b)–(d) Optical images and AFM scans of the Te region in capacitors with ZrO_2 ALD temperatures of 120, 150, and 180 °C, respectively.

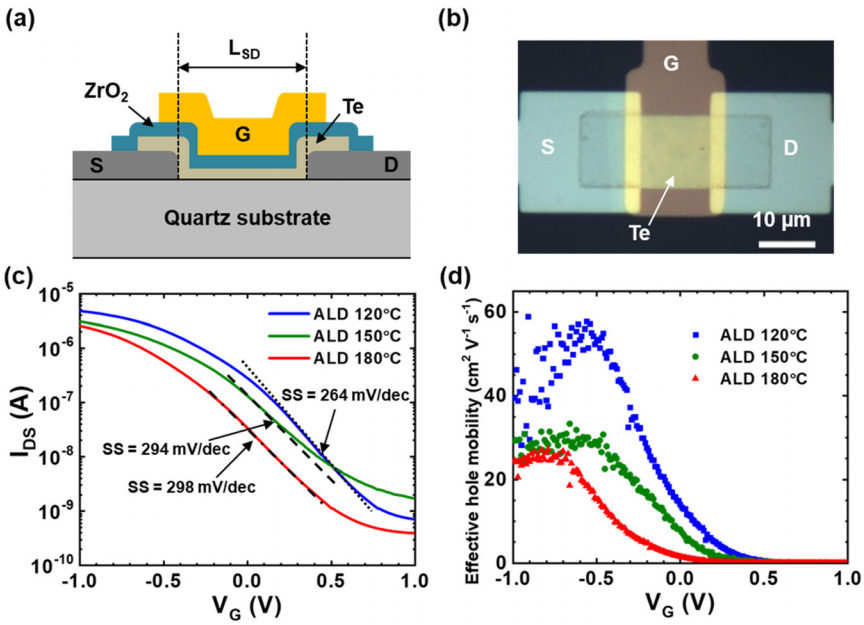

FIG. 4. (a) Cross-sectional schematic of the Te FET device structure and the measurement setup used for I–V measurements. (b) An optical microscope image of the FET with ZrO_2 gate oxide deposited at an ALD temperature of 120 °C. (c) I_{DS}–V_G characteristics of Te FETs with channel dimensions of 12 μm × 12 μm at ZrO_2 deposition temperatures of 120, 150, and 180 °C. (d) Effective hole mobility of FETs as a function of V_G.

reports.[6] Future improvements in Te-FET performance can be achieved by optimizing the device fabrication process, particularly developing optimal contacts for Te devices.

In conclusion, D_{it} of Te capacitors with ALD-deposited ZrO_2 gate dielectric was extracted from the C–V and G/ω-f characterization as a function of ALD deposition temperature. Te capacitors were fabricated in both SB and MB types, and the lowest D_{it} value, calculated using the conductance method, was found to be 5×10^{12} states/cm^2·eV for the MB capacitor with ZrO_2 deposited at 120 °C, where the influence of Te grain boundaries was minimized. As the ZrO_2 ALD deposition temperature increased up to 180 °C, D_{it} showed a notable increase, revealing a rise in grain boundary density due to Te recrystallization. Increase in the ALD temperature led to the generation of deep trap sites at the Te–ZrO_2 interface. Likewise, Te FETs fabricated under the same conditions exhibited degradation in SS and effective hole mobility with increasing ZrO_2 deposition temperature, confirming a strong correlation with D_{it}. This work highlights the importance of defect minimized interface for enhancing scaled Te transistors in future technologies.

See the supplementary material for room temperature C–V characteristics and G/ω vs frequency plots of single and multi-bridged Te capacitors at various ZrO_2 ALD temperatures, and Raman spectra of the Te regions within the capacitors.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Kyeong-Jae Byeon: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **I. K. M. Reaz Rahman:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Inha Kim:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Project administration (equal); Writing – original draft (equal); Writing – review & editing (equal). **Howoo Park:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Ali Javey:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]J. Qiao, Y. Pan, F. Yang, C. Wang, Y. Chai, and W. Ji, Sci. Bull. **63**, 159 (2018).
[2]Z. Shi, R. Cao, K. Khan, A. K. Tareen, X. Liu, W. Liang, Y. Zhang, C. Ma, Z. Guo, X. Luo, and H. Zhang, Nano-Micro Lett. **12**, 99 (2020).
[3]J. Zha, D. Dong, H. Huang, Y. Xia, J. Tong, H. Liu, H. P. Chan, J. C. Ho, C. Zhao, Y. Chai, and C. Tan, Adv. Mater. **36**, 2408969 (2024).
[4]Y. Yang, M. Xu, S. Jia, B. Wang, L. Xu, X. Wang, H. Liu, Y. Liu, Y. Guo, L. Wang, S. Duan, K. Liu, M. Zhu, J. Pei, W. Duan, D. Liu, and H. Li, Nat. Commun. **12**, 6081 (2021).
[5]C. Zhao, H. Batiz, B. Yasar, H. Kim, W. Ji, M. C. Scott, D. C. Chrzan, and A. Javey, Adv. Mater. **33**, 2100860 (2021).
[6]C. Zhao, C. Tan, D.-H. Lien, X. Song, M. Amani, M. Hettick, H. Y. Y. Nyein, Z. Yuan, L. Li, M. C. Scott, and A. Javey, Nat. Nanotechnol. **15**, 53 (2020).
[7]J. Zha, J. Tong, H. Huang, Y. Xia, D. Dong, and C. Tan, Appl. Phys. Lett. **125**, 070504 (2024).
[8]L. Li, G. Zhang, M. Younis, T. Luo, L. Yang, W. Jin, H. Wu, B. Xiao, W. Zhang, and H. Chang, ACS Appl. Electron. Mater. **6**, 2161 (2024).
[9]C. Zhao, L. Hurtado, and A. Javey, Appl. Phys. Lett. **117**, 192104 (2020).
[10]R. Dutton and R. Muller, Thin Solid Films **11**, 229 (1972).
[11]Y.-C. Byun, J.-G. Lee, X. Meng, J. S. Lee, A. T. Lucero, S. J. Kim, C. D. Young, M. J. Kim, and J. Kim, Appl. Phys. Lett. **111**, 082905 (2017).
[12]M. Reinke, Y. Kuzminykh, and P. Hoffmann, Chem. Mater. **27**, 1604 (2015).
[13]M. Leskelä and M. Ritala, Thin Solid Films **409**, 138 (2002).
[14]D. M. Hausmann, E. Kim, J. Becker, and R. G. Gordon, Chem. Mater. **14**, 4350 (2002).
[15]N. Huby, S. Ferrari, E. Guziewicz, M. Godlewski, and V. Osinniy, Appl. Phys. Lett. **92**, 023502 (2008).
[16]K. Okuyama and Y. Kumagai, J. Appl. Phys. **46**, 1473 (1975).
[17]C. M. Smyth, G. Zhou, A. T. Barton, R. M. Wallace, and C. L. Hinkle, Adv. Mater. Interfaces **8**, 2002050 (2021).
[18]X. Wang, S. K. Ghosh, M. Afshar-Mohajer, H. Zhou, Y. Liu, X. Han, J. Cai, M. Zou, and X. Meng, J. Mater. Res. **35**, 804 (2020).
[19]A. Zavabeti, P. Aukarasereenont, H. Tuohey, N. Syed, A. Jannat, A. Elbourne, K. A. Messalea, B. Y. Zhang, B. J. Murdoch, J. G. Partridge, and M. Wurdack, Nat. Electron. **4**, 277 (2021).
[20]A. Liu, Y. S. Kim, M. G. Kim, Y. Reo, T. Zou, T. Choi, S. Bai, H. Zhu, and Y. Y. Noh, Nature **629**, 798 (2024).
[21]S. Hlali, N. Hizem, and A. Kalboussi, J. Comput. Electron. **15**, 1340 (2016).
[22]I. Hussain, M. Y. Soomro, N. Bano, O. Nur, and M. Willander, J. Appl. Phys. **112**, 064506 (2012).
[23]R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S. H. Kim, T. Hoshii, T. Yasuda, W. Jevasuwan, T. Maeda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, Appl. Phys. Lett. **100**, 132906 (2012).
[24]S. M. Pazos, F. L. Aguirre, K. Tang, P. McIntyre, and F. Palumbo, J. Appl. Phys. **124**, 224102 (2018).
[25]V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, E. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, IEEE Trans. Electron Devices **59**, 1084 (2012).
[26]K. Takei, R. Kapadia, H. Fang, E. Plis, S. Krishna, and A. Javey, Appl. Phys. Lett. **102**, 153513 (2013).
[27]E. H. Nicollian and A. Goetzberger, Appl. Phys. Lett. **10**, 60 (1967).
[28]K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, IEEE Trans. Electron Devices **55**, 547 (2008).
[29]T. Balasubramaniam, S. K. Narayandass, and D. Mangalaraj, Bull. Mater. Sci. **20**, 79 (1997).