NANOTUBE ELECTRONICS

# High-performance transistors

Future computers will require nanoscale transistors with high-dielectric-constant gate oxides. Carbon nanotube transistors integrated with $ZrO_2$ gate oxides emerge as very promising candidates.

RICHARD MARTEL is at the IBM T. J. Watson Research Center, Yorktown Heights, New York 10598, USA.
e-mail: martelr@us.ibm.com

There are potentially many ways to make computers faster, more economical, and even smarter. As far as silicon is concerned, this is usually achieved by scaling down the relevant dimensions of the metal oxide semiconductor field-effect transistor (MOSFET)[1]. This means scaling down not only the channel length, but all other dimensions, including the thickness of the $SiO_2$ gate oxide (currently less than 2 nm in advanced integrated circuits). Although concerted efforts to push the ultimate scaling limit of MOSFETs are underway, the miniaturization is inevitably going to stall within a decade or so. How small silicon MOSFETs can be made is a matter of continuing debate, and is stimulating exploration of potential alternatives to silicon technology.

The paper by Ali Javey and colleagues[2] published in this issue of *Nature Materials* brings an interesting new twist to this debate with the introduction of vertically scaled carbon nanotube FETs. Javey and colleagues fabricated prototype FETs based on single semiconducting nanotubes using a novel geometry, and integrated them with a $ZrO_2$ gate oxide (Fig. 1a,b). Because $ZrO_2$ has a much higher dielectric constant ($\kappa$) than $SiO_2$, the gate-to-channel capacitance is higher, which enables better switching of the FETs. The performance of the nanotube FETs (normalized by the width of the nanotube) exceeds those of state-of-the-art silicon MOSFETs. These results provide strong evidence that carbon nanotubes offer great potential for use in logic circuits.

Since their discovery by Sumio Iijima[3] in 1991, carbon nanotubes have attracted much interest for future electronic applications. There are three main reasons for this. First, individual carbon nanotubes have the ability to carry electrical current at significantly higher densities than most metals and semiconductors[4]. This property indicates that carriers in nanotubes undergo very little scattering, even at room temperature. This leads to significant advantages in electronic applications, because the charge carriers travel the length of the tubes with high mobility[5].

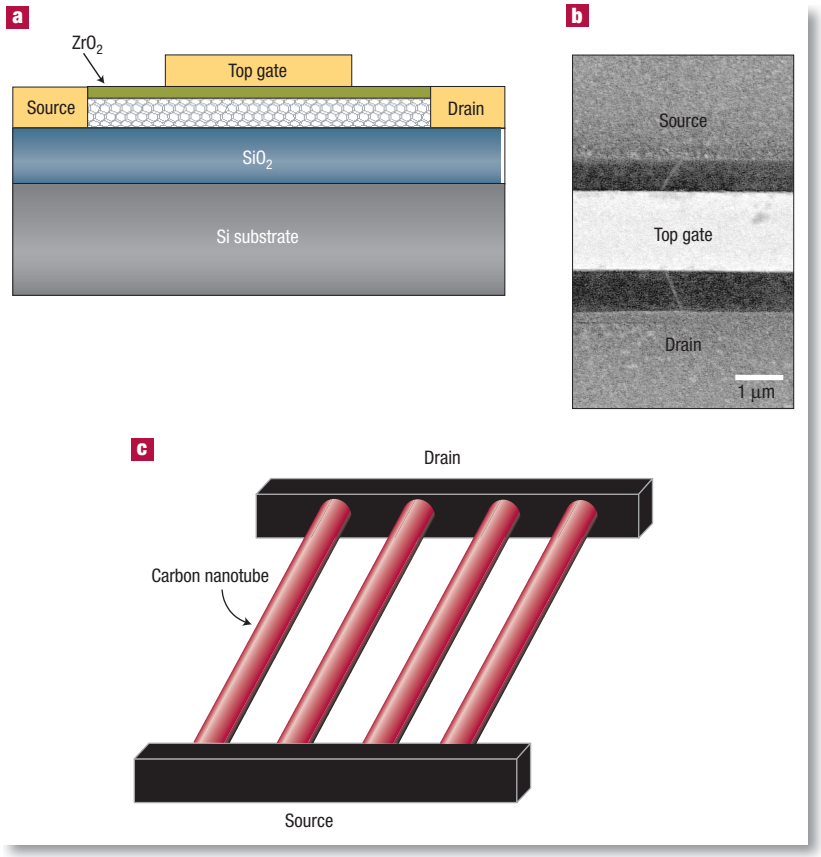


**Figure 1** High-performance carbon nanotube field-effect transistors. **a**, Geometry of a typical nanotube transistor built by Ali Javey and co-workers[2]. **b**, Scanning electron micrographof the same device. The transistors integrate a new local top-gate structure with a thin $ZrO_2$ oxide layer. **c**, The comparison of the transistor performance with a silicon MOSFET involves the theoretical construction of a compact array, in which the nanotubes are laid out with a spacing of at least the diameter of a single nanotube.

Second, carbon nanotubes are inert and present no surface states: all the carbon bonds are satisfied and no dangling bonds are present at the surface of the tube. This feature makes them more compatible with other materials such as oxides, and significantly reduces the

need to passivate the oxide–semiconductor interface, as is required for silicon. Finally, nanotubes can be grown at specific locations[6,7], or simply dispersed from solution[8,9]. Moreover, they can potentially be handled and separated in solution with modern chemical techniques[10,11].

These properties give nanotubes some significant advantages over other molecular conductors, but nanotubes also present some difficulties. Most importantly, synthesis products always consist of a mixture of metallic and semiconducting nanotubes. For electronic applications, it will be essential that these can be separated. This is not yet possible, though a partial solution has already been proposed[12]. Another important challenge is the assembly of nanotubes at specific locations and orientations in well-ordered arrays. This poses problems particular to nanotubes, because the assembly can easily be disrupted because of the strong intermolecular interactions. Much work is presently being pursued in these directions, and progress in nanotube synthesis, assembly, characterization and separation has so far been rapid.

A number of prototype nanotube devices have already been made and evaluated. Earlier this year, a team at IBM demonstrated that several elements could be integrated to fabricate carbon nanotube FETs that closely resemble conventional semiconductor transistors[13]. The work by Javey and co-workers improves on this in two significant ways. First, they use a new high-$\kappa$ dielectric material — $ZrO_2$ — as the gate oxide, permitting a thickness of about 8 nm. In addition, they constructed the device using a local top-gate (Fig. 1a,b), rather than a top-gate covering the full length of the nanotube between source and drain electrodes. This local top-gate effectively prevents leakage between the gate and the contact electrodes. The end result is an impressive FET structure that allows very significant electric fields to be generated at the nanotube interface on application of a low voltage on the gate electrode. These devices work in a depletion mode: the gate locally depletes the carriers in the nanotube and turns OFF the devices with an efficiency that approaches the theoretical limit for room-temperature operation.

Further improvements in the ON state of these nanotube transistors are possible, and the performance limit is yet to be reached. But the level of performance certainly justifies comparison with silicon MOSFETs. Unfortunately, the FET characteristics cannot be compared directly, because the nanotube transistor geometry is radically different (cylindrical as opposed to planar). As pointed out by Javey and co-workers, a simple normalization with the tube diameter cannot adequately account for the different electrostatic effects. This means that some assumptions are required.

To the first order, the comparison implies that a circuit topology similar to today's silicon-based circuit technology will be used — that is, the nanotube FETs are switches that form logic gates interconnected by wires. A FET made of only one nanotube cannot fulfill this task because it cannot deliver enough current. Thus, an array of nanotubes is theoretically constructed by assembling them with equal spacing of at least the nanotube diameter (Fig. 1c). The comparison is then made possible when taken on a per unit device-width basis, which includes the nanotube diameter and the unavoidable gaps between nanotubes in the array. Here, we have to be careful as the prototype device gives results from an individual nanotube, rather than an array. Nevertheless, the comparison is reasonable, and the assumptions can be tested later by constructing nanotube FETs from arrays of carbon nanotubes. Many other considerations arise, but this test should probably be pursued with greatest urgency.

We do not yet know whether future computers will take advantage of the unique properties of carbon nanotubes. The next steps towards this goal will be increasingly more difficult, but this work points in a very promising direction for nanotube transistors.

## References


1. *International Technology Roadmap for Semiconductors* Semiconductor Industry Association, 2001. http://public.itrs.net.
2. Javey, A. *et al. Nature Mater.* **1**, 241–246 (2002).
3. Iijima, S. *Nature* **354,** 56–58 (1991).
4. Frank, S., Poncharal, P., Wang, Z. L. & DeHeer, W. A. *Science* **280,** 1744–1746 (1998).
5. Fuhrer, M. S., Kim, B. M., Dürkop, T. & Brintlinger, T. *Nano Lett.* **2,** 755–759 (2002).
6. Fan, S. *et al. Science* **283,** 512–514 (1999).
7. Wei, B. Q. *et al. Nature* **416,** 495–496 (2002).
8. Bockrath, M. *et al. Science* **275,** 1922–1925 (1997).
9. Tans, S. J. *et al. Nature* **386,** 474–477 (1997).
10. Chen, J. *et al. Science* **282,** 95–98 (1998).
11. Chattopadhyay, D., Lastella, S., Kim, S. & Papadimitrakopoulos, F. *J. Am. Chem. Soc.* **124,** 728–729 (2002).
12. Collins, P. G., Arnold, M. S. & Avouris, Ph. *Science* **292,** 706–709 (2001).
13. Wind, S., Appenzeller, J., Martel, R., Derycke, V. & Avouris, Ph. *Appl. Phys. Lett.* **80,** 3817–3819 (2002).