

Low-Resistance Electrical Contact to Carbon Nanotubes With Graphitic Interfacial Layer

Yang Chai, Arash Hazeghi, Kuniharu Takei, Hong-Yu Chen, *Student Member, IEEE*, Philip C. H. Chan, *Fellow, IEEE*, Ali Javey, and H.-S. Philip Wong, *Fellow, IEEE*

Abstract—Carbon nanotubes (CNTs) are promising candidates for transistors and interconnects for nanoelectronic circuits. Although CNTs intrinsically have excellent electrical conductivity, the large contact resistance at the interface between CNT and metal hinders its practical application. Here, we show that electrical contact to the CNT is substantially improved using a graphitic interfacial layer catalyzed by a Ni layer. The p-type semiconducting CNT with graphitic contact exhibits high ON-state conductance at room temperature and a steep subthreshold swing in a back-gate configuration. We also show contact improvement to the semiconducting CNTs with different capping metals. To study the role of the graphitic interfacial layer in the contact stack, the capping metal and Ni catalyst were selectively removed and replaced with new metal pads deposited by evaporation and without further annealing. Good electrical contact to the semiconducting CNTs was still preserved after the new metal replacement, indicating that the contact improvement is attributed to the presence of the graphitic interfacial layer.

Index Terms—Amorphous carbon, carbon nanotube (CNT), contact, field-effect transistor, graphene, graphitic, interface.

I. INTRODUCTION

ELECTRICAL contact is an indispensable part in integrated circuits. The small contact area between carbon nanotubes (CNTs) and metal electrode makes electrical coupling between them extremely difficult [1]–[3]. The large electrical contact resistance hinders the practical electronics applications of the CNTs, although it has high intrinsically electrical conductivity [2], [3]. The contact between semiconducting CNT (*s*-CNT) and metal is generally modeled as a Schottky barrier (SB), resulting from the Fermi level mismatch between

s-CNT and metal electrode [4]–[6]. However, experimental results have shown that the contact resistance is still large for the CNTs with metallic band structure [2], where the SB should not exist at the interface between metallic CNT and metal. This indicates that there is additional contact barrier or series resistance for metallic CNT/metal. Recent experimental results on both semiconducting and metallic CNT devices revealed that surface chemistry is very important for forming good electrical contact between CNT and metal [7], [8]. The metal wetting to the tubular structure of the CNT is imperfect, where the metal atoms are not fully covered on the CNT surface. An atomic-level physical gap exists between CNT and metal [9], [10]. The cohesion between metal and *sp*² carbon is inversely correlated with the metal-carbon distance [11]. Researchers also experimentally and theoretically demonstrated that the contact resistance to the CNT is dependent on the contact length, indicating that the contact resistance has a spreading resistance component [12]–[15].

To develop the CNT-based electronics to achieve its full performance potential, it is imperative to minimize the contact resistance to the CNT device. For Si CMOS technology, metal silicides have been widely used for ohmic contacts [1]. For Si nanowire, doped epitaxial Si has been reported for the use of the contact material [16]. For carbon-based large-band-gap semiconductors, such as silicon carbide and diamond, a graphitic carbon layer has been used to form ohmic contact [17]–[19]. Graphitic carbon, with metal-like resistivity, similar chemical bonding to the CNT, and much better wettability to the CNT than other regular metal, is possibly a low-resistance contact material to the CNT. Recently, researchers have used electron-beam-induced carbon deposition to the CNT/metal contact region inside a scanning electron microscope (SEM) or transmission electron microscope (TEM) and formed low-resistance electrical contact to multiwalled CNT [20]–[26]. The graphitization of the carbon layer can be formed via dehydrogenation by electron beam irradiation. Kane et al. reported that electrical contact to the single-walled metallic CNT device was greatly improved by a high-temperature annealing process in vacuum [27], [28]. They showed that the chemisorbed carbonaceous contamination to the CNT surface can be graphitized with the high-temperature anneal process [27], [28]. In an earlier work, we have used amorphous carbon (*a*-C) as the interfacial layer between the metal and the single-walled metallic CNT. After the graphitization of the *a*-C assisted by Ni catalyst, the electrical contact to the metallic CNT has been substantially improved [3]. Theoretical calculations also suggested that good electrical contact can be formed between the CNT and the

Manuscript received May 25, 2011; revised July 25, 2011, August 15, 2011, September 15, 2011, and September 21, 2011; accepted September 25, 2011. Date of publication October 31, 2011; date of current version December 23, 2011. This work was supported in part by the Focus Center for Functional Engineered Nano Architectonics, which is one of the six research centers funded under the Focus Center Research Program, a Semiconductor Research Corporation subsidiary; by the Research Grant Council of Hong Kong Government under CERG Grant HKUST 611307; by the Berkeley Sensors and Actuators Center; and by the World Class University program. The review of this paper was arranged by Editor A. C. Seabaugh.

Y. Chai, H.-Y. Chen, and H.-S. P. Wong are with the Department of Electrical Engineering and the Center for Integrated Systems, Stanford University, Stanford, CA 94305 USA (e-mail: hspwong@stanford.edu).

A. Hazeghi is with Quswami Inc., San Francisco, CA 94111 USA.

K. Takei and A. Javey are with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA 94720 USA.

P. C. H. Chan is with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong, and the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Kowloon, Hong Kong.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TED.2011.2170216

graphitic carbon [29], [30]. In this paper, we show that the use of a graphitic carbon (*G-C*) interfacial layer to *s*-CNT can improve the electrical contact to the *s*-CNT and reduce the subthreshold swing of transistors with these improved contacts.

II. FABRICATION OF TEST STRUCTURE

We used a 4-in Si wafer coated with 200-nm-thick thermal oxide as the substrate. We grew the horizontally aligned CNTs on quartz wafers and transferred the CNTs to the Si/SiO₂ substrate. The detailed CNT growth and transfer process has been described elsewhere [31]. The average diameter of the CNTs is 1.2 nm in this work. The patterns of the metal electrodes were defined by a standard photolithography process. The metal was deposited by *e*-beam evaporation and then lifted off. The active region of the CNT device was defined by another photolithography process. The rest of the CNT outside the active region was etched away by oxygen plasma. The average site density of the CNTs is 2 CNT/ μm . The number of CNTs for devices with 1- μm channel width ranges from 1 to 3. In this paper, we select the devices with only a single CNT and report their electrical characterization.

III. RESULTS

The CNT field-effect transistor (FET) with metal side-contacted configuration (metal/CNT sidewall) has been shown to work as an SB transistor, where the SB height is mainly determined by the metal work function and the band gap of *s*-CNT [4]–[6]. For a typical p-type CNT transistor, the metal with high work function forms small SB height contact, as schematically shown in Fig. 1(a), where the Fermi level of the metal aligns well with the valence band of the CNT. Palladium (Pd), which is a noble metal with high work function and good wetting interactions with CNT, has been found with good electrical contact to both semiconducting and metallic CNTs [32], [33]. In this paper, we used five kinds of metal with different work functions as the contact to the single CNT. The CNT extends beyond the electrodes and make side contacts to the electrodes. The devices were electrically characterized at room temperature in air ambient with p-type doped Si substrate as the back-gate electrode. Five different kinds of metal electrodes (Pd, Pt, Au, Ti, and W) were fabricated on different CNTs. Fig. 1(b) shows the representative I_d - V_{gs} transfer curves of the CNT devices with different metal contacts, where the channel length defined by the source–drain electrode is 1 μm . All the devices show p-type dominant transport characteristics. The ON-state conductance of the *s*-CNTs shows no obvious dependence on the metal work function. Although Pt has the highest work function (5.9 eV) in this group of metals, the ON-state current of Pt contacted CNFET is much lower than that of the devices with other capping metals. The expected low contact barrier according to the SB theory was not realized in the case of Pt contact. The high contact resistance with Pt contact has been attributed to the dewetting property of Pt to the CNT [9]. Instead of a uniformly coated contact region, the deposited Pt and Au typically form nanoclusters that cover the CNT surface discretely [9], [10]. The atomic vacuum gap

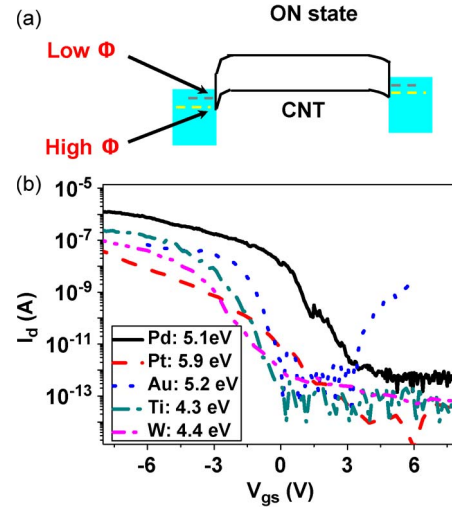


Fig. 1. Electrical characterization of the *s*-CNT devices with different contact metals. (a) Schematic energy band diagram of the ON-state (p-channel only) for the SB-type CNT devices with different contact metals. The high-work-function metal forms a small SB barrier to the *s*-CNT. (b) Representative I_d - V_{gs} transfer curves of single CNT devices with Pt, Pd, Au, Ti, and W contact metal. $V_{d,s}$ is -1 V. The channel length is 1 μm . The ON current of the CNT devices shows no obvious dependence on the metal work function.

results in a large series contact resistance or a physical barrier. In contrast, Ti has a lower work function (4.4 eV) than Pt, but the CNT devices with Ti contact show better conductance than the Pt contact devices. These results clearly indicate that the electrical contact resistance to *s*-CNT is not only determined by the SB height but also correlates the cohesive strength of the electrode-carbon interface [11]. Theoretical work has showed that the contact resistance to CNT also depends on the contact length, the coupling conductance, and the mean-free path of the CNT [15]. To further understand the contact resistance to CNT, we need to consider the factors previously mentioned.

Compared to regular metal contact, carbon itself is a material with the best wettability to the CNT surface. In this paper, we deposited a thin carbon film (“nominal” thickness ~ 2 nm) by *e*-beam evaporation method on top of the CNT surface as an interfacial layer. The carbon layer was only located at the contact region to CNT. The pattern of carbon layer was defined by photolithography and lift off. The as-deposited carbon has an amorphous structure, consisting of both sp^2 and sp^3 bonding. The amorphous carbon (*a-C*) can be graphitized with the assistance of a transitional metal catalyst at high temperature [34], [35]. Fig. 2(a) shows the schematic of the formation of the graphitic interfacial layer. We used a thin Ni layer (~ 5 nm) as the catalyst on top of the *a-C* layer with the same pattern. The whole stack was annealed at a temperature of 850 $^\circ\text{C}$ in a furnace, where the chamber was pumped to base pressure (~ 50 mtorr) by a mechanical pump before raising to high temperature. The anneal process was then conducted in Ar or H₂ ambient. After the anneal process, the CNT is fully wrapped by graphitic carbon (*G-C*), as schematically depicted in Fig. 2(b). Zheng *et al.* showed that graphene formed on top of the Ni surface with a similar process [34], whereas our experimental results suggested that the graphitic carbon can form both on top and underneath the Ni layer if the Ni thickness is optimized. We prepared a cross-sectional TEM sample to characterize the

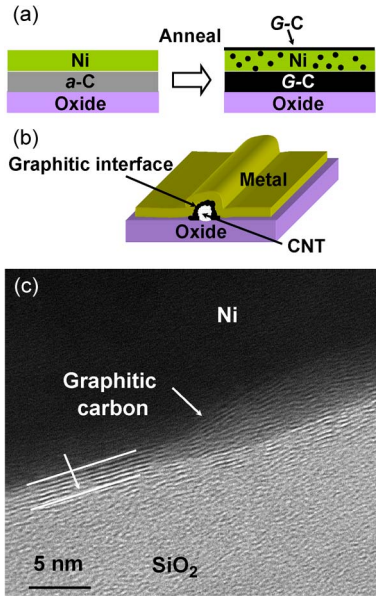


Fig. 2. Characterization of the graphitic interfacial layer. (a) Process flow of introducing the graphitic interfacial layer between the CNT and the metal electrode. The graphitic carbon is crystallized by the Ni catalyst on top of the *a*-C. (b) Schematic of the CNT/metal interface with the *G*-C interfacial layer. The metal electrode wetting to the CNTs is greatly improved by the *G*-C interfacial layer. (c) Cross-sectional TEM image of the *G*-C interfacial layer sandwiched between metal and oxide.

interface underneath the Ni layer. The cross-section TEM image in Fig. 2(c) clearly shows the presence of *G*-C, which has multiple layers and is sandwiched between metal and oxide. The lattice distance of the *G*-C is 3.4 Å, which is the hallmark of the graphite (2 0 0) direction. Our results are also in agreement with the results by Itoh [35]. The *G*-C interfacial layer has good wetting to both the metal and the CNTs, and the similar sp^2 structure to the CNTs. The vacuum gaps between the metal and the CNT are bridged by the *G*-C layer. In the ideal case, the coupling between the layers of the graphite is weak. However, the CNT produced by chemical vapor deposition method is typically defective. The anneal process was conducted at a high temperature with both solid carbon and Ni catalyst. These conditions are similar to the CNT growth process. It is reasonable to expect that the *a*-C possibly reacts with the defective sites in the CNTs assisted by Ni catalyst, forming a strong chemical bonding to the CNT at the contact region. The *G*-C interfacial layer with covalent chemical bonding to the CNTs enlarges the actual contact area between the CNTs and the metal, and provides more conduction channels at the contact region. The graphitic layer has a ~ 2 -nm thickness, a micrometer width, and many defective sites (characterized by Raman spectroscopy subsequently). These help the carriers transport through the graphitic interfacial layer easily. Thus, the *G*-C interfacial layer helps establish the low-resistance electrical contact to the single-walled CNT. To compare the effect of the *G*-C interfacial layer on the electrical contact to the CNTs, we fabricated the electrical contact with and without the *G*-C layer on the same CNT to minimize the variations resulting from the different CNTs. Fig. 3(a) and (b) shows the schematic of the process flow and the SEM images of our test structures. The dimension of the metal contact finger to the CNT is 5 μm .

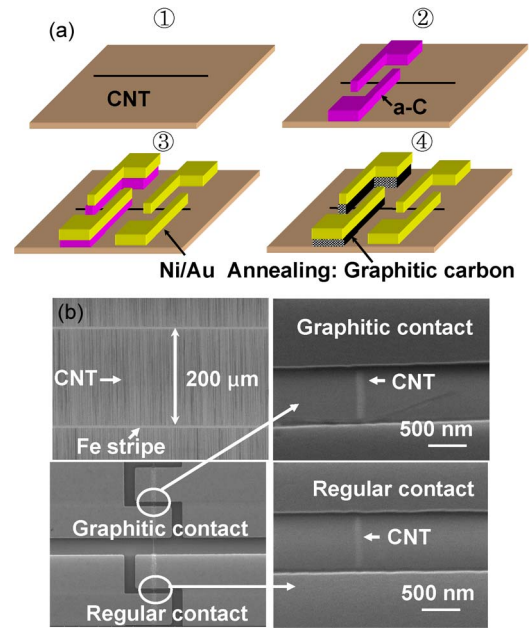


Fig. 3. Process flow and SEM images of the devices. (a) Schematic of the process flow for fabricating the devices. (b) SEM images of the horizontally aligned CNTs and the test structures on the same CNT with and without the *G*-C interfacial layer.

Fig. 4(a) shows the I_d - V_{gs} transfer curves of the same CNT with and without the *G*-C interfacial layer at a V_{ds} of -1 V. The capping metal is Ni/Au, where Ni is the catalyst for graphitization and Au is used for protecting Ni oxidation. Here, a slash “/” between the different metals indicates the deposition sequence. (Ni was deposited first, and Au was deposited afterward.) Since the devices with and without the interfacial contacts are fabricated on the same CNT with the same channel length, it is reasonable to conclude that the current level difference is a direct result of electrical contact improvement at the interface. Before the anneal process, the interfacial layer still has an amorphous structure. The ON-current of the CNT devices with and without the *a*-C interfacial layer shows negligible difference within the range of normal device variation. Although the *a*-C layer has better wettability than the Ni/Au metal pad, the sp^3 bonding carbon is insulating. Its effect on the contact is similar to the vacuum gap. Therefore, the *a*-C interfacial layer does not improve the electrical contact to CNT too much prior to the annealing.

After the anneal process, both the CNT devices with and without the *G*-C layers show ON-current improvement. However, we believe that the reasons for contact improvement in these two structures are different. For the device without the *G*-C interfacial layer, the reduction in the contact resistance or the potential barrier is most likely to result from the heat-induced desorption of adsorbates or the relaxation of structural imperfection at the interface. Similar contact improvements to the CNT devices have been realized by local Joule heating [36], [37], rapid thermal annealing [38], and vacuum annealing [27]. Fig. 4(b) shows the I_d - V_{ds} output curves of the CNT device without the *G*-C layer after the annealing process, exhibiting a nonlinear relationship at low V_{ds} . The V_{gs} was swept from -10 to -2 V in steps of 2 V. The shape of the I_d - V_{ds} curve

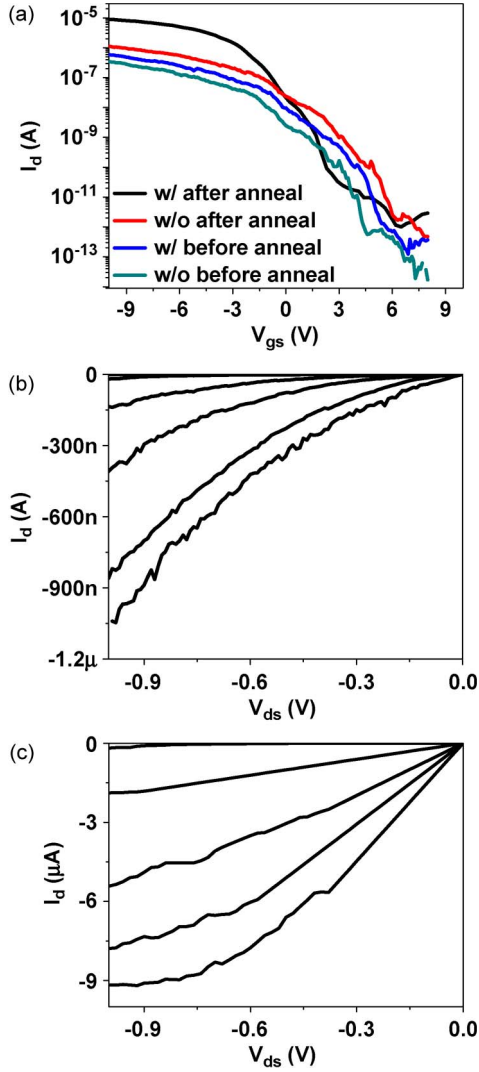


Fig. 4. Electrical characteristics of the CNT devices with the graphitic interfacial layer. (a) I_d - V_{gs} curves of the same CNT devices with and without the G -C interfacial layer, where the channel length is $1 \mu\text{m}$, and V_{ds} is -1 V . The ON current of the CNT is substantially improved by the G -C interfacial layer. Output I_d - V_{ds} curves of the same s -CNT (b) without and (c) with the G -C interfacial layer. V_{gs} was swept from -10 to -2 V in steps of 2 V .

indicates that there is a potential barrier at the contact region, although the annealing process improves the electrical contact by a small amount. The CNFET without the G -C layer in this work has the geometry of side contact, planar back gate, and planar channel. Its subthreshold slope is determined by not only the electrostatics of the device structure but also the carrier injection at the contact region [4], [39]. The contact barrier width in the SB-type CNFET is modulated by the gate electric field, leading to a large subthreshold slope [4].

The ON-current of the CNT device with the G -C layer is substantially improved after the annealing process. In addition to the effects of the desorption of adsorbates and the relaxation of imperfect structure, the a -C is crystallized into the G -C and possibly forms chemical bonding with the defective sites in the CNTs. This G -C layer extends the effective wave-function overlap to the CNTs, improving the electrical contact of the interface [27]. The steep subthreshold swing provides additional evidences that chemical reactions occur in the contact region.

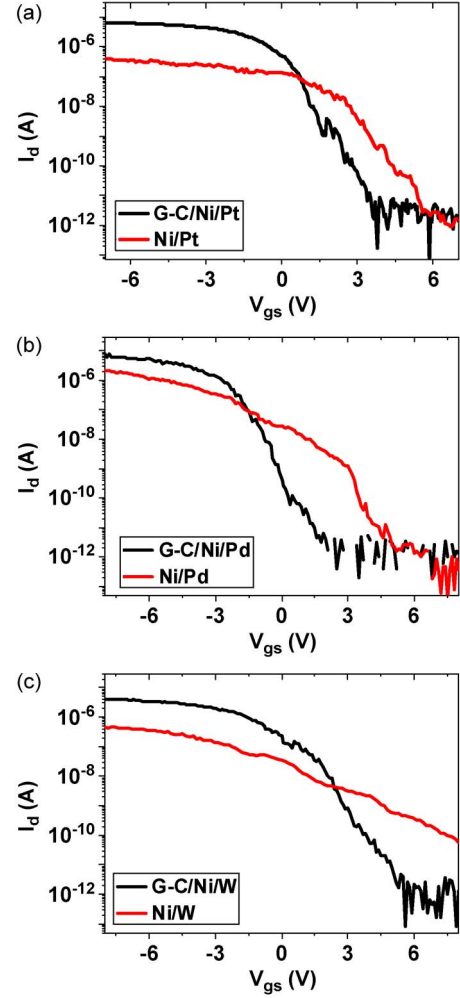


Fig. 5. Electrical characteristics of the CNT devices with different contact metals. (a) Transfer I - V curves of the Ni/Pt contact devices of the same CNT with and without the G -C interfacial layer after the anneal process, showing substantial improvement with the G -C interfacial layer. Transfer I_d - V_{gs} curves of (b) Ni/Pd and (c) Ni/W with and without the G -C interfacial layer, also exhibiting ON-current improvement and subthreshold swing reduction.

The shape of the I_d - V_{ds} output curve of the CNT device with the G -C layer (Fig. 4(c), V_{gs} was swept from -10 V to -2 V in steps of 2 V) exhibits linear regions at low V_{ds} and saturation regions at high V_{ds} . This suggests that the contact barrier between the metal and the CNT is greatly decreased with the G -C interfacial layer.

The annealing at high temperature with the G -C interfacial layer involves both physical and chemical property change. The exact nature of the contact remains unclear at this point. Here, we present a plausible explanation for the observations that the subthreshold region becomes steeper after introducing the G -C interfacial layer. As we discussed previously, the anneal of the a -C assisted by Ni may help form chemical bonding to the defective sites in the CNTs. The contact barrier between the metal electrode and the CNT is greatly reduced with the G -C interfacial layer. The device characteristics appear to only have the thermal subthreshold slope, which is normally steep. Thus, the subthreshold slope of CNFET becomes smaller when we introduced the G -C layer. The function of the G -C layer is similar to a source-drain electrode. The ‘‘artificial’’ source-drain

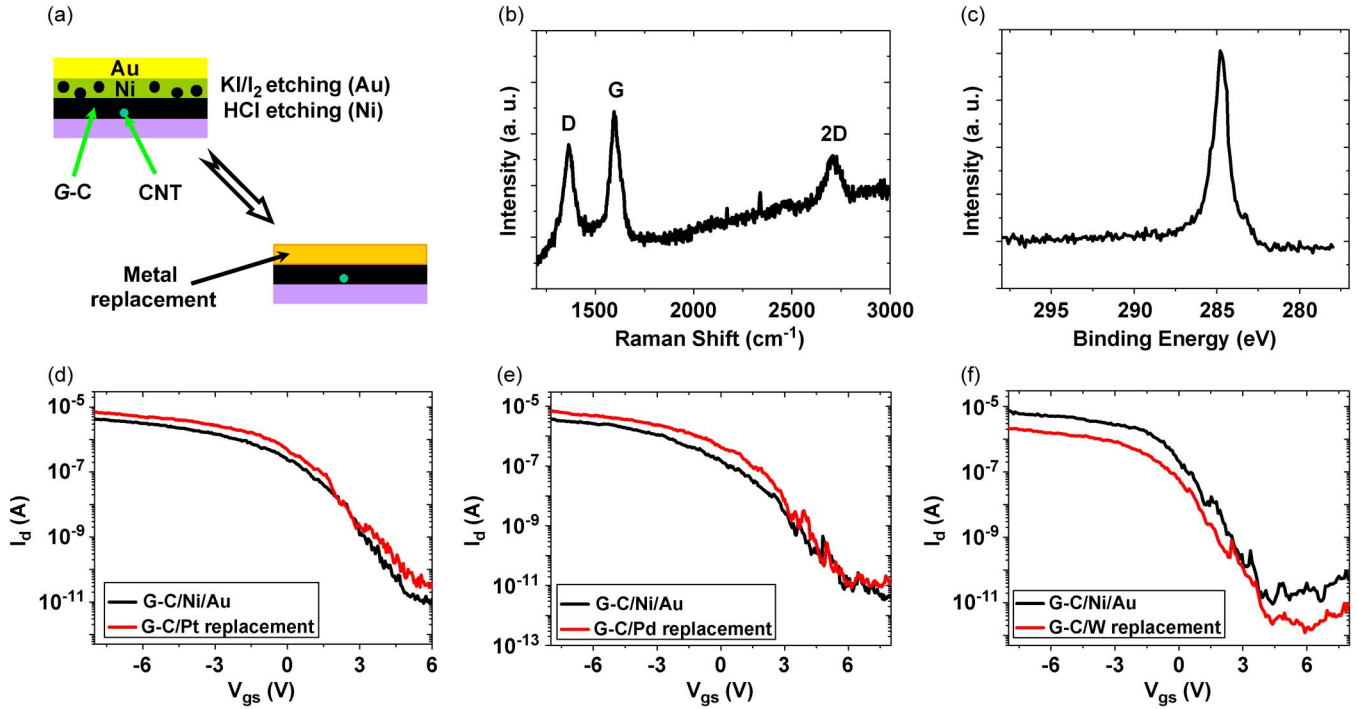


Fig. 6. Characteristics of the graphitic CNT device replaced by other capping metals. (a) Schematic of the process for removing Ni/Au metal and replacing with other metals without further anneal. (b) Raman spectroscopy and (c) XPS of the *G-C/Ni/Au* stack after Ni/Au wet etching. The material analysis clearly showed that the graphitic layer preserved well after the wet-etching process. I_d - V_{gs} transfer curves of the graphitic contact CNT devices with (d) Pt, (e) Pd, and (f) W metal replacement.

electrodes with doped CNT segment have been demonstrated previously [40], [41]. The extended source-drain electrode could be doped to form p- or n-type contacts. In our work, the *G-C* layer is under the metal pad. Doping the CNTs under the metal with graphitic layer may help make p-type contact and n-type contact similar to the work reported with Si nanowire FET [16]. More investigations are needed to clearly understand the interface between the graphitic layer and the CNT.

We have shown contact improvement to *s*-CNT with the *G-C/Ni/Au* stack. To investigate the effect of the capping metal on top of the *G-C* layer, we also choose the capping metal with different work functions and chemistry properties. Fig. 5 shows the representative electrical characteristics of the CNFETs with the *G-C/Ni/Pt*, *G-C/Ni/Pd*, and *G-C/Ni/W* stack. Although the CNT devices show different characteristics due to CNT-to-CNT variation, all of them exhibit high ON-current level after the use of the *G-C* interfacial layer. Similar to the *G-C/Ni/Au* contact, they also exhibit steeper subthreshold region compared with devices without the *G-C* layer. After the use of the *G-C* interfacial layer, the average resistance of the CNT devices with different kinds of capping metal is reduced to a similar level. A noticeable example is devices with Pt capping metal, which typically have high contact resistance to the CNTs [7], [9]. The contact resistance of the Pt-contacted CNT device is greatly reduced with the *G-C* interfacial layer. These results suggest that the electrical contacts to the CNTs with different capping metals can be improved with the use of the *G-C* interfacial layer.

In the preceding experiments, we used capping metal Au to protect the Ni from oxidation, which also served as the metal pad. The Ni/Au stack underwent the high-temperature anneal process. To understand the role of the *G-C* layer in contact im-

provement, we removed the Ni/Au capping metal by wet etching (KI/I₂ and HCl), as schematically shown in Fig. 6(a). Then, we replaced with other kinds of as-deposited metal without further annealing process. Fig. 6(b) shows the Raman spectrum of the sample after removing the Ni/Au layer. The sharp G (~1571 cm⁻¹) peak is clearly observed in the Raman spectrum, indicating that the *G-C* layer is still preserved after wet chemical etching. The high D peak (~1350 cm⁻¹) suggests the presence of many defective sites in the graphitic layer, providing carrier conduction paths through the graphitic layers. Fig. 6(c) shows x-ray spectroscopy (XPS) of the sample after removing the Ni/Au layer. The C1s peak (~284 eV) in XPS spectroscopy shows that the majority of the carbon is in graphitic form, indicating that the *sp*³ carbon in *a*-C has been converted to the *sp*² carbon by the annealing process assisted with the Ni catalyst. The average site density of the CNTs is 2 μm in this work, and the active region is 1 μm wide. One or two single-walled CNTs are beyond the XPS detection limit. We believe that the peaks in the spectrums resulted from the graphitic carbon layer (100 μm × 100 μm). These spectroscopy analyses are in agreement with the cross-sectional TEM result shown in Fig. 2(c), indicating that the *G-C* layer exists underneath the Ni catalyst and preserves well after the selective etching process.

Fig. 6(d)-(f) shows the I_d - V_{gs} transfer curves of the same CNT devices with annealed metal pad and with other replaced capping metals. The pattern of the metal pad was defined by photolithography using an ASML stepper. This allows us to precisely locate the different kinds of metal on the original CNT. Although the devices with the replaced metal show different electrical characteristics, they still exhibit a similar ON-current level compared to the device with the annealed Ni/Au

capping metal. From this control experiment, we are able to conclude that the contact improvement in our experiment indeed comes from the presence of the *G-C* interfacial layer, instead of heat-induced relaxation. The devices with Pt-, Pd-, and W-replacement show similar *I-V* characteristics to the Au contacted device on the same CNT. This suggests that the Ni/*G-C* is the dominant factor for the contact barrier to the CNT in this case.

IV. CONCLUSION

In summary, a *G-C* interfacial layer has been introduced by the crystallization of the *a-C*. The low-resistance electrical contact has been established to the *s-CNTs* with different capping metals using the *G-C* interfacial layer. The reduction in the contact resistance has been attributed to the improved wetting and the formation chemical bonding to the CNTs. The actual contact area to CNT is enlarged due to the presence of the *G-C* interfacial layer. Selective removal of capping metal and subsequent replacement with other metals indicates that the contact improvement is indeed from the presence of the *G-C* interfacial layer. Our works not only provide an alternative approach to forming good electrical contact to the CNTs but also help to understand the nature of the contact interface at nanoscale.

ACKNOWLEDGMENT

Device fabrication was performed in the Stanford Nanofabrication Facility, which is a node of the National Nanotechnology Infrastructure Network, which, in turn, is funded by the National Science Foundation.

REFERENCES

- J. P. Gambino and E. G. Colgan, "Silicides and ohmic contacts," *Mater. Chem. Phys.*, vol. 52, no. 2, pp. 99–146, Feb. 1998.
- W. Kim, A. Javey, R. Tu, J. Cao, Q. Wang, and H. J. Dai, "Electrical contacts to carbon nanotubes down to 1 nm in diameter," *Appl. Phys. Lett.*, vol. 87, no. 17, pp. 173 101–173 103, Oct. 2005.
- Y. Chai, A. Hazeghi, K. Takei, H. Y. Chen, P. C. H. Chan, A. Javey, and H.-S. P. Wong, "Graphitic interfacial layer to carbon nanotube for low electrical contact resistance," in *IEDM Tech. Dig.*, Dec. 2010, pp. 210–213.
- S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, "Carbon nanotubes as Schottky barrier transistors," *Phys. Rev. Lett.*, vol. 89, no. 10, pp. 106801-1–106801-4, Sep. 2002.
- Z. Chen, J. Appenzeller, J. Knoch, Y. M. Lin, and P. Avouris, "The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors," *Nano Lett.*, vol. 5, no. 7, pp. 1497–1502, Jul. 2005.
- Y. Noshu, Y. Ohno, S. Kishimoto, and T. Mizutani, "Relation between conduction property and work function of contact metal in carbon nanotube field-effect transistors," *Nanotechnology*, vol. 17, no. 14, pp. 3412–3415, Jul. 2006.
- S. C. Lim, J. H. Jang, D. J. Bae, G. H. Han, S. Lee, I.-S. Yeo, and Y. H. Lee, "Contact resistance between metal and carbon nanotube interconnects: Effect of work function and wettability," *Appl. Phys. Lett.*, vol. 95, no. 26, pp. 264103-1–264103-3, Dec. 2009.
- D. McClain, N. Thomas, S. Youkey, R. Schaller, J. Jiao, and K. P. O'Brien, "Comparative investigation of the effect of oxygen adsorbate and electrode work function on carbon-nanotube field-effect transistors," *IEEE Electron Device Lett.*, vol. 31, no. 2, pp. 156–158, Feb. 2010.
- S. Lee, S. J. Kahng, and Y. Kuk, "Nano-level wettings of platinum and palladium on single-walled carbon nanotubes," *Chem. Phys. Lett.*, vol. 500, no. 1–3, pp. 82–85, Nov. 2010.
- Y. Zhang, N. W. Franklin, R. J. Chen, and H. J. Dai, "Metal coating on suspended carbon nanotubes and its implications to metal-tube interaction," *Chem. Phys. Lett.*, vol. 331, no. 1, pp. 35–41, Nov. 2000.
- Y. Matsuda, W. Q. Deng, and W. A. Goddard, III, "Contact resistance properties between carbon nanotubes and various metals from quantum mechanics," *J. Phys. Chem. C*, vol. 111, pp. 11 113–11 116, 2007.
- C. Lan, D. N. Zakharov, and R. G. Reifengerger, "Determining the optimal contact length for a metal/multiwalled carbon nanotube interconnect," *Appl. Phys. Lett.*, vol. 92, no. 21, pp. 213112-1–213112-3, May 2008.
- C. Lan, P. Srisungsitthisunti, P. B. Amama, T. S. Fisher, X. Xu, and R. G. Reifengerger, "Measurement of metal/carbon nanotube contact resistance by adjusting contact length using laser ablation," *Nanotechnology*, vol. 19, no. 12, p. 125 703, Mar. 2008.
- A. D. Franklin and Z. Chen, "Length scaling of carbon nanotube transistors," *Nat. Nanotechnol.*, vol. 5, no. 12, pp. 858–862, Dec. 2010.
- P. M. Solomon, "Contact resistance to a one-dimensional quasi-ballistic nanotube/wire," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 246–248, Mar. 2011.
- G. M. Cohen, M. J. Rooks, J. O. Chu, S. E. Laux, P. M. Solomon, J. A. Ott, R. J. Miller, and W. Haensch, "Nanowire metal–oxide–semiconductor field effect transistor with doped epitaxial contacts for source and drain," *Appl. Phys. Lett.*, vol. 90, no. 23, pp. 233110-1–233110-3, Jun. 2007.
- I. P. Nikitina, K. V. Vassilevski, N. G. Wright, A. B. Horsfall, A. G. O'Neill, and C. M. Johnson, "Formation and role of graphite and nickel silicide in nickel based ohmic contacts to n-type silicon carbide," *J. Appl. Phys.*, vol. 97, no. 8, pp. 083709-1–083709-7, Apr. 2005.
- W. Lu, W. C. Mitchel, G. R. Landis, T. R. Crenshaw, and W. E. Collins, "Catalytic graphitization and Ohmic contact formation on 4H-SiC," *J. Appl. Phys.*, vol. 93, no. 9, pp. 5397–5403, May 2003.
- M. Yokoba, Y. Koide, A. Otsuki, F. Ako, T. Oku, and M. Murakami, "Carrier transport mechanism of Ohmic contact to p-type diamond," *J. Appl. Phys.*, vol. 81, no. 10, pp. 6815–6821, May 1997.
- Q. Chen, S. Wang, and L. M. Peng, "Establishing Ohmic contacts for in situ current-voltage characteristic measurements on a carbon nanotube inside the scanning electron microscope," *Nanotechnology*, vol. 17, no. 4, pp. 1087–1098, Feb. 2006.
- K. Rykaczewski, M. R. Henry, and A. G. Fedorov, "Electron beam induced deposition of residual hydrocarbons in the presence of a multiwall carbon nanotube," *Appl. Phys. Lett.*, vol. 95, no. 11, pp. 113112-1–113112-3, Sep. 2009.
- K. Rykaczewski, M. R. Henry, S. K. Kim, A. G. Fedorov, D. Kulkarni, S. Singamaneni, and V. V. Tsukruk, "The effect of geometry and material properties of a carbon joint produced by electron beam induced deposition on the electrical resistance of a multiwalled carbon nanotube-to-metal contact interface," *Nanotechnology*, vol. 21, no. 3, pp. 035202-1–035202-12, Jan. 2010.
- F. Banhar, "The formation of a connection between carbon nanotubes in an electron beam," *Nano Lett.*, vol. 1, no. 6, pp. 329–332, 2001.
- Y. Yoshikawa, S. Akita, and Y. Nakayamai, "Barrier modification at contacts between carbon nanotube and Pt electrode using well-controlled Joule heating," *Jpn. J. Appl. Phys.*, vol. 46, no. 15, pp. L359–L361, Apr. 2007.
- A. Andoa, T. Shimizub, H. Abeb, Y. Nakayamac, and H. Tokumotod, "Improvement of electrical contact at carbon nanotube/Pt by selective electron irradiation," *Phys. E*, vol. 24, no. 1/2, pp. 6–9, Aug. 2004.
- Y. H. Kahng, J. Choi, B. C. Park, D. H. Kim, J. H. Choi, J. Lyon, and S. J. Ahn, "The role of an amorphous carbon layer on a multi-wall carbon nanotube attached atomic force microscope tip in making good electrical contact to a gold electrode," *Nanotechnology*, vol. 19, no. 19, pp. 195705-1–195705-7, May 2008.
- A. A. Kane, T. Sheps, E. T. Branigan, V. A. Apkarian, M. H. Cheng, J. C. Hemminger, S. R. Hunt, and P. G. Collins, "Graphitic electrical contacts to metallic single-walled carbon nanotubes using Pt electrodes," *Nano Lett.*, vol. 9, no. 10, pp. 3586–3591, Oct. 2009.
- A. A. Kane, K. Loutherbach, B. R. Goldsmith, and P. G. Collins, "High temperature resistance of small diameter, metallic single-walled carbon nanotube devices," *Appl. Phys. Lett.*, vol. 92, no. 8, pp. 083506-1–083506-3, Feb. 2008.
- S. Paulson, A. Helsen, M. B. Nardelli, R. M. Taylor, II, M. Falvo, R. Superfine, and S. Washburn, "Tunable resistance of a carbon nanotube/graphite interface," *Science*, vol. 290, no. 5497, pp. 1742–1744, Dec. 2000.
- F. D. Novaes, R. Rurali, and P. Ordejon, "Electronics transport between graphene layers covalently connected by carbon nanotube," *ACS Nano*, vol. 4, no. 12, pp. 7596–7602, Dec. 2010.
- N. Patil, A. Lin, E. R. Myers, K. Ryu, A. Badmave, C. W. Zhou, H.-S. P. Wong, and S. Mitra, "Wafer-scale growth and transfer of aligned single-walled carbon nanotubes," *IEEE Trans. Nanotechnol.*, vol. 8, no. 4, pp. 498–504, Jul. 2009.

- [32] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, no. 6949, pp. 654–657, Aug. 2003.
- [33] D. Mann, A. Javey, J. Kong, Q. Wang, and H. J. Dai, "Ballistic transport in metallic nanotubes with reliable Pd Ohmic contacts," *Nano Lett.*, vol. 3, no. 11, pp. 1541–1544, 2003.
- [34] M. Zheng, K. Takei, B. Hsia, H. Fang, X. B. Zhang, N. Ferralis, H. Ko, Y. L. Chueh, Y. G. Zhang, R. Maboudian, and A. Javey, "Metal-catalyzed crystallization of amorphous carbon to graphene," *Appl. Phys. Lett.*, vol. 96, no. 6, pp. 063110-1–063110-3, Feb. 2010.
- [35] T. Itoh, "Study of reactions in transition metal/amorphous carbon layered thin films using transmission electron microscopy," Ph.D. dissertation, Stanford Univ., Stanford, CA, 1996.
- [36] L. Dong, S. Youkey, J. Bush, J. Jiao, V. M. Dubin, and R. V. Chebiam, "Effects of local Joule heating on the reduction of contact resistance between carbon nanotubes and metal electrodes," *J. Appl. Phys.*, vol. 101, no. 2, pp. 024320-1–024320-7, Jan. 2007.
- [37] Y. Woo, G. S. Duesberg, and S. Roth, "Reduced contact resistance between an individual single-walled carbon nanotube and a metal electrode by a local point annealing," *Nanotechnology*, vol. 18, no. 9, pp. 095203-1–095203-7, Mar. 2007.
- [38] J.-O. Lee, C. Park, J.-J. Kim, J. Kim, J. W. Park, and K.-H. Yoo, "Formation of low-resistance ohmic contacts between carbon nanotube and metal electrodes by a rapid thermal annealing method," *J. Phys. D, Appl. Phys.*, vol. 33, no. 16, pp. 1953–1956, Aug. 2000.
- [39] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field effect transistors," *Phys. Stat. Sol.*, vol. 205, no. 4, pp. 679–694, Apr. 2008.
- [40] Y. M. Lin, J. Appenzeller, J. Knoch, and P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable polarities," *IEEE Trans. Nanotechnol.*, vol. 4, no. 5, pp. 481–489, Sep. 2005.
- [41] A. Javey, R. Tu, D. B. Farmer, J. Guo, R. G. Gordon, and H. J. Dai, "High performance n-type carbon nanotube field-effect transistors with chemically doped contact," *Nano Lett.*, vol. 5, no. 2, pp. 345–348, Feb. 2005.



Yang Chai received the Ph.D. degree from The Hong Kong University of Science and Technology, Kowloon, Hong Kong, in 2009.

He is currently with the Department of Electrical Engineering and the Center for Integrated Systems, Stanford University, Stanford, CA, working on the fabrication of carbon-related materials and carbon-based devices, including testing and characterization of the resulting prototypes.



Arash Hazeghi received the M.Sc. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, in 2006 and 2011, respectively.

During his time at Stanford, he was a member of the Stanford Nanoelectronics Group led by Prof. Wong. He is currently a Device Research Scientist with Quswami Inc., San Francisco, CA. His major publications include a carbon nanotube (CNT) field-effect-transistor ballistic model with Schottky barriers and integrated capacitance bridge for high-resolution wide-temperature range quantum capacitance measurements in nanostructures. His research interests include theoretical and experimental investigation of ballistic electron transport in 1-D mesoscopic systems, with main focus on CNT systems for high-performance logic applications.



Kuniharu Takei received the B.S., M.S., and Ph.D. degrees from Toyohashi University of Technology, Aichi, Japan, in 2003, 2006, and 2009, respectively, all in electrical engineering. He is currently a Postdoctoral Fellow with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley.

During his Ph.D. studies, he focused on complementary metal-oxide-semiconductor/microelectromechanical-system integration for neural electronic interfaces such as spike signal recordings and drug deliveries. His research interests include nanomaterial integrations for high-performance electronics on any substrates, such as conventional Si substrate and flexible substrates.



Hong-Yu (Henry) Chen (S'10) received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 2007 and the M.S. degree from Stanford University, Stanford, CA, in 2011, both in electrical engineering. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering and the Center for Integrated Systems, Stanford University, Stanford, CA.

In the summer of 2011, he worked as an Intern in Applied Materials, Sunnyvale, CA, where he worked on high- k metal gate modeling. His research interests

include carbon nanotubes, particularly material synthesis, novel transistor device structures, very large scale integration fabrication and processing, and applications in phase change memory.



Philip C. H. Chan (SM-97-F'07) received the B.S. degree in electrical engineering from the University of California, Davis, in 1973 and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana-Champaign (UIUC), in 1975 and 1978, respectively.

He started his career as Postdoctoral Fellow and Assistant Professor with the UIUC. He later joined Intel Corporation in the U.S. and was promoted to Senior Project Manager. In 1991, he was a Reader and a Founding Member of the Hong Kong University of Science and Technology (HKUST), where he became the Chair

Professor of the Department of Electronic and Computer Engineering. Since September 2003, he has been the Dean of Engineering with HKUST. He has also served as the Director of the Microelectronics Fabrication Facility, HKUST, and has received a total research funding of HK\$71.7 million since he joined the university. He has also been a key player in the commercialization of the HKUST knowledge and technology. He is currently the Deputy President and Provost of Hong Kong Polytechnic University, Kowloon, Hong Kong. His research interests include very-large-scale-integration devices, circuits, and systems; microelectronics; electronic packaging; integrated sensors; semiconductor devices; and material research.

Dr. Chan is a Fellow of the Hong Kong Institution of Engineering (HKIE). In Hong Kong, he has served on various Innovation and Technology Commission and HKIE committees, and the Electronics Committee of the Industry and Trade Department Council. He has advised the government on the setup of the Hong Kong Applied Science and Technology Research Institute Company, Ltd., where he currently serves in its board and is the Chair of the Technology Committee. He has also served as a panel member on the Research Grant Council and the University Grants Committee's Research Assessment Panel. He has extensive network in the U.S. and has facilitated the collaboration between the HKUST and many topnotch engineering schools in the U.S., including the University of Pennsylvania, Cornell University, and the University of Southern California. He also holds honorary positions in various universities in the Chinese mainland. He is the recipient of the Electrical and Computer Engineering Distinguished Alumni Award from the UIUC in 2010.



Ali Javey received the Ph.D. degree in chemistry from Stanford University, Stanford, CA, in 2005.

He then joined the faculty of the University of California, Berkeley, where he is currently an Associate Professor of electrical engineering and computer sciences with the Department of Electrical Engineering and Computer Sciences. He is a Co-Director of the Berkeley Sensor and Actuator Center and serves as an Associate Editor for *ACS Nano*. His work focuses on the integration of nanoscale electronic materials for various technological appli-

cations, including novel nanoelectronics, flexible circuits and sensors, and energy generation and harvesting. His research interests include chemistry, materials science, and electrical engineering.

Prof. Javey was a Junior Fellow of the prestigious Harvard Society of Fellows from 2005 to 2006. He was the recipient of a number of awards, including the IEEE Nanotechnology Early Career Award (2010), Alfred P. Sloan Fellow (2010), Mohr Davidow Ventures Innovators Award (2010), National Academy of Sciences Award for Initiatives in Research (2009), Technology Review TR35 (2009), NSF Early CAREER Award (2008), U.S. Frontiers of Engineering by National Academy of Engineering (2008), and the Peter Verhofstadt Fellowship from the Semiconductor Research Corporation (2003).



H.-S. Philip Wong (S'81–M'82–SM'95–F'01) received the B.Sc. (Hons.) degree from the University of Hong Kong, Kowloon, Hong Kong, in 1982, the M.S. degree from the State University of New York at Stony Brook, in 1983, and the Ph.D. degree from Lehigh University, Bethlehem, PA, in 1988, all in electrical engineering.

He joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, in 1988. In September 2004, he joined Stanford University, Stanford, CA, as a Professor of electrical engineering with the Department of Electrical Engineering and the Center for Integrated Systems. While at IBM, he worked on charge-coupled device and complementary metal-oxide-semiconductor (MOS) image sensors, double-gate/multigate MOS field-effect transistor (FET), device simulations for advanced/novel MOSFET, strained silicon, wafer bonding, ultrathin-body silicon-on-insulator, extremely short gate FET, germanium MOSFET, carbon nanotube FET, and phase change memory. He held various positions from Research Staff Member to Manager, and Senior Manager. While he was Senior Manager, he had the responsibility of shaping and executing IBM's strategy on nanoscale science and technology, as well as exploratory silicon devices and semiconductor technology. His research interests include nanoscale science and technology, semiconductor technology, solid-state devices, electronic imaging, new materials, novel fabrication techniques, novel device concepts for future nanoelectronics systems, and explorations into device-driven circuits and systems. Novel devices often enable new concepts in circuit and system designs. His current research interests include carbon nanotubes, self-assembly, exploratory logic devices, nanoelectromechanical devices, novel memory devices, and biosensors.

Dr. Wong served on the IEEE Electron Devices Society (EDS) as elected AdCom member from 2001 to 2006. He served on the IEDM committee from 1998 to 2007 and was the Technical Program Chair in 2006 and General Chair in 2007. He served on the ISSCC program committee from 1998 to 2004 and was the Chair of the Image Sensors, Displays, and MEMS subcommittee from 2003 to 2004. He serves on the Executive Committee of the Symposia of VLSI Technology and Circuits. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON NANOTECHNOLOGY in 2005–2006. He has been a Distinguished Lecturer of the IEEE Electron Devices Society since 1999 and the Solid-State Circuit Society from 2005 to 2007.