Nanoscale Bipolar and Complementary Resistive Switching Memory Based on Amorphous Carbon

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***Abstract*—There has been a strong demand for developing an ultradense and low-power nonvolatile memory technology. In this paper, we present a carbon-based resistive random access memory device with a carbon nanotube (CNT) electrode. An amorphous carbon layer is sandwiched between the fast-diffusing top metal electrode and the bottom CNT electrode, exhibiting a bipolar switching behavior. The use of the CNT electrode can substantially reduce the size of the active device area. We also demonstrate a carbon-based complementary resistive switch (CRS) consisting of two back-to-back connected memory cells, providing a route to reduce the sneak current in the cross-point memory. The bit information of the CRS cell is stored in a high-resistance state, thus reducing the power consumption of the CRS memory cell. This paper provides valuable early data on the effect of electrode size scaling down to nanometer size.**

***Index Terms*—Amorphous carbon (a-C), carbon nanotube (CNT), complementary resistive switching, nonvolatile memory, resistive random access memory (RRAM), resistive switching memory.**

I. Introduction

BECAUSE OF the drive toward smaller, faster, and denser nanoelectronics systems, the feature size of the nonvolatile memory continues to scale down toward nanometer size. The conventional Si-based Flash memory is expected to run into its physical limits in the near future [1]. Technology breakthroughs in materials and device concepts are required for next-generation nonvolatile memory. The two-terminal resistive switching memory, where two metal electrodes are separated by a functional insulator, offers the potential for high scalability and ease of integration with current complementary metal–oxide–semiconductor technology. To increase the density of the resistive memory, the cross-point architecture, where a bistable material is sandwiched between the parallel bottom electrodes and the orthogonal top electrodes, has been proposed because the memory cell size can be reduced to $4F^2$ ($F =$ minimize feature size) and potentially even smaller if the memory cells are stacked in three dimensions [2], [3]. The switching material can be electrically triggered between two resistance states. This resistive switching behavior has been observed in a variety of solid insulating and semiconducting materials, including transition metal oxides (e.g., NiO, TiO_2, HfO_2, ZnO, and Al_2O_3) [4]–[7], ferroelectric (e.g., $PbZr_{0.52}Ti_{0.48}O_3$) [8], ferromagnetic (e.g., MgO) [9], perovskite (e.g., $SrZrO_3$) [10], chalcogenides (e.g., GeSbTe) [11], organics (e.g., Alq_3) [12], amorphous silicon (a-Si) [13]–[15], and Si/a-Si core/shell nanowires [16].

Carbon-based materials, including amorphous carbon (a-C) [17]–[26], fullerene [27], graphene oxide [28], [29], carbon/organic composite [30], and carbon nanotube (CNT) [31], have been shown to exhibit resistive switching behavior for nonvolatile memory application. Amorphous carbon is a noncrystalline carbon allotrope in which a long-range crystalline order is not present. Different switching mechanisms for a-C have been proposed to explain the resistive change behavior, including thermochemical sp^2 carbon chain forming/rupture [17], [18], electrochemical metallization [19]–[21], and valence change [22], [23].

To achieve ultrahigh-density cross-point memory, it is necessary to scale down the metal electrodes to nanometer size. However, the fabrication of the nanometer feature size (e.g., 1–2 nm) is still challenging for current lithography technologies. At the nanoscale, carrier scattering at the surface leads to a dramatic increase in metal resistivity. This requires researchers to find a way for fabricating nanometer electrodes beyond the limitation of current lithography length scales, and yet maintain the good electrical conductivity at such a small scale. A metallic single-walled CNT, another allotrope in the carbon family, has a nanometer diameter (1–2 nm in this paper), excellent electrical conductivity, and a high current-carrying capacity [32], and it has been used as a nanoscale electrode for resistive switching memory with chalcogenide [33], [34] AgTCNQ [35] and silicon oxide [36], [37]. This bottom-up approach using CNT as the electrode is a promising solution for scaling down the memory device to the nanometer size. The memory device with CNT electrode also enables us to study the resistive switching mechanism of the conduction filament below 5 nm. In this paper, we demonstrate nonvolatile resistive switching for an a-C

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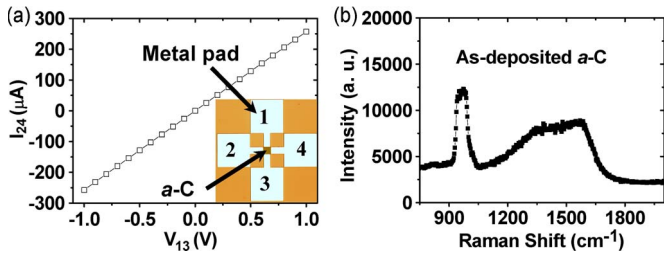

Fig. 1. Characterization of the as-deposited 30-nm-thick a-C film by e-beam evaporation. (a) I–V curve of the a-C film measured by a four-point method. (Inset) Photograph of the four-point measurement structure. (b) Raman spectroscopy of the a-C film, showing a broad peak distribution from 1200 to 1700 cm^{-1}. The strong peak around 1000 cm^{-1} is the second-order effect from the Si substrate.

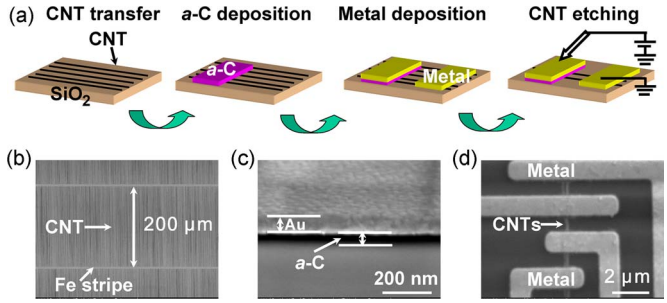

Fig. 2. Fabrication of the metal/a-C/CNT/metal memory device. (a) Process flow for fabricating the memory structure. (b) SEM image of the horizontally aligned CNTs with 200-μm length. (c) Cross-sectional SEM image of the carbon memory cell, showing the metal electrode on top of the a-C layer. (d) Top-view SEM image of the carbon memory cell, showing that the CNT acts as the bottom electrode of the memory cell.

layer sandwiched between the top metal electrode and the bottom CNTs. The single-walled CNT, with an average diameter of 1.2 nm, is an ideal nanoscale electrode for ultradense memory cells. We also demonstrate a complementary resistive switch (CRS) [2] for a planar metal/a-C/CNT/a-C/metal device for the first time. This CRS device potentially enables a large passive crossbar array, with the CRS itself serving as an integrated array cell selection device.

II. Fabrication of the Test Structure

The chemical bonding of carbon element has sp^1, sp^2, and sp^3 hybridization configurations. The a-C contains a mixture of sp^3, sp^2 and sometimes a small fraction of sp^1 sites, and some hydrogen [38]. The sp^2 bonding-dominated graphitic carbon has low resistivity close to that of a metal, whereas the sp^3 bonding-dominated diamond-like carbon is an insulator with high resistivity. In this paper, we deposited a-C by an electron-beam (e-beam) evaporation technique. A 30-nm-thick a-C was deposited at the pressure of 10^{-5} torr. The experimental details are described in the Appendix. To accurately determine the resistivity of the as-deposited a-C film, we used a four-point electrical test structure [see inset in Fig. 1(a)]. Fig. 1(a) shows a typical current–voltage (I–V) curve measured from a 30-nm-thick a-C by e-beam evaporation. The resistivity ($121.7 \pm 75.7\ \Omega \cdot \mu$m) of the 30-nm-thick a-C is in the same order with the previous report of a-C by e-beam evaporation and filtered cathodic vacuum arc [22], [39]. Fig. 1(b) shows the Raman spectra of the as-deposited a-C by e-beam evaporation. The G peak is centered around 1572 cm^{-1}. According to the three-stage model by Ferrari and Robertson [40], the G peak position locates in the range between nanocrystalline graphite and a-C. The broad peak distribution from 1200 to 1700 cm^{-1} indicates the amorphous structure of the carbon film.

Fig. 2(a) shows the process flow for fabricating the metal/a-C/CNT/metal memory device. Horizontally aligned CNTs were grown on ST-cut single-crystal quartz wafers using Fe catalyst and CH_4 as the carbon source. The detailed CNT synthesis process has been described elsewhere [41]. Fig. 2(b) shows a scanning electron microscope (SEM) image of the horizontally aligned CNTs. The average CNT density is $\sim$2 CNT/μm with the number of the CNTs for the typical device with 1-μm width varying from 1–3. The length of the CNT is 200 μm in this paper, making the use of CNT for long bit and word lines possible. Earlier work showed the aligned CNT can be $\sim$1 mm long [41]. The horizontally aligned CNTs were then transferred to a Si/SiO_2 substrate using a 100-nm-thick Au film and a thermal release adhesive tape [41]. The a-C pattern was defined by a standard photolithography process. A 30-nm-thick a-C layer was deposited on top of the transferred CNT by e-beam evaporation, followed by a liftoff process. The top metal electrodes were patterned by a second e-beam evaporation process and liftoff. In this paper, we used a fast-diffusing metal, e.g., Ag or Au. Thus, the a-C layer was sandwiched between the top metal electrode and the bottom CNTs. Fig. 2(c) shows a cross-sectional SEM image of the a-C memory cell. The unwanted CNTs were etched away by the oxygen plasma, leaving the CNT only in the active region. Fig. 2(d) shows a top-view SEM image of one memory cell. The CNTs act as the bottom electrode in the memory cell, and they are orthogonal to the top metal electrode.

III. Results

The capping metal on top of a-C plays an important role in determining the switching behavior. Unipolar switching has been reported for the a-C layer with an inert metal electrode such as W and Cr [17], [18]. The unipolar switching mechanism of a-C has been explained as the formation/rupture of the sp^2 carbon chain in the sp^3 carbon matrix, in which carbon is the monoatom for both the conductive filament and the insulating matrix. Devices with a fast-diffusing metal such as Cu, Ag, and Au on top of a-C have been reported to exhibit the bipolar resistive switching behavior [19]–[21]. The bipolar resistive switching behavior is the result of electrochemical metallization of the conductive filaments, similar to the conductive-bridge resistive memory [13]–[15], [19]–[21]. Bipolar switching is more controllable than unipolar switching as the SET and the RESET processes occur at opposite voltage polarities. In this paper, we used a fast-diffusing metal (Ag or Au) as the top metal electrode and CNTs as the nanoscale bottom electrode. DC voltage sweeps were applied at the top metal electrode with the bottom CNT electrode grounded [see Fig. 2(a)]. The initial state of the memory device exhibits the high-resistance state (HRS) around 5 MΩ. A positive dc sweep was used to switch the memory cell to the low-resistance state (LRS). The dc

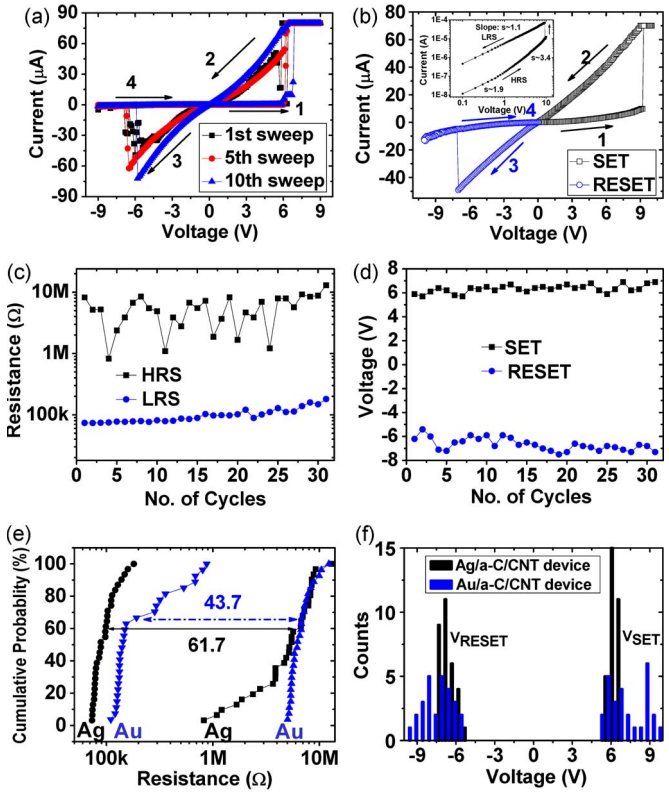

Fig. 3. Electrical characterization of the carbon-based bipolar memory. (a) I–V curves of a Ag/a-C/CNT/Ag memory cell. The dc sweep was performed from $0 \rightarrow 9$ V $\rightarrow 0 \rightarrow -9$ V $\rightarrow 0$. The current compliance is 80 μA. (b) I–V curve of a Au/a-C/CNT/Au memory cell. The dc sweep was performed from $0 \rightarrow 10$ V $\rightarrow 0 \rightarrow -10$ V $\rightarrow 0$. The current compliance is 70 μA. Inset of (b) shows the I–V curve of the Au/a-C/CNT/Au memory cell in the log–log scale. Evolution of (c) HRS/LRS, where the resistance state is read at 1 V, and (d) $V_{\rm SET}/V_{\rm RESET}$ of a Ag/a-C/CNT/Ag cell. Statistical distribution of (e) HRS/LRS and (f) $V_{\rm SET}/V_{\rm RESET}$ of Ag/a-C/CNT/Ag and Au/a-C/CNT/Au cells during endurance testing.

voltage was swept in the sequence of $0 \rightarrow V \rightarrow 0 \rightarrow -V \rightarrow 0$ with current compliance below 100 μA. Fig. 3(a) shows the first, fifth, and tenth sweeps of a Ag/a-C/CNT/Ag cell. SET switching was swept with current compliance (80 μA in this curve) to prevent the device from suffering permanent breakdown. The resistance state of the memory cell was switched from HRS to LRS about 6.2 V and switched back to HRS only by applying a negative dc voltage, exhibiting the typical bipolar switching behavior. The resistance OFF/ON ratio at 5 V is around 80. The Au/a-C/CNT/Au device [see Fig. 3(b)] shows similar resistive switching behaviors to the Ag/a-C/CNT/Ag device. Inset in Fig. 3(b) shows the log–log scale I–V curve of the memory cell. The current–voltage relationship indicates the different conduction mechanisms in HRS and LRS. In our device configuration, the bottom CNT electrode is chemically inert. No atomic migration will happen in the CNT in the normal device operation region due to the high current-carrying capacity ($> 10^9$ A/cm^2) of the CNT [32]. Resistive switching is most likely to be caused by the precipitates from the top diffusing metal electrode to the a-C matrix [19]–[21]. The I–V curve of the LRS of a Au/a-C/CNT/Au cell shows an ohmic-like behavior with a slope of 1.1. This is believed to be from the formation of a Au or Ag conduction filament during the SET process [19]–[21]. The charge transport in HRS is in agreement

TABLE I
PARAMETERS OF THE CARBON-BASED MEMORY CELLS WITH DIFFERENT ACTIVE DEVICE AREAS

	This work	Choi'09		Zhuge'10
Device	Ag/*a*-C/CNT	Pt/Cu-C/Pt		Cu/*a*-C/Pt
C deposition	e-beam	sputtering		ion-beam
Area (μm^2)	**0.001**	**0.01**	**25**	**10^4**
Reset I (μA)	40-75	206.4	6985	~12000
Reset V (V)	5.4-7.5	1.1	N/A	0.8-1.2
ON/OFF	40-200	~100	~2.24	>100
Retention	>10^6 s	N/A	N/A	>10^5 s

with a trap-controlled space-charge-limited current mechanism [19], [22]. The ON and OFF states of the memory cells retained for at least two weeks at room temperature in air. No electrical power was needed to maintain the resistance states, indicating the nonvolatile property of the memory cell.

The use of the nanoscale CNT electrode enables us to study the effect of the scaling of the active area on power consumption. The active area of the memory device can be estimated by the width of the top metal electrode and the diameter of the bottom CNT, around 1 μm $\times$ 0.001 μm $=$ 0.001 μm^2. Table I documents the comparisons of major memory parameters between our devices and the other a-C-based memory cells [19]–[21]. Although the memory devices were fabricated by different processes (different carbon deposition methods and different top metal electrodes), all of them exhibit a similar bipolar switching behavior. We listed the parameters of the devices with different active areas in Table I. The RESET current is defined as the maximum current that is attained before an abrupt decrease in resistance. The dramatic decrease in the RESET current is noticeably observed when the active device area is reduced, whereas the resistance ON/OFF ratio and the retention time of our nanoscale device remain comparable to those of the larger device. These results suggest that the downward scaling of the active device area can reduce the RESET current of the a-C-based memory device [19]–[21]. The reduction of the active device area using the CNT electrode confines the conduction filament more locally and reduces the RESET current.

The cycling measurements were repeated by the dc sweep. Fig. 3(c) shows the resistance evolution of HRS and LRS of a Ag/a-C/CNT/Ag device during the dc sweep cycling. Resistance switching is reproducible, and the memory cell successfully operates over 31 times. Fig. 3(d) shows the evolution of $V_{\rm SET}$ and $V_{\rm RESET}$ during endurance testing. The $V_{\rm SET}$ and $V_{\rm RESET}$ of Ag/a-C/CNT/Ag are higher than those of the metal/a-C/metal structure [19]–[21], probably related to the bottom CNT/metal contact. The contact area at the nanoscale electrode is very small, resulting in current crowding. The actual contact resistance of CNT is much larger than the ideal quantum resistance limit. There is a large voltage drop at the interface between CNT and surrounding materials (CNT/metal and CNT/a-C). Fig. 3(e) and (f) shows the statistical distribution of the HRS/LRS resistance and the SET/RESET voltage for Ag/a-C/CNT/Ag and Au/a-C/CNT/Au memory cells during endurance

testing. In LRS, the overall resistance of the cell is hundreds of kiloohms, close to that of the CNT device directly contacted with metal. In HRS, the presence of some sp^3 carbon results in the overall resistance of the cell on the order of megaohms. Both the HRS and LRS resistance values of the memory cells show a large variation during endurance testing. Our results are in contrast to the better uniformity for a nanoscale memory device (electrode diameter $\Phi = 50$ nm) [42]. This difference possibly results from the effect of further electrode downscaling. For a large memory device, (e.g., $\Phi > 1$ μm), the conductive filaments' formation process is determined by the competition among many possible filamentary paths [19], resulting in a large variation of the resistance states during endurance testing [42]. For a nanoscale device, (e.g., $\Phi = 50$ nm) [42], the conduction filament is confined in a nanoscale location. Limited possible filamentary paths are competitive for the formation of the filament. As a result, the nanoscale memory device during endurance testing exhibits better uniformity. For our nanoscale memory device, (the average diameter of the CNT electrode is $\sim$1.2 nm), the CNT electrode is comparable to or even smaller than the size of the conductive filament. In the ON state, the small contact area between the bottom CNT and the conductive filament makes electrical coupling extremely difficult. The dominant factor becomes the interface between the nanometer electrode and the conduction filament instead of the formation of different filamentary conduction paths. In each switching cycle, the contact configuration at nanoscale is quite different in the small contact area. It is reasonable to expect the resistance states and $V_{\rm SET}/V_{\rm RESET}$ to have a large variation in our nanometer memory device.

We have successfully demonstrated the nanoscale resistive memory based on the structure of metal/a-C/CNT/metal. To further increase the density of the memory, cross-point memory is preferred. The sneak leakage current is an inherent disadvantage of cross-point memory [2]. A selection diode integrated with the memory cell is often proposed to solve the sneak current path problem [3]. Recently, CRSs have been proposed for solving the sneak leakage current in cross-point memory, in which two bipolar resistive memory cells are connected back to back [2]. In our structure, the two series memory cells were simultaneously fabricated, alleviating the impact from fabricating the top cell on the bottom cell. We fabricated the carbon-based lateral CRS structure with two bipolar metal/a-C/CNT/metal cells connected back to back by a common CNT as a metal/a-C/CNT/a-C/metal device. The fabrication process has been schematically described in Fig. 4(a). The difference between the metal/a-C/CNT/metal memory and metal/a-C/CNT/a-C/metal memory devices lies in the pattern of the a-C layer. For the metal/a-C/CNT/metal memory device, a-C only deposited on top of one end of the CNT; for the metal/a-C/CNT/a-C/metal device, both ends of the CNT are contacted with a-C/metal.

Inset in Fig. 4(b) shows the resistance measurement of a Ag/a-C/CNT/a-C/Ag cell during the initialization process. The as-fabricated two memory cells are both at HRS initially. This HRS/HRS in CRS only exists in the pristine device. When a positive voltage sweep is applied to the CRS cell, one (cell 1) of the two memory cells is triggered to LRS. The decreasing

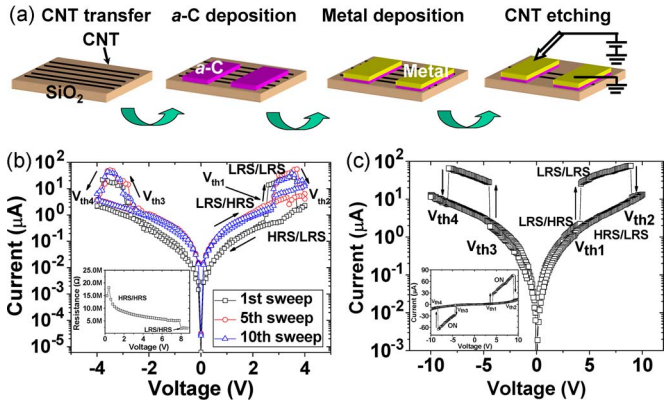

Fig. 4. I–V curves of the CRS memory cell. (a) Schematic of the process flow for fabricating the metal/a-C/CNT/a-C/metal CRS cell. (b) I–V curves of a Ag/a-C/CNT/a-C/Ag CRS cell. The dc sweep was performed from 0 $\rightarrow$ 4 V $\rightarrow$ 0 $\rightarrow$ -4 V $\rightarrow$ 0. Inset of (b) shows the resistance measurement of the initialization process of the CRS cell. The resistance state of the CRS cell is converted from initial HRS/HRS to LRS/HRS. (c) Semilog I–V curve of a Au/a-C/CNT/a-C/Au CRS cell. The dc sweep was performed from 0 $\rightarrow$ 10 V $\rightarrow$ 0 $\rightarrow$ -10 V $\rightarrow$ 0. Inset of (c) shows the linear scale I–V curve of the Au/a-C/CNT/a-C/Au cell.

resistance is observed in the inset in Fig. 4(b). Because the polarity of the SET voltage in the other cell (cell 2) is opposite, it remains in the HRS and acts as a voltage divider. When we continue to sweep the voltage from zero to $-V_{\rm th3}$ (beyond the SET voltage of cell 2), both cells are in LRS. When the negative voltage is increased to $-V_{\rm th4}$, cell 1 is RESET to its HRS. Fig. 4(b) shows the typical I–V curves of a Ag/a-C/CNT/a-C/Ag CRS cell, which is a superimposed I–V characteristic of the two bipolar memory cells connected back to back. The four distinct threshold voltages enable us to define the CRS cell with four different states [i.e., "ON" (LRS/LRS), "OFF" (HRS/HRS), "0" (LRS/HRS), and "1" (HRS/LRS)] [2]. The bit information is stored in the two back-to-back memory cells, whereas the overall resistance of the CRS remains dominated by the HRS, i.e., $R_{\rm HRS}$. The CRS cell exhibits overall high resistance when storing the bit information, thus effectively reducing the sneak current to the unselected cell. The use of two distinct HRSs to store the bit information also reduces static power consumption [2], while at the same time, this scheme is subject to read/write noise margin constraints [43]. The Ag/a-C/CNT/a-C/Ag CRS cell in Fig. 4(b) shows poor endurance performance. The cell failed only after 11 cycles. In addition to the reasons similar to the Ag/a-C/CNT/Ag cell, the poor endurance of the cell is also related to the CRS structure itself. The two cells in the CRS structure are not identical due to device variations. The undesired RESET process may happen in one cell before the desired SET in the other cell. Fig. 4(c) shows the I–V curve from a Au/a-C/CNT/a-C/Au cell. It is found to have a larger ON/OFF ratio and a larger switching voltage than those of the Ag/a-C/CNT/a-C/Ag cell. This indicates that the top metal electrode plays an important role on the performance of the memory cell.

IV. Conclusion

In summary, we have successfully demonstrated a new carbon-based resistive random access memory device. The use

of the CNT as an electrode leads to the ultimately scaled cross-point area. The operation current is greatly reduced, providing the advantages, which lead themselves to a low-power device. We have also shown a carbon-based CRS memory cell for the first time. This new structure has the potential for use in dense cross-point memory without the cell selection devices.

APPENDIX

The resistivity of carbon film is closely related to the deposition process. In this paper, we used an Edwards EB3 electron beam evaporator, and we used a graphite target as a carbon source. We conduct the deposition process at the pressure of 10^{-5} torr. The graphite has a very high melting point. To make sure that the carbon is evaporated, we used the beam current 80–100 mA at the voltage of 5.6 kV. The through distance between the target and the substrate is short ($\sim$30 cm). The strong radiation from the carbon target heats the substrate. In this paper, the deposition process is actually not a room-temperature process. The thermal couple close to the sample holder displays over 135 °C. The actual substrate temperature is even higher than this value. Deposition of a 30-nm-thick carbon film takes 12–15 min. This process at elevated temperature is similar to an *in situ* anneal, it and helps reduce the resistivity of carbon film [38].

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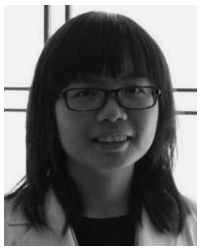

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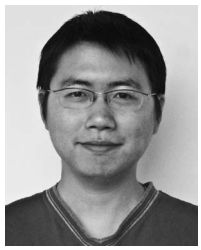

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