10. A. Schirotzek, C.-H. Wu, A. Sommer, M. W. Zwierlein, *Phys. Rev. Lett.* **102**, 230402 (2009).
11. S. Nascimbène *et al.*, *Phys. Rev. Lett.* **103**, 170402 (2009).
12. C. Kohstall *et al.*, *Nature* **485**, 615–618 (2012).
13. M. Koschorreck *et al.*, *Nature* **485**, 619–622 (2012).
14. Y. Zhang, W. Ong, I. Arakelyan, J. E. Thomas, *Phys. Rev. Lett.* **108**, 235302 (2012).
15. P. Massignan, M. Zaccanti, G. M. Bruun, *Rep. Prog. Phys.* **77**, 034401 (2014).
16. M. Sidler *et al.*, http://arXiv.org/abs/1603.09215 (2016).
17. J. Goold, T. Fogarty, N. Lo Gullo, M. Paternostro, T. Busch, *Phys. Rev. A* **84**, 063632 (2011).
18. M. Knap *et al.*, *Phys. Rev. X* **2**, 041020 (2012).
19. M. Cetina *et al.*, *Phys. Rev. Lett.* **115**, 135302 (2015).
20. See supplementary materials on *Science* Online.
21. D. Naik *et al.*, *Eur. Phys. J. D* **65**, 55–65 (2011).
22. J. Loschmidt, *Sitzungsber. Akad. Wissenschaften Wien* **73**, 128 (1876).
23. E. L. Hahn, *Phys. Rev.* **80**, 580–594 (1950).
24. P. Nozières, C. T. De Dominicis, *Phys. Rev.* **178**, 1097–1107 (1969).
25. R. A. Jalabert, H. M. Pastawski, *Adv. Solid State Phys.* **41**, 483–496 (2001).
26. F. Chevy, *Phys. Rev. A* **74**, 063628 (2006).
27. X. Cui, H. Zhai, *Phys. Rev. A* **81**, 041602 (2010).
28. J. Dubois *et al.*, *Nature* **502**, 659–663 (2013).
29. C. Mora, F. Chevy, *Phys. Rev. Lett.* **104**, 230402 (2010).
30. Z. Yu, S. Zöllner, C. J. Pethick, *Phys. Rev. Lett.* **105**, 188901 (2010).
31. W. Zwerger, Ed., *The BCS-BEC Crossover and the Unitary Fermi Gas* (Springer, 2012).
32. R. A. Hart *et al.*, *Nature* **519**, 211–214 (2015).
33. L. J. LeBlanc, J. H. Thywissen, *Phys. Rev. A* **75**, 053612 (2007).

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SUPPLEMENTARY MATERIALS

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DEVICE TECHNOLOGY

MoS_2 transistors with 1-nanometer gate lengths

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Scaling of silicon (Si) transistors is predicted to fail below 5-nanometer (nm) gate lengths because of severe short channel effects. As an alternative to Si, certain layered semiconductors are attractive for their atomically uniform thickness down to a monolayer, lower dielectric constants, larger band gaps, and heavier carrier effective mass. Here, we demonstrate molybdenum disulfide (MoS_2) transistors with a 1-nm physical gate length using a single-walled carbon nanotube as the gate electrode. These ultrashort devices exhibit excellent switching characteristics with near ideal subthreshold swing of ~65 millivolts per decade and an On/Off current ratio of ~10^6. Simulations show an effective channel length of ~3.9 nm in the Off state and ~1 nm in the On state.

As Si transistors rapidly approach their projected scaling limit of ~5-nm gate lengths, exploration of new channel materials and device architectures is of utmost interest (*1*–*3*). This scaling limit arises from short channel effects (*4*). Direct source-to-drain tunneling and the loss of gate electrostatic control on the channel severely degrade the Off state leakage currents, thus limiting the scaling of Si transistors (*5*, *6*). Certain semiconductor properties dictate the magnitude of these effects for a given gate length. Heavier carrier effective mass, larger band gap, and lower in-plane dielectric constant yield lower direct source-to-drain tunneling currents (*7*). Uniform and atomically thin semiconductors with low in-plane dielectric constants are desirable for enhanced electrostatic control of the gate. Thus, investigation and introduction of semiconductors that have more ideal properties than Si could lead to further scaling of transistor dimensions with lower Off state dissipation power.

Transition metal dichalcogenides (TMDs) are layered two-dimensional (2D) semiconductors that have been widely explored as a potential channel material replacement for Si (*8*–*11*), and each material exhibits different band structures and properties (*12*–*16*). The layered nature of TMDs allows uniform thickness control with atomic-level precision down to the monolayer limit. This thickness scaling feature of TMDs is highly desirable for well-controlled electrostatics in ultrashort transistors (*3*). For example, monolayer and few-layer MoS_2 have been shown theoretically to be superior to Si at the sub-5-nm scaling limit (*17*, *18*).

The scaling characteristics of MoS_2 and Si transistors as a function of channel thickness and gate length are summarized in Fig. 1. We calculated direct source-to-drain tunneling currents ($I_{SD\text{-}LEAK}$) in the Off state for different channel lengths and thicknesses using a dual-gate device structure (fig. S1) as a means to compare the two materials. MoS_2 shows more than two orders of magnitude reduction in $I_{SD\text{-}LEAK}$ relative to Si mainly because of its larger electron effective mass along the transport direction ($m_n^* \sim 0.55m_0$ for MoS_2 versus $m_n^* \sim 0.19m_0$ for Si [100]) (*19*), with a trade-off resulting in lower ballistic On current. Notably, $I_{SD\text{-}LEAK}$ does not limit the scaling of monolayer MoS_2 even down to the ~1-nm gate length, presenting a major advantage over Si [see more details about calculations in the supplementary materials (*20*)]. Finally, few-layer MoS_2 exhibits a lower in-plane dielectric constant (~4) compared with bulk Si (~11.7), Ge (~16.2), and GaAs (~12.9), resulting in a shorter electrostatic characteristic length (λ) as depicted in fig. S2 (*21*).

The above qualities collectively make MoS_2 a strong candidate for the channel material of future transistors at the sub-5-nm scaling limit. However, to date, TMD transistors at such small gate lengths have not been experimentally explored. Here, we demonstrate 1D gated, 2D semiconductor field-effect transistors (1D2D-FETs) with a single-walled carbon nanotube (SWCNT) gate, a MoS_2 channel, and physical gate lengths of ~1 nm. The 1D2D-FETs exhibit near ideal switching characteristics, including a subthreshold swing (SS) of ~65 mV per decade at room temperature and high On/Off current ratios. The SWCNT diameter $d \sim 1$ nm for the gate electrode (*22*) minimized parasitic gate to source-drain capacitance, which is characteristic of lithographically patterned tall gate structures. The ~1-nm gate length of the SWCNT also allowed for the experimental exploration of the device physics and properties of MoS_2 transistors as a function of semiconductor thickness (i.e., number of layers) at the ultimate gate-length scaling limit.

The experimental device structure of the 1D2D-FET (Fig. 2A) consists of a MoS_2 channel (number of layers vary), a ZrO_2 gate dielectric, and a SWCNT gate on a 50-nm SiO_2/Si substrate with a physical gate length ($L_G \sim d$) of ~1 nm. Long, aligned SWCNTs grown by chemical vapor deposition

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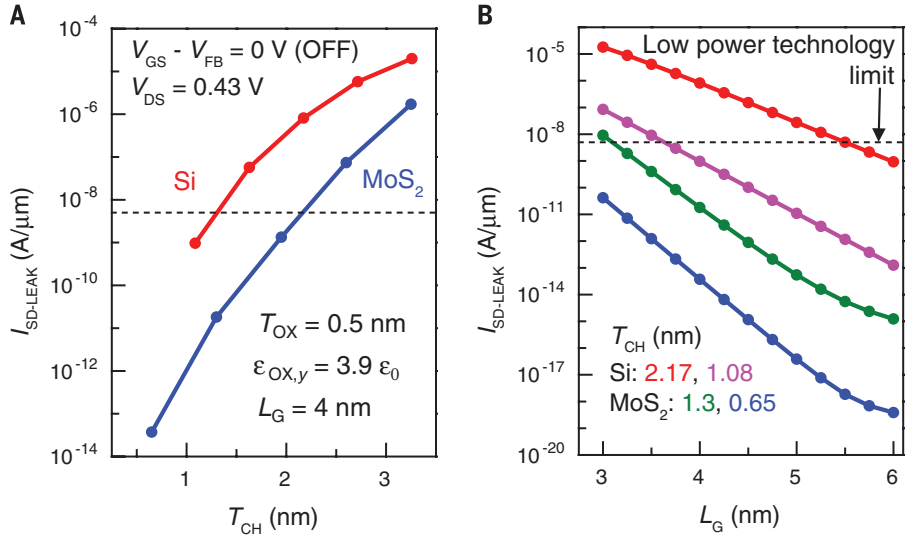

Fig. 1. Direct source-to-drain tunneling leakage current. (**A**) Normalized direct source-to-drain tunneling leakage current ($I_{SD-LEAK}$), calculated using the WKB (Wentzel-Kramers-Brillouin) approximation as a function of channel thickness T_{CH} for Si and MoS_2 in the Off state. $V_{DS} = V_{DD} = 0.43$ V from the International Technology Roadmap for Semiconductors (ITRS) 2026 technology node. (**B**) $I_{SD-LEAK}$ as a function of gate length L_G for different thicknesses of Si and MoS_2 for the same Off state conditions as Fig. 1A. The dotted line in Fig. 1, A and B represents the low operating power limit for the 2026 technology node as specified by the ITRS.

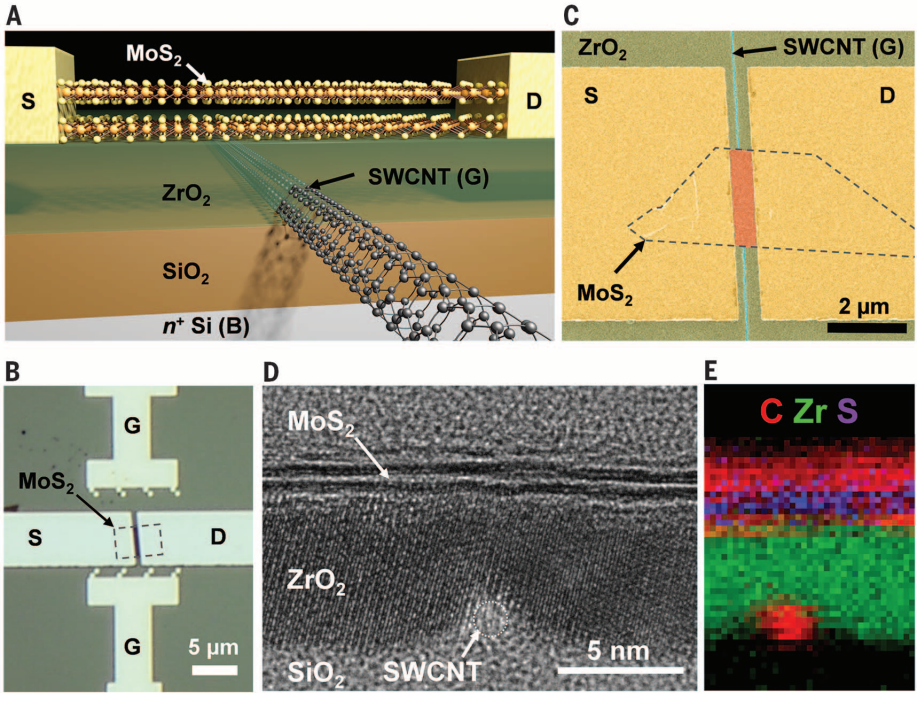

Fig. 2. 1D2D-FET device structure and characterization. (**A**) Schematic of 1D2D-FET with a MoS_2 channel and SWCNT gate. (**B**) Optical image of a representative device shows the MoS_2 flake, gate (G), source (S), and drain (D) electrodes. (**C**) False-colored SEM image of the device showing the SWCNT (blue), ZrO_2 gate dielectric (green), MoS_2 channel (orange), and the Ni source and drain electrodes (yellow). (**D**) Cross-sectional TEM image of a representative sample showing the SWCNT gate, ZrO_2 gate dielectric, and bilayer MoS_2 channel. (**E**) EELS map showing spatial distribution of carbon, zirconium, and sulfur in the device region, confirming the location of the SWCNT, MoS_2 flake, and ZrO_2 dielectric.

were transferred onto a n^+ Si/SiO_2 substrate (50-nm-thick SiO_2) (*23*), located with a scanning electron microscope (SEM), and contacted with palladium via lithography and metallization. These steps were followed by atomic layer deposition (ALD) of ZrO_2 and pick-and-place dry transfer of MoS_2 onto the SWCNT covered by ZrO_2 (*14*). Nickel source and drain contacts were made to MoS_2 to complete the device. The detailed process flow and discussion about device fabrication is provided in fig. S3.

Figure 2B shows the optical image of a representative 1D2D-FET capturing the MoS_2 flake, the source and drain contacts to MoS_2, and the gate contacts to the SWCNT. The SWCNT and the MoS_2 flake can be identified in the false-colored SEM image of a representative sample (Fig. 2C). The 1D2D-FET consists of four electrical terminals; source (S), drain (D), SWCNT gate (G), and the n^+ Si substrate back gate (B). The SWCNT gate underlaps the S/D contacts. These underlapped regions were electrostatically doped by the Si back gate during the electrical measurements, thereby serving as n^+ extension contact regions. The device effectively operated like a junctionless transistor (*24*), where the SWCNT gate locally depleted the n^+ MoS_2 channel after applying a negative voltage, thus turning Off the device.

A cross-sectional transmission electron microscope (TEM) image of a representative 1D2D-FET (Fig. 2D) shows the SWCNT gate, ZrO_2 gate dielectric (thickness T_{OX}~5.8 nm), and the bilayer MoS_2 channel. The topography of ZrO_2 surrounding the SWCNT and the MoS_2 flake on top of the gate oxide was flat, as seen in the TEM image. This geometry is consistent with ALD nucleation initiating on the SiO_2 substrate surrounding the SWCNT and eventually covering it completely as the thickness of deposited ZrO_2 exceeds the SWCNT diameter d (*25*). The spatial distribution of carbon, zirconium, and sulfur was observed in the electron energy-loss spectroscopy (EELS) map of the device region (Fig. 2E), thus confirming the location of the SWCNT, ZrO_2, and MoS_2 in the device (fig. S4) (*20*).

The electrical characteristics for a 1D2D-FET with a bilayer MoS_2 channel (Fig. 3) show that the MoS_2 extension regions (the underlapped regions between the SWCNT gate and S/D contacts) could be heavily inverted (i.e., n^+ state) by applying a positive back-gate voltage of $V_{BS} = 5$ V to the Si substrate. The I_D-V_{BS} characteristics (fig. S5) indicate that the MoS_2 flake was strongly inverted by the back gate at $V_{BS} = 5$ V. The I_D-V_{GS} characteristics for the device at $V_{BS} = 5$ V and $V_{DS} =$ 50 mV and 1 V (Fig. 3A) demonstrate the ability of the ~1-nm SWCNT gate to deplete the MoS_2 channel and turn Off the device. The 1D2D-FET exhibited excellent subthreshold characteristics with a near ideal SS of ~65 mV per decade at room temperature and On/Off current ratio of ~10^6. The drain-induced barrier lowering (DIBL) was ~290 mV/V. Leakage currents through the SWCNT gate (I_G) and the n^+ Si back gate (I_B) are at the measurement noise level (Fig. 3A). The interface trap density (D_{IT}) of the ZrO_2-MoS_2 interface estimated from SS was ~1.7 × 10^{12} cm^{-2} eV^{-1},

which is typical for transferred MoS_2 flakes (*26*) because of the absence of surface dangling bonds (*20*).

Figure 3B shows the I_D-V_{DS} characteristics at different V_{GS} values and fixed V_{BS} = 5 V. The I_D-V_{GS} characteristics depended strongly on the value of V_{BS}, which affects the extension region resistance. The inversion of the extension regions increased with increasing V_{BS}, thus reducing the series resistance and contact resistance and led to an increase in the On current and an improvement in the SS. At more positive values of V_{BS}, V_{GS} had to be more negative in order to deplete the MoS_2 channel, which in turn made the threshold voltage (V_T) more negative. Above V_{BS} = 1 V, the SS and I_{On} did not improve any further, and the extension regions were strongly inverted (Fig. 3C). Thus, the 1D2D-FET operated as a short-channel device.

We performed detailed simulations using Sentaurus TCAD to understand the electrostatics of the 1D2D-FET. The Off and On state conditions correspond to (V_{GS}-V_T) of −0.3 V and 1.5 V, respectively (which give an On/Off current ratio of ~10^6). The electric field contour plot (Fig. 3D) in the Off state has a region of low electric field in the MoS_2 channel near the SWCNT, indicating that it is depleted. The reduced electron density in the MoS_2 channel (Fig. 3E), and the presence of an energy barrier to electrons in the conduction band (fig. S6A) are also consistent with the Off state of the device. The extension regions are still under inversion because of the positive back-gate voltage. The electron density of the MoS_2 channel in the depletion region can be used to define the effective channel length (L_{EFF}) of the 1D2D-FET, which is the region of channel controlled by the SWCNT gate (*27*–*29*). The channel is considered to be depleted if the electron density falls below a defined threshold ($n_{threshold}$). The Off state L_{EFF}, defined as the region of MoS_2 with electron density $n < n_{threshold}$ ($n_{threshold}$ = 1.3 × 10^5 cm^{-2}), for this simulated 1D2D-FET is L_{EFF} ~ 3.9 nm (Fig. 3E). L_{EFF} is dependent on V_{GS} and the value of $n_{threshold}$ (fig. S7).

As the device is turned Off, the fringing electric fields from the SWCNT (Fig. 3D) deplete farther regions of the MoS_2 channel and thus increase L_{EFF}. The short height of the naturally defined SWCNT gate prevents large fringing fields from controlling the channel and hence achieves a smaller L_{EFF} compared with lithographically patterned gates (fig. S8). The electric field and electron density contours for the device in the On state confirm the strong inversion of the channel region near the SWCNT (Fig. 3, F and G) with L_{EFF} ~ L_G = 1 nm. The energy bands in this case are flat in the entire channel region (fig. S6B), with the On state current being limited by the resistance of the extension regions and mainly the contacts. Doped S/D contacts along with shorter extension regions will result in increased On current.

The effect of T_{OX} scaling on short-channel effects like DIBL was also studied using simulations (fig. S9). The electrostatics of the device improves, and the influence of the drain on the channel reduces, as T_{OX} is scaled down to values

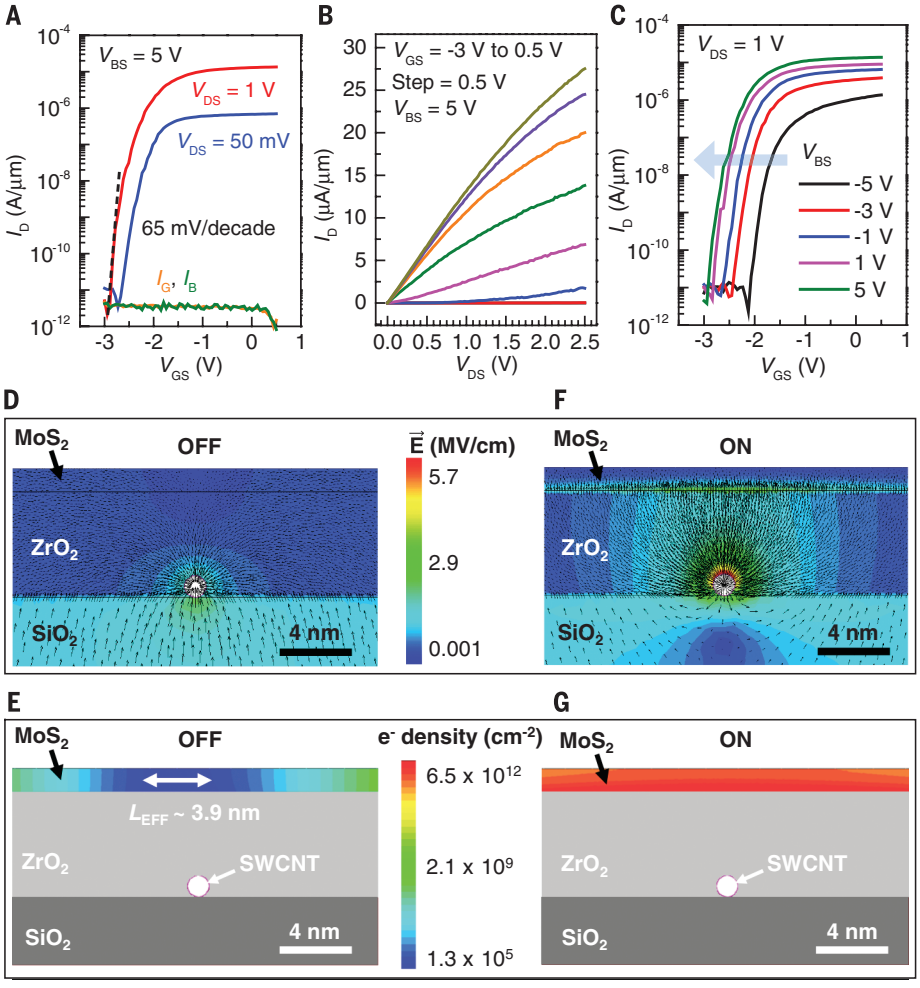

Fig. 3. Electrical characterization and TCAD simulations of 1D2D-FET. (**A**) I_D-V_{GS} characteristics of a bilayer MoS_2 channel SWCNT gated FET at V_{BS} = 5 V and V_{DS} = 50 mV and 1 V. The positive V_{BS} voltage electrostatically dopes the extension regions n^+. (**B**) I_D-V_{DS} characteristic for the device at V_{BS} = 5 V and varying V_{GS}. (**C**) I_D-V_{GS} characteristics at V_{DS} = 1 V and varying V_{BS} illustrating the effect of back-gate bias on the extension region resistance, SS, On current, and device characteristics. Electric field contour plots for a simulated bilayer MoS_2 device using TCAD in the (**D**) Off and (**F**) On state. Electron density plots for the simulated device using TCAD in the (**E**) Off and (**G**) On state. The electron density in the depletion region is used to define the L_{EFF}. L_{EFF} ~ d ~ L_G in the On state and L_{EFF} > L_G in the Off state because of the fringing electric fields from the SWCNT gate.

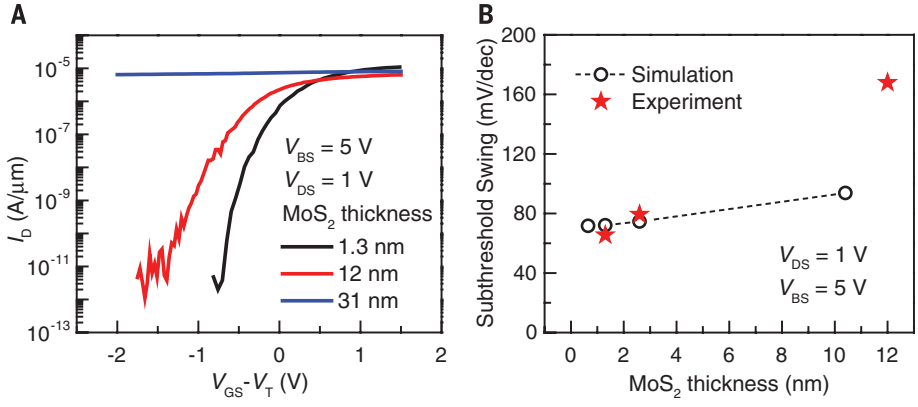

Fig. 4. MoS_2 thickness dependence. (**A**) Dependence of MoS_2 channel thickness on the performance of 1D2D-FET. SS increases with increasing MoS_2 channel thickness. (**B**) Extracted SS from experimental curves and TCAD simulations show increasing SS as channel thickness T_{CH} increases.

commensurate with L_G. This effect is seen by the strong dependence of DIBL on T_{OX}, thus demonstrating the need for T_{OX} scaling and high-κ (dielectric constant) 2D dielectrics to further enhance the device performance.

The effect of MoS_2 thickness on the device characteristics was systematically explored. At the scaling limit of the gate length, the semiconductor channel thickness must also be scaled down aggressively, as described earlier. The electrostatic control of the SWCNT gate on the MoS_2 channel decreased with increasing distance from the ZrO_2-MoS_2 interface. Thus, as the MoS_2 flake thickness was increased, the channel could not be completely depleted by applying a negative V_{GS}. Because of this effect, the SS for a 12-nm-thick MoS_2 device (~170 mV per decade) was much larger than that of bilayer MoS_2 (~65 mV per decade), and as the thickness of MoS_2 was increased to ~31 nm, the device could no longer be turned off (Fig. 4A). The experimental SS as a function of MoS_2 thickness was qualitatively consistent with the TCAD simulations (Fig. 4B and S10), showing an increasing trend with increasing channel thickness. The unwanted variations in device performance caused by channel thickness fluctuations (Fig. 4B and fig. S10), and the need for low Off state current at short channel lengths (Figs. 1 and 3), thus justify the need for layered semiconductors like TMDs at the scaling limit.

TMDs offer the ultimate scaling of thickness with atomic-level control, and the 1D2D-FET structure enables the study of their physics and electrostatics at short channel lengths by using the natural dimensions of a SWCNT, removing the need for any lithography or patterning processes that are challenging at these scale lengths. However, large-scale processing and manufacturing of TMD devices down to such small gate lengths are existing challenges requiring future innovations. For instance, research on developing process-stable, low-resistance ohmic contacts to TMDs, and scaling of the gate dielectric by using high-κ 2D insulators is essential to further enhance device performance. Wafer-scale growth of high-quality films (*30*) is another challenge toward achieving very-large-scale integration of TMDs in integrated circuits. Finally, fabrication of electrodes at such small scale lengths over large areas requires considerable advances in lithographic techniques. Nevertheless, the work here provides new insight into the ultimate scaling of gate lengths for a FET by surpassing the 5-nm limit (*3*–*7*) often associated with Si technology.

REFERENCES AND NOTES

1. T. N. Theis, P. M. Solomon, *Science* **327**, 1600–1601 (2010).
2. R. Chau, B. Doyle, S. Datta, J. Kavalieros, K. Zhang, *Nat. Mater.* **6**, 810–812 (2007).
3. A. D. Franklin, *Science* **349**, aab2750 (2015).
4. M. Lundstrom, *Science* **299**, 210–211 (2003).
5. M. Luisier, M. Lundstrom, D. A. Antoniadis, J. Bokor, in *Electron Devices Meeting (IEDM), 2011 IEEE International* (IEEE, 2011), pp. 11.12.11–1.12.14.
6. H. Kawaura, T. Sakamoto, T. Baba, *Appl. Phys. Lett.* **76**, 3810–3812 (2000).
7. W. S. Cho, K. Roy, *IEEE Electron Device Lett.* **36**, 427–429 (2015).
8. B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **6**, 147–150 (2011).
9. D. Sarkar *et al.*, *Nature* **526**, 91–95 (2015).
10. H. Liu, A. T. Neal, P. D. Ye, *ACS Nano* **6**, 8563–8569 (2012).
11. H. Wang *et al.*, *Nano Lett.* **12**, 4674–4680 (2012).
12. K. F. Mak, K. L. McGill, J. Park, P. L. McEuen, *Science* **344**, 1489–1492 (2014).
13. D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, M. C. Hersam, *ACS Nano* **8**, 1102–1120 (2014).
14. H. Fang *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **111**, 6198–6202 (2014).
15. K. S. Novoselov *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **102**, 10451–10453 (2005).
16. C.-H. Lee *et al.*, *Nat. Nanotechnol.* **9**, 676–681 (2014).
17. Y. Yoon, K. Ganapathi, S. Salahuddin, *Nano Lett.* **11**, 3768–3773 (2011).
18. L. Liu, Y. Lu, J. Guo, *IEEE Trans. Electron. Dev.* **60**, 4133–4139 (2013).
19. D. Wickramaratne, F. Zahid, R. K. Lake, *J. Chem. Phys.* **140**, 124710 (2014).
20. Supplementary materials are available on *Science* Online.
21. K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, Y. Arimoto, *IEEE Trans. Electron. Dev.* **40**, 2326–2329 (1993).
22. J. Svensson *et al.*, *Nanotechnology* **19**, 325201 (2008).
23. N. Patil *et al.*, *IEEE Trans. NanoTechnol.* **8**, 498–504 (2009).
24. J.-P. Colinge *et al.*, *Nat. Nanotechnol.* **5**, 225–229 (2010).
25. A. Javey *et al.*, *Nano Lett.* **4**, 1319–1322 (2004).
26. X. Zou *et al.*, *Adv. Mater.* **26**, 6255–6261 (2014).
27. Y. Taur, *IEEE Trans. Electron. Dev.* **47**, 160–170 (2000).
28. L. Barbut, F. Jazaeri, D. Bouvet, J.-M. Sallese, *Int. J. Microelectron. Comput. Sci.* **4**, 103–109 (2013).
29. S. Hong, K. Lee, *IEEE Trans. Electron. Dev.* **42**, 1461–1466 (1995).
30. K. Kang *et al.*, *Nature* **520**, 656–660 (2015).

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SUPPLEMENTARY MATERIALS

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BIOCATALYSIS

An artificial metalloenzyme with the kinetics of native enzymes

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Natural enzymes contain highly evolved active sites that lead to fast rates and high selectivities. Although artificial metalloenzymes have been developed that catalyze abiological transformations with high stereoselectivity, the activities of these artificial enzymes are much lower than those of natural enzymes. Here, we report a reconstituted artificial metalloenzyme containing an iridium porphyrin that exhibits kinetic parameters similar to those of natural enzymes. In particular, variants of the P450 enzyme CYP119 containing iridium in place of iron catalyze insertions of carbenes into C–H bonds with up to 98% enantiomeric excess, 35,000 turnovers, and 2550 hours^{-1} turnover frequency. This activity leads to intramolecular carbene insertions into unactivated C–H bonds and intermolecular carbene insertions into C–H bonds. These results lift the restrictions on merging chemical catalysis and biocatalysis to create highly active, productive, and selective metalloenzymes for abiological reactions.

The catalytic activity of a metalloenzyme is determined by both the primary coordination sphere of the metal and the surrounding protein scaffold. In some cases, laboratory evolution has been used to develop variants of native metalloenzymes for selective reactions of unnatural substrates (*1*, *2*). Yet with few exceptions (*3*), the classes of reactions that such enzymes undergo are limited to those of biological transformations. To combine the favorable qualities of enzymes with the diverse reactivity of synthetic transition-metal catalysts, abiological transition-metal centers or cofactors have been incorporated into native proteins. The resulting artificial metalloenzymes catalyze classes of reactions for which there is no known enzyme (abiological transformations) (*3*, *4*).

Although the reactivity of these artificial systems is new for an enzyme, the rates of these reactions have been much slower and the

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Supplementary Materials for

MoS_2 transistors with 1-nanometer gate lengths

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Materials and methods

(1) SWCNT growth on quartz: Aligned SWCNTs were grown according to a process similar to (*23*) modified to deliver a low aligned SWCNT density. 4" ST-cut quartz wafers were purchased from Hoffman Materials, Inc. then annealed at 900°C for 8.5 hours to repair the surface crystal. A ≈3.66 Å film of iron (99.95% pure) was evaporated using electron-beam evaporation onto 4μm wide stripes defined using photo-lithography at a rate of 0.33 Å/s. This was followed by metal liftoff and resist removal. The sample was grown in a 5" diameter FirstNano EasyTube 3000 CNT CVD furnace. The temperature was ramped to 610 °C in O_2 for calcination, then to 865 °C in 120 sccm H_2 at 315 Torr for reduction of the iron catalyst. After stabilizing temperature for 10 minutes, 1 SLM of CH_4 was introduced to the chamber to begin growth. After one hour, the sample was cooled in H_2 ambient. The SWCNT density as measured by SEM was 1 SWCNT per 15 μm across the wafer.

(2) SEM (scanning electron microscopy) imaging was performed using a Zeiss Gemini Ultra-55 field emission scanning electron microscope (FESEM). A ~ 1 kV accelerating voltage was used for imaging the devices and to register the locations of the SWCNTs with respect to pre-patterned lithography markers.

(3) AFM (atomic force microscopy) was performed using a Digital Instruments Nanoscope Dimension 3100 AFM. The AFM was done in the tapping mode using ~ 300 kHz resonance frequency, Budget sensors Tap300-G tapping mode tips.

(4) TEM (transmission electron microscopy) / STEM (scanning transmission electron microscopy): High resolution TEM/STEM imaging was performed using a probe-corrected JEM-ARM200F (JEOL USA, Inc.) operated at 200 kV. HAADF-STEM imaging was carried out with a 24 mrad convergence semi-angle electron beam and the collection angle for the ADF detector was set to 90-370 mrad.

(5) Elemental Mapping: Electron energy loss spectroscopy (EELS) and energy dispersive spectroscopy (EDS) mapping was performed with a Gatan Enfina spectrometer and X-MaxN 100TLE detector (Oxford Instruments), respectively. The collection angle for the EELS spectrum was set to be 31 mrad. The spatial resolution of the mapping is 0.27 nm/pixel and the collection time is 0.4 s/pixel.

(6) Electrical characterization: Electrical measurements were performed under vacuum (~ 10^{-5} mbar) in Lakeshore vacuum probe station using Agilent Technologies B1500A Semiconductor Device Analyzer.

Supplementary text

(1) Analytical 2D electrostatics model for Dual Gate Metal-Oxide-Semiconductor Field-Effect Transistor (DGMOS-FET) (*21*, *31*)

A symmetric DGMOS-FET structure is assumed as shown in Fig. S1. An analytical solution to the 2D Poisson equation is derived assuming a channel material with anisotropic dielectric constant using the approach taken in reference (*21*).

$$\nabla . D = \rho \ \ldots (1)$$

$$\begin{matrix} Dx \\ Dy \\ Dz \end{matrix} = \begin{matrix} \varepsilon x & 0 & 0 \\ 0 & \varepsilon y & 0 \\ 0 & 0 & \varepsilon z \end{matrix} \begin{matrix} Ex \\ Ey \\ Ez \end{matrix} \ \ldots (2)$$

$$\varepsilon_x \frac{\partial^2 \varphi}{\partial x^2} + \varepsilon_y \frac{\partial^2 \varphi}{\partial y^2} = qN_A \ \ldots (3)$$

Equation 3 is Poisson's equation in 2D considering an anisotropic dielectric constant. Here the axes of transport X and Y (Fig. S1) are assumed to coincide with the crystal axes of the material. Thus the electric permittivity tensor is diagonal. To solve the differential equation 3 and get an analytical expression for the electric potential, we assume the first term on the left hand side to be much smaller than the second term (quasi-2D approximation). The 2D electric potential in the channel region is then computed similar to the procedure in reference (*21*).

$$\varphi\ x, y\ = \frac{y^2 \varepsilon_{OX,y}\ V_{GS} - V_{FB} - \varphi_s(x)}{\varepsilon_{CH,y} T_{CH} T_{OX}} - \frac{y \varepsilon_{OX,y}\ V_{GS} - V_{FB} - \varphi_s\ x}{\varepsilon_{CH,y} T_{OX}} + \varphi_s(x) \ \ldots (4)$$

Here $\varphi_s(x)$ is the surface potential.

Equation 4 is evaluated at the center of the channel to give $\varphi_C\ x\ = \varphi(x,\frac{T_{CH}}{2})$ and is then expressed in terms of $\varphi_C\ x$ by replacing $\varphi_s\ x\ .\ \varphi\ x,y$ which is expressed in terms of $\varphi_C(x)$ must satisfy equation 3. After substitution into equation 3 and simplification we get,

$$\frac{\partial^2\varphi_C(x)}{\partial x^2}+\frac{1}{\lambda^2}\ V_{GS}-V_{FB}-\varphi_C(x)-\frac{qN_A\lambda^2}{\varepsilon_{CH,x}}\ =0 \ldots (5)$$

where λ is the characteristic length of the device.

$$\lambda=\ \overline{\frac{\varepsilon_{CH,x}T_{CH}T_{OX}}{2\varepsilon_{OX,y}}\ 1+\frac{\varepsilon_{OX,y}T_{CH}}{4\varepsilon_{CH,y}T_{OX}}}\ \ldots (6)$$

From the above equation we see that the characteristic length depends on the dielectric constant along both x and y. The larger the dielectric constant along y, the more the influence of gate voltage and smaller the characteristic length and short channel effects. On the other hand, a large dielectric constant along x means the influence of drain voltage on the channel increases and short channel effects such as DIBL become more prominent. The boundary conditions for solving equation 5 are $\varphi_C(0)=V_{bi}$ and $\varphi_C\ L_G\ =V_{bi}+V_{DS}$. Considering the case of very light to no doping in the channel i.e. $N_A \sim 0$ (hence $V_{bi}=\frac{E_g}{2q}$) , and solving equation 5 with the above boundary conditions we get,

$$\varphi_C\ x\ =\ V_{GS}-V_{FB}\quad 1-e^{-\frac{x}{\lambda}}\ +V_{bi}e^{-\frac{x}{\lambda}}-\frac{\sinh\frac{x}{\lambda}}{\sinh\frac{L}{\lambda}}\ V_{GS}-V_{FB}-V_{bi}\quad 1-e^{-\frac{L}{\lambda}}\ +V_{DS}\frac{\sinh\frac{x}{\lambda}}{\sinh\frac{L}{\lambda}}$$

… (7)

Using $\varphi_C(x)$ as found above, the potential at the surfaces $\varphi_S(x)$ and the 2D potential in the entire channel $\varphi(x,y)$ can also be computed using equation 4. The barrier between the source and drain in the OFF-state is dependent on V_{bi} and hence the bandgap (E_g) of the semiconductor. The larger the bandgap, the larger is the OFF-state barrier between source and drain. λ determines the shape of the barrier between source and drain.

The quasi-2D model provides a good qualitative analysis of the electrostatics in a DGMOS-FET for comparing different channel materials. For more accurate analysis, first principle calculations and self-consistent solutions of the Schrodinger-Poisson equations are essential.

(2) Direct source-to-drain tunneling leakage

A qualitative estimate of the amount of direct source-to-drain tunneling in a material in the OFF-state can be obtained using the electrostatic model derived above. The WKB approximation (equation 8) is used to compute the probability of tunneling across the energy barrier, and the Landauer relation (equation 9) is used to calculate the leakage current due to tunneling (*32*, *33*).

$$T\ E\ = e^{-\frac{2}{\hbar}\int_{x_i}^{x_o}\sqrt{2m^*\ E_C\ x\ -E}\ dx} \quad \ldots (8)$$

$$I_{SD-LEAK} = \frac{2q}{h}\int_{E_S}^{E_{C,max}} M\ E\ \ T\ E\ \ \ f\ E,E_{F,S}\ - f\ E,E_{F,D}\ \ \ dE \ \ldots (9)$$

$$M(E) = \frac{W\ \sqrt{2m^*(E-E_S)}}{\pi\ \hbar} \ldots (10)$$

The parameter values used for the calculations in Fig. 1 are given in table S1.

In equation 8, $T(E)$ is the tunneling probability through the energy barrier at energy level E. x_o and x_i indicate the extent of the barrier. $E_C(x)$ is the conduction band profile between the source and drain from x_i to x_0. m^* is the effective mass of the carriers tunneling through the barrier.

In equation 9, $I_{\text{SD-LEAK}}$ is the direct source to drain leakage current. *M(E)* is the number of ballistic modes of transport at energy E (equation 10) (*32*), E_S is the energy level of the source

(reference) and $E_{C,max}$ is the top of the conduction band profile between the source and drain. $f(E)$ is the Fermi-Dirac distribution and $E_{F,S}$ and $E_{F,D}$ are the Fermi levels in source and drain respectively.

TMDCs have a higher effective mass along the direction of transport (e.g. $m_n^* \sim 0.55m_0$ for MoS_2 versus $m_n^* \sim 0.19m_0$ for Si [100]) (*19, 34*) which reduces the tunneling probability and therefore $I_{SD\text{-}LEAK}$. Figure 1 discusses the impact of effective mass on transistor scaling using the example of a symmetric double-gate MOSFET (DGMOS-FET) structure (Fig. S1). Figure 1A shows normalized $I_{SD\text{-}LEAK}$ as a function of channel thickness for Si and MoS_2. The channel conduction band profile required to calculate $I_{SD\text{-}LEAK}$ is derived using the analytical 2D DGMOS-FET electrostatic model proposed in ref (*21*). The parameter values used in the calculations (table S1) account for quantum mechanical effects on the bandgap, dielectric constant and effective mass at ultra-thin channel thicknesses (*19, 35-39*). MoS_2 shows more than two orders reduction in $I_{SD\text{-}LEAK}$ compared to Si due to the larger electron effective mass. Figure 1B plots the dependence of $I_{SD\text{-}LEAK}$ on L_G. The dotted lines in Fig. 1A and 1B represent the Low Operating Power (LOP) limit for the 2026 technology node as specified by the international technology roadmap for semiconductors (ITRS) (*40*). Figure 1B reveals that for similar channel thickness, MoS_2 transistors can be scaled to shorter gate lengths as compared to Si.

(3) Calculation of D_{IT}

$$SS = \frac{kT ln\ 10}{q}\left(1 + \frac{C_D + C_{IT}}{C_{OX}}\right) \ldots (11)$$

Equation 11 relates SS to the interface trap density for the device (*41*). Here k is the Boltzmann constant, T is temperature in Kelvin and q is the charge of an electron. For the 1D2D-FET

structure, C_D (depletion capacitance) ~ 0, C_{IT} (interface trap capacitance) = qD_{IT} and C_{OX} (oxide capacitance) = ε_{OX}/T_{OX}. ε_{OX} is the permittivity of the gate oxide (ZrO_2 dielectric constant ~ 25 (*42*)) and T_{OX} is the oxide thickness (~ 5.8 nm) measured from TEM in Fig. 2D.

(4) Analytical derivation of parasitic capacitance from fringing electric fields

Figure S8 shows the fringing electric field lines in an underlap transistor. The fringing electric field lines lead to parasitic capacitance ($C_{parasitic}$) and a larger effective channel length (L_{EFF}).

$$C_{OX} = \frac{L_G W \varepsilon_{OX}}{T_{OX}} \ldots (12)$$

$$C_{parasitic} \approx \int_{T_{OX}}^{T_{ZrO2}} \frac{2W\varepsilon_{OX}}{\pi y}\, dy = \frac{2W\varepsilon_{OX}}{\pi} \ln \frac{T_{ZrO2}}{T_{OX}} = \frac{2W\varepsilon_{OX}}{\pi} \ln \left(1 + \frac{T_G}{T_{OX}}\right) \ldots (13)$$

Equation 12 gives the capacitance C_{OX} for the parallel electric field lines from the gate electrode to the channel. ε_{OX} is the electric permittivity of the gate dielectric, W is the width and L_G is the physical gate length. $T_{OX} = (T_{ZrO2} - T_G)$ is kept constant for devices of different gate heights (T_G). Equation 13 calculates the parasitic capacitance due to the fringing electric field lines from the gate electrode and is dependent on T_G. Larger the height of the electrode, higher is the parasitic capacitance. The natural short height of a SWCNT helps achieve small L_{EFF} and small $C_{parasitic}$ compared to lithographically patterned tall gate structures. The above simplistic analytical derivation for $C_{parasitic}$ assumes the fringing electric field lines to be circular (Fig. S8) and underestimates the capacitance. For accurate analysis, simulation of the 2D electrostatics in the device is essential.

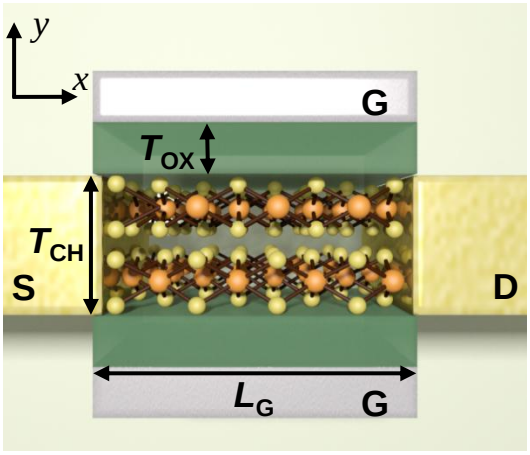

Figure S1: Schematic of dual-gated metal-oxide-semiconductor-field-effect-transistor. Schematic of a symmetric dual-gated metal-oxide-semiconductor-field-effect-transistor (DGMOS-FET) used to study impact of channel material properties on the scaling limit of transistors in Fig. 1.

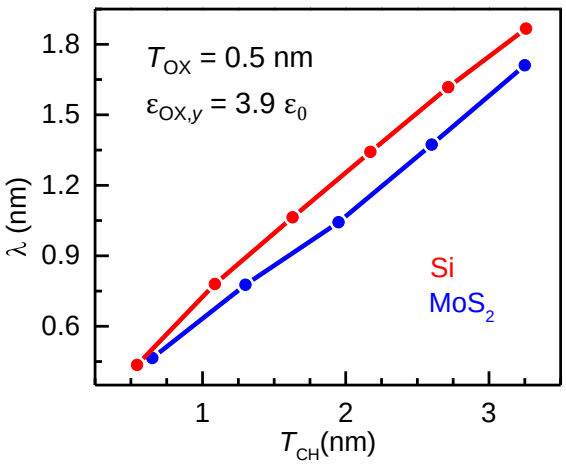

Figure S2: Dependence of characteristic length on channel thickness. Device electrostatic characteristic length (λ) as a function of channel thickness (T_{CH}) for Si and MoS_2.

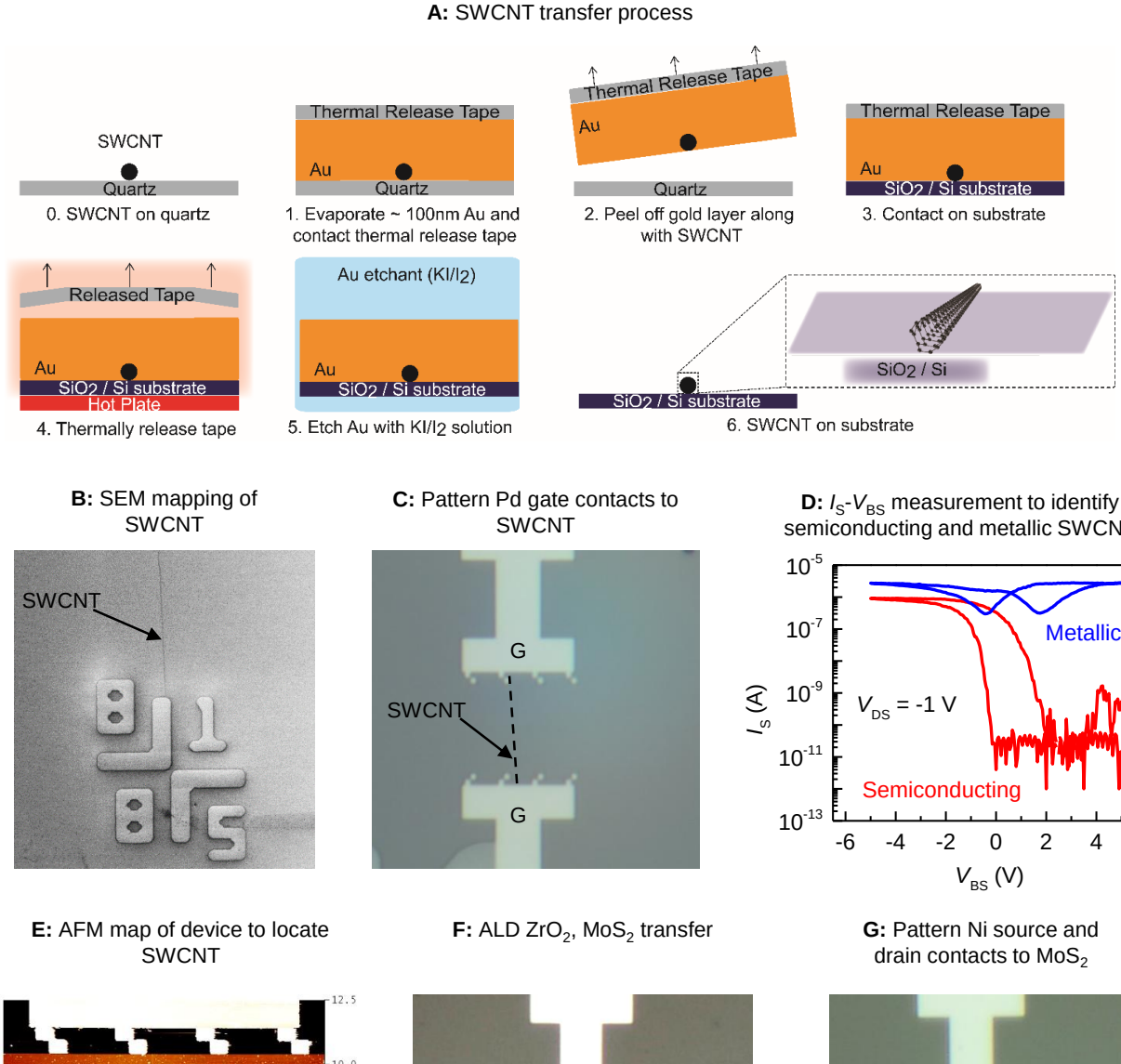

Figure S3: Detailed process flow for SWCNT gated MoS_2 FET

Figure S3 shows the detailed process flow for the device fabrication. The first step of the process involves the transfer of grown SWCNT from the growth substrate (quartz) to the target 50 nm SiO_2 / Si substrate using gold as the transfer layer (*23*) (Fig. S3A). The target substrate is pre-patterned with 0.5/30 nm Cr/Pt alignment markers. These alignment markers are used to relatively locate the transferred SWCNT in a scanning electron microscope (SEM) image (Fig. S3B). Care is taken to ensure the SWCNTs are not damaged during the SEM by minimizing the exposure time under the electron-beam. Gate electrodes are then patterned using electron-beam lithography followed by 30 nm Pd evaporation and liftoff process (Fig. S3C). I_S-V_{BS} measurements of the SWCNT devices help to identify the metallic or semiconducting nature of the SWCNT (Fig. S3D). After the measurement, the SWCNT devices are mapped with an atomic force microscope (AFM) to find the relative location of the SWCNT with respect to the gate electrodes (Fig. S3E). Post the AFM map, ZrO_2 gate dielectric is deposited using atomic layer deposition (ALD) and the MoS_2 flake is transferred on top using a dry pick and transfer method (*14*) using poly(methyl methacrylate) (PMMA) as the transfer medium (Fig. S3F). The AFM map taken prior to the ALD is then used as a mask for a second electron-beam lithography step, to pattern the source and drain electrodes (Ni 40 nm) as shown in Fig. S3G, thus completing the device fabrication.

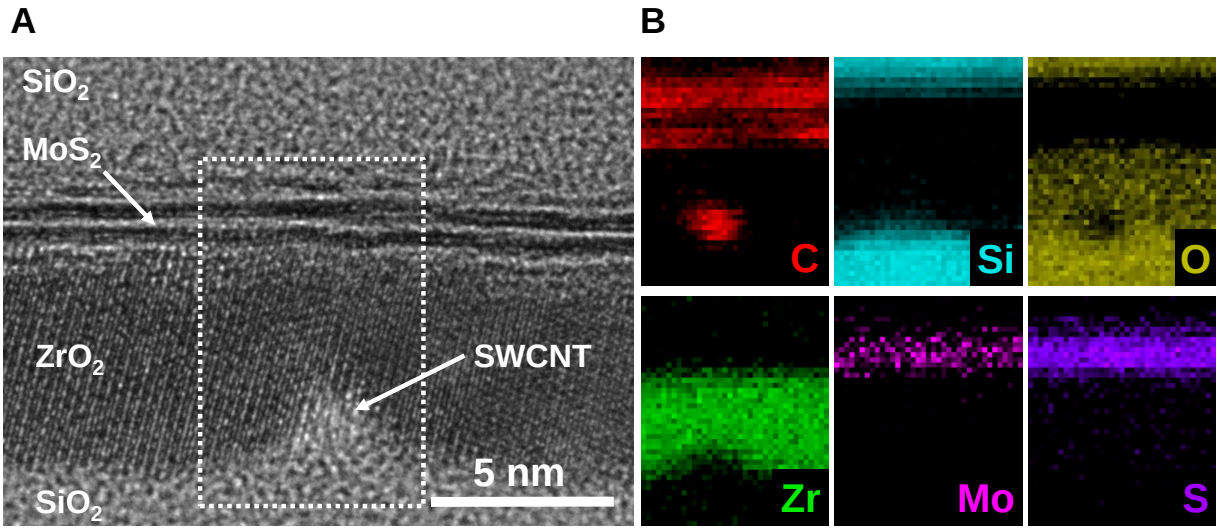

Figure S4: EELS map. EELS mapping of the 1D2D-FET showing the spatial location of the different elements (EDS map is shown for Mo). Carbon mapping clearly indicates the position of the SWCNT under the ZrO_2 gate dielectric and the MoS_2 flake on top of it. Carbon seen on top of the ZrO_2 can be attributed to organic residue like PMMA and contaminants from processing steps and dry transfer of MoS_2.

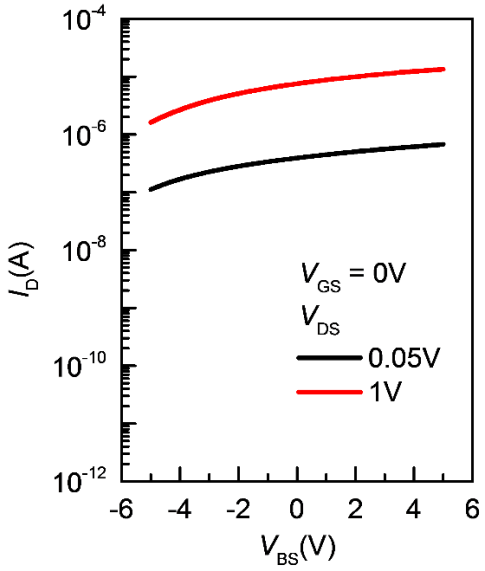

Figure S5: I_D-V_{BS} characteristics obtained by varying the n^+ Si back gate. I_D-V_{BS} characteristics for the device in Fig. 3A-C. The MoS_2 extensions regions are completely inverted using the Si back gate at V_{BS} = 5 V.

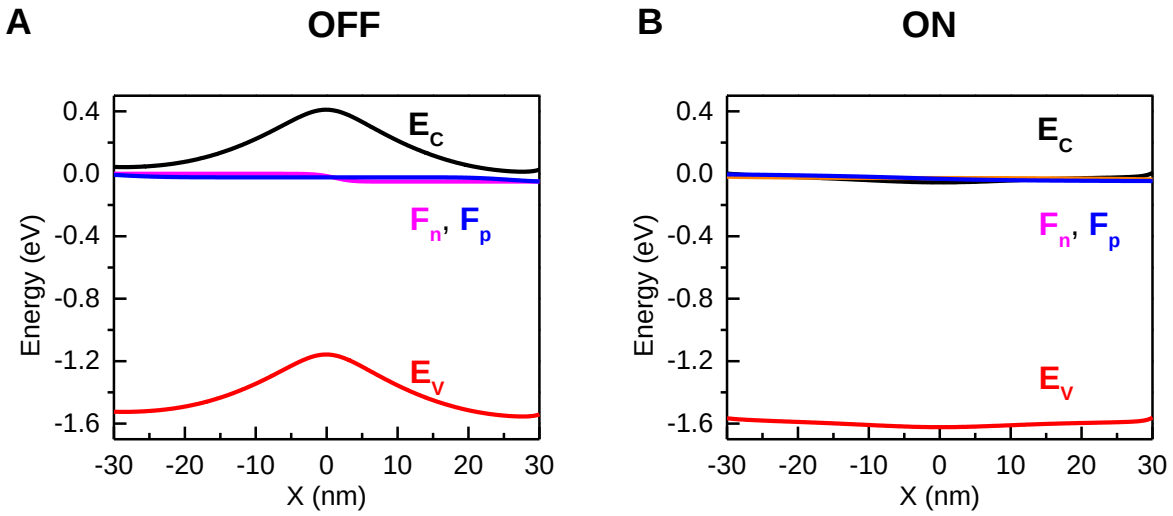

Figure S6: Energy band diagrams in ON and OFF-states. Energy band diagrams corresponding to the TCAD simulations in Fig. 3D-G. V_{BS} = 5 V, V_{DS} = 50 mV, (V_{GS} - V_T) = 1.5 V (ON) and (V_{GS} - V_T) = -0.3 V (OFF), for the 2L MoS_2 device. In the OFF-state the bias applied to the SWCNT creates a barrier which opposes the flow of carriers from source to drain. In the ON-state no barrier exists to the flow of electrons from the source to drain and the ON-current is limited by the series resistance of the extension regions.

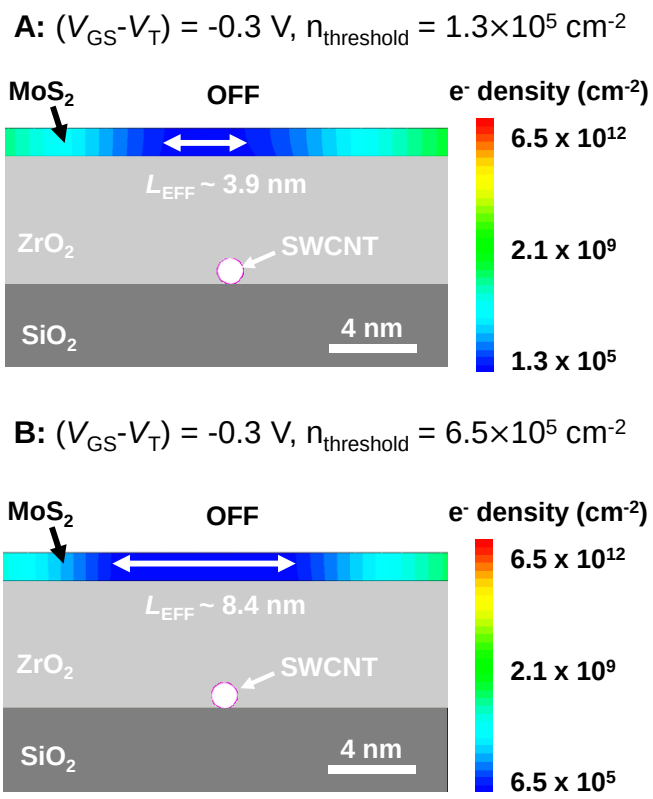

Figure S7: Electron density contour plots. Dependence of L_{EFF} on the definition of OFF-state and $n_{thershold}$ (electron density below which the channel is considered depleted) for V_{BS} = 5 V, V_{DS} = 50 mV (*27-29*). The OFF-state corresponds to (V_{GS} - V_T) = -0.3 V and ON-state corresponds to (V_{GS} - V_T) = 1.5 V (or an ON/OFF current ratio of ~ 10^6). L_{EFF} is of the order of 5 nm as seen from the simulations. The 2D electron density is obtained by multiplying the 3D density obtained from simulations with T_{CH}, by assuming uniform distribution along the thickness of MoS_2.

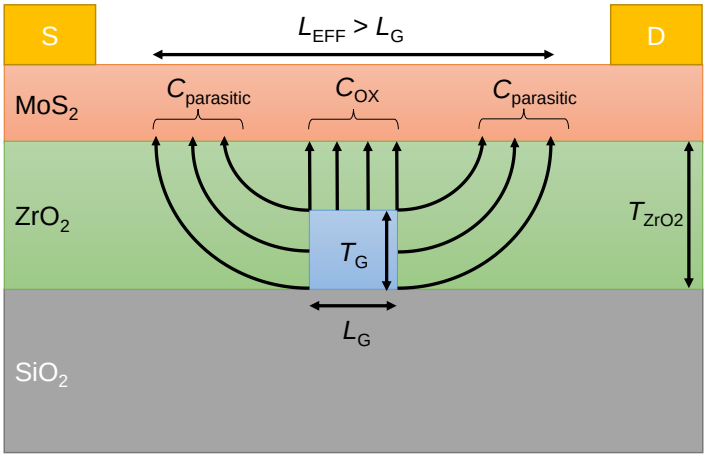

Figure S8: Parasitic capacitance and dependence on gate height. Effective channel length (L_{EFF}) > physical gate length (L_G) due to fringing electric field. L_{EFF} and $C_{parasitic}$ increase as the height of the gate (T_G) increases, for the same value of T_{OX} ($T_{ZrO2} - T_G$). L_{EFF} and $C_{parasitic}$ are small for a SWCNT gate as compared to lithographically defined gates because of the naturally short height of a SWCNT, and hence less fringing electric field lines coupling to the channel (*43*).

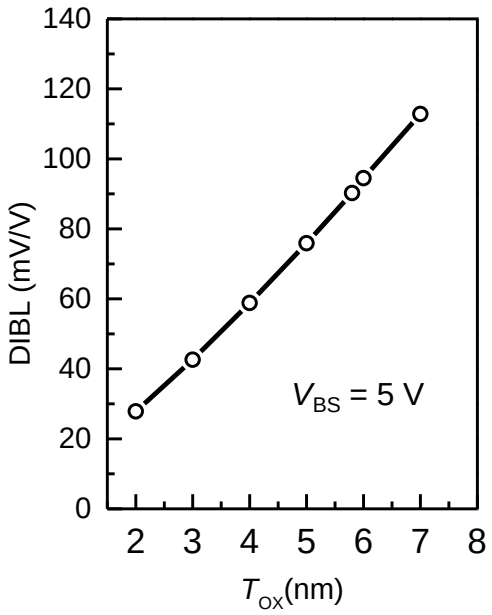

Figure S9: Dependence of DIBL on gate oxide thickness. Drain-induced barrier-lowering (DIBL) as a function of the ZrO_2 thickness calculated using simulations. Effective oxide thickness (EOT) scaling helps improve the electrostatics in the device and reduce DIBL.

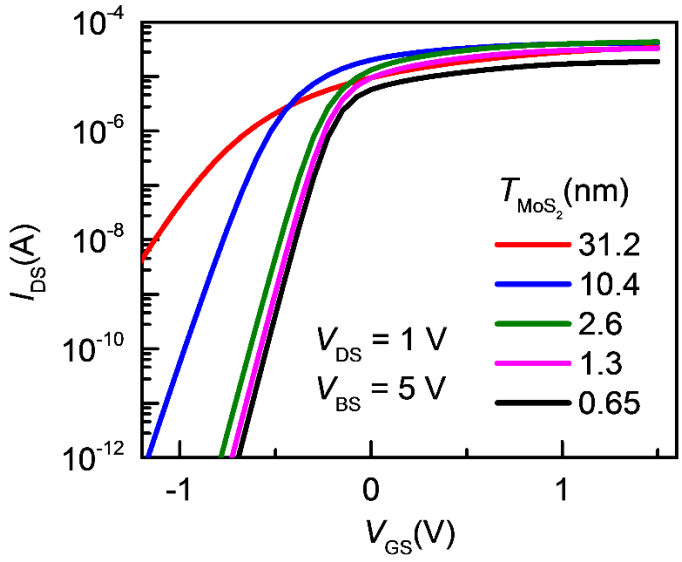

Figure S10: Thickness dependence of MoS_2. I_{DS}-V_{GS} curves for several different channel thicknesses from TCAD simulations used to calculate SS in Fig. 4B. The TCAD results qualitatively match the experimental trends. Doping of MoS_2 (N_D) is assumed to be 10^{17} cm^{-3}, and the dielectric constant of ZrO_2 = 25 (*42*). Electron affinity of MoS_2 is assumed to be 4 eV (*44*). All other values are as specified in table S1. For more quantitative comparison, the analysis must involve simulation of the 2D density of states for MoS_2, correction for contact resistance, oxide and interface traps, along with using more accurate values for m^*, E_G, N_D, etc.

MoS_2				Si			
T_{CH} (nm)	ε (relative) (*35*)	E_G (*38*)	m_e* (*19*)	T_{CH} (nm)	ε (relative) (*36*)	E_G (*37*)	m_e* (*39*)
0.65	3.93	1.88	~ 0.55	0.5431	4.39		~ 0.22
1.3	4.71	1.59	~ 0.55	1.0862	6.62	1.90	~ 0.22
1.95	4.90	1.47	~ 0.55	1.6293	7.66	1.46	~ 0.22
2.6	6.24	1.44	~ 0.55	2.1724	8.70	1.31	~ 0.22
3.25	7.71	1.42	~ 0.55	2.7155	9.73	1.23	~ 0.22
10.4	~ 10	~ 1.3	~ 0.55	3.2586	10.32	1.19	~ 0.22
31.2	~ 10.5	~ 1.3	~ 0.55				

Table S1: Parameter values used for calculations in Fig. 1 and Fig. S2. Values have been extracted from references (*19, 35-39*). The effects of quantum confinement at atomic-scale channel thicknesses on parameter values like bandgap, dielectric constant and effective mass are considered for more accurate analysis. The bandgap values for MoS_2 correspond to the optical bandgap from photoluminescence spectra. The bandgap of Si is obtained from optical absorption spectra.

References

1. T. N. Theis, P. M. Solomon, It's time to reinvent the transistor! *Science* **327**, 1600–1601 (2010). Medline doi:10.1126/science.1187597

2. R. Chau, B. Doyle, S. Datta, J. Kavalieros, K. Zhang, Integrated nanoelectronics for the future. *Nat. Mater.* **6**, 810–812 (2007). Medline doi:10.1038/nmat2014

3. A. D. Franklin, Nanomaterials in transistors: From high-performance to thin-film applications. *Science* **349**, aab2750 (2015). Medline doi:10.1126/science.aab2750

4. M. Lundstrom, Moore's law forever? *Science* **299**, 210–211 (2003). Medline doi:10.1126/science.1079567

5. M. Luisier, M. Lundstrom, D. A. Antoniadis, J. Bokor, in *Electron Devices Meeting (IEDM), 2011 IEEE International* (IEEE, 2011), pp. 11.12.11–1.12.14.

6. H. Kawaura, T. Sakamoto, T. Baba, Observation of source-to-drain direct tunneling current in 8 nm gate electrically variable shallow junction metal–oxide–semiconductor field-effect transistors. *Appl. Phys. Lett.* **76**, 3810–3812 (2000). doi:10.1063/1.126789

7. W. S. Cho, K. Roy, The effects of direct source-to-drain tunneling and variation in the body thickness on (100) and (110) sub-10-nm Si double-gate transistors. *IEEE Electron Device Lett.* **36**, 427–429 (2015). doi:10.1109/LED.2015.2413785

8. B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **6**, 147–150 (2011). Medline doi:10.1038/nnano.2010.279

9. D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, K. Banerjee, A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature* **526**, 91–95 (2015). Medline doi:10.1038/nature15387

10. H. Liu, A. T. Neal, P. D. Ye, Channel length scaling of MoS_2 MOSFETs. *ACS Nano* **6**, 8563–8569 (2012). Medline doi:10.1021/nn303513c

11. H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong, T. Palacios, Integrated circuits based on bilayer MoS_2 transistors. *Nano Lett.* **12**, 4674–4680 (2012). Medline doi:10.1021/nl302015v

12. K. F. Mak, K. L. McGill, J. Park, P. L. McEuen, The valley Hall effect in MoS_2 transistors. *Science* **344**, 1489–1492 (2014). Medline doi:10.1126/science.1250140

13. D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, M. C. Hersam, Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides. *ACS Nano* **8**, 1102–1120 (2014). Medline doi:10.1021/nn500064s

14. H. Fang, C. Battaglia, C. Carraro, S. Nemsak, B. Ozdol, J. S. Kang, H. A. Bechtel, S. B. Desai, F. Kronast, A. A. Unal, G. Conti, C. Conlon, G. K. Palsson, M. C. Martin, A. M. Minor, C. S. Fadley, E. Yablonovitch, R. Maboudian, A. Javey, Strong interlayer coupling in van der Waals heterostructures built from single-layer chalcogenides. *Proc. Natl. Acad. Sci. U.S.A.* **111**, 6198–6202 (2014). Medline doi:10.1073/pnas.1405435111

15. K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevich, S. V. Morozov, A. K. Geim, Two-dimensional atomic crystals. *Proc. Natl. Acad. Sci. U.S.A.* **102**, 10451–10453 (2005). Medline doi:10.1073/pnas.0502848102

16. C.-H. Lee, G.-H. Lee, A. M. van der Zande, W. Chen, Y. Li, M. Han, X. Cui, G. Arefe, C. Nuckolls, T. F. Heinz, J. Guo, J. Hone, P. Kim, Atomically thin p-n junctions with van der Waals heterointerfaces. *Nat. Nanotechnol.* **9**, 676–681 (2014). Medline doi:10.1038/nnano.2014.150

17. Y. Yoon, K. Ganapathi, S. Salahuddin, How good can monolayer MoS_2 transistors be? *Nano Lett.* **11**, 3768–3773 (2011). Medline doi:10.1021/nl2018178

18. L. Liu, Y. Lu, J. Guo, On Monolayer MoS_2 field-effect transistors at the scaling limit. *IEEE Trans. Electron. Dev.* **60**, 4133–4139 (2013). doi:10.1109/TED.2013.2284591

19. D. Wickramaratne, F. Zahid, R. K. Lake, Electronic and thermoelectric properties of few-layer transition metal dichalcogenides. *J. Chem. Phys.* **140**, 124710 (2014). Medline doi:10.1063/1.4869142

20. Supplementary materials are available on *Science* Online.

21. K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, Y. Arimoto, Scaling theory for double-gate SOI MOSFET's. *IEEE Trans. Electron. Dev.* **40**, 2326–2329 (1993). doi:10.1109/16.249482

22. J. Svensson, Y. Tarakanov, D. S. Lee, J. M. Kinaret, Y. W. Park, E. E. B. Campbell, A carbon nanotube gated carbon nanotube transistor with 5 ps gate delay. *Nanotechnology* **19**, 325201 (2008). Medline doi:10.1088/0957-4484/19/32/325201

23. N. Patil, A. Lin, E. R. Myers, K. Ryu, A. Badmaev, C. Zhou, H.-S. P. Wong, S. Mitra, wafer-scale growth and transfer of aligned single-walled carbon nanotubes. *IEEE Trans. NanoTechnol.* **8**, 498–504 (2009). doi:10.1109/TNANO.2009.2016562

24. J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, R. Murphy, Nanowire transistors without junctions. *Nat. Nanotechnol.* **5**, 225–229 (2010). Medline doi:10.1038/nnano.2010.15

25. A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, H. Dai, Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays. *Nano Lett.* **4**, 1319–1322 (2004). doi:10.1021/nl049222b

26. X. Zou, J. Wang, C.-H. Chiu, Y. Wu, X. Xiao, C. Jiang, W.-W. Wu, L. Mai, T. Chen, J. Li, J. C. Ho, L. Liao, Interface engineering for high-performance top-gated MoS_2 field-effect transistors. *Adv. Mater.* **26**, 6255–6261 (2014). Medline doi:10.1002/adma.201402008

27. Y. Taur, MOSFET channel length: Extraction and interpretation. *IEEE Trans. Electron. Dev.* **47**, 160–170 (2000). doi:10.1109/16.817582

28. L. Barbut, F. Jazaeri, D. Bouvet, J.-M. Sallese, Downscaling and short channel effects in twin gate junctionless vertical slit FETs. *Int. J. Microelectron. Comput. Sci.* **4**, 103–109 (2013).

29. S. Hong, K. Lee, Extraction of metallurgical effective channel length in LDD MOSFET's. *IEEE Trans. Electron. Dev.* **42**, 1461–1466 (1995). doi:10.1109/16.398660

30. K. Kang, S. Xie, L. Huang, Y. Han, P. Y. Huang, K. F. Mak, C.-J. Kim, D. Muller, J. Park, High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **520**, 656–660 (2015). Medline doi:10.1038/nature14417

31. D. J. Frank, Y. Taur, H. S. P. Wong, Generalized scale length for two-dimensional effects in MOSFETs. *IEEE Electron Device Lett.* **19**, 385–387 (1998). doi:10.1109/55.720194

32. Mark Lundstrom, (2005), "Notes on the Ballistic MOSFET," https://nanohub.org/resources/489.

33. C. S. Lee, E. Pop, A. D. Franklin, W. Haensch, H. S. P. Wong, A compact virtual-source model for carbon nanotube FETs in the sub-10-nm regime–Part II: Extrinsic elements, performance assessment, and design optimization. *IEEE Trans. Electron. Dev.* **62**, 3070–3078 (2015). doi:10.1109/TED.2015.2457424

34. H. D. Barber, Effective mass and intrinsic concentration in silicon. *Solid-State Electron.* **10**, 1039–1051 (1967). doi:10.1016/0038-1101(67)90122-0

35. X. Chen, Z. Wu, S. Xu, L. Wang, R. Huang, Y. Han, W. Ye, W. Xiong, T. Han, G. Long, Y. Wang, Y. He, Y. Cai, P. Sheng, N. Wang, Probing the electron states and metal-insulator transition mechanisms in molybdenum disulphide vertical heterostructures. *Nat. Commun.* **6**, 6088 (2015). Medline doi:10.1038/ncomms7088

36. G. Zhang, M. B. Yu, C. H. Tung, G. Q. Lo, Quantum size effects on dielectric constants and optical absorption of ultrathin silicon films. *IEEE Electron Device Lett.* **29**, 1302–1305 (2008). doi:10.1109/LED.2008.2005651

37. H. Jang, W. Lee, S. M. Won, S. Y. Ryu, D. Lee, J. B. Koo, S.-D. Ahn, C.-W. Yang, M.-H. Jo, J. H. Cho, J. A. Rogers, J.-H. Ahn, Quantum confinement effects in transferrable silicon nanomembranes and their applications on unusual substrates. *Nano Lett.* **13**, 5600–5607 (2013). Medline doi:10.1021/nl403251e

38. K. F. Mak, C. Lee, J. Hone, J. Shan, T. F. Heinz, Atomically thin MoS_2: A new direct-gap semiconductor. *Phys. Rev. Lett.* **105**, 136805 (2010). Medline doi:10.1103/PhysRevLett.105.136805

39. Y. Liu, N. Neophytou, T. Low, G. Klimeck, M. S. Lundstrom, A tight-binding study of the ballistic injection velocity for ultrathin-body SOI MOSFETs. *IEEE Trans. Electron. Dev.* **55**, 866–871 (2008). doi:10.1109/TED.2007.915056

40. International Technology Roadmap for Semiconductors (ITRS) 2013, http://www.itrs2.net/2013-itrs.html.

41. S. M. Sze, K. K. Ng, *Physics of Semiconductor Devices* (3rd ed., Wiley, 2006).

42. P. Harrop, J. Wanklyn, The dielectric constant of zirconia. *Br. J. Appl. Phys.* **18**, 739–742 (1967). doi:10.1088/0508-3443/18/6/305

43. H. Zhao, Y. C. Yeo, S. C. Rustagi, G. S. Samudra, Analysis of the effects of fringing electric field on FinFET device performance and structural optimization using 3-D simulation. *IEEE Trans. Electron. Dev.* **55**, 1177–1184 (2008). doi:10.1109/TED.2008.919308

44. S. Das, H.-Y. Chen, A. V. Penumatcha, J. Appenzeller, High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett.* **13**, 100–105 (2013). Medline doi:10.1021/nl303583v