Shape-controlled single-crystal growth of InP at low temperatures down to 220 °C

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III–V compound semiconductors are widely used for electronic and optoelectronic applications. However, interfacing III–Vs with other materials has been fundamentally limited by the high growth temperatures and lattice-match requirements of traditional deposition processes. Recently, we developed the templated liquid-phase (TLP) crystal growth method for enabling direct growth of shape-controlled single-crystal III-Vs on amorphous substrates. Although in theory, the lowest temperature for TLP growth is that of the melting point of the group III metal (e.g., 156.6 °C for indium), previous experiments required a minimum growth temperature of 500 °C, thus being incompatible with many application-specific substrates. Here, we demonstrate low-temperature TLP (LT-TLP) growth of single-crystalline InP patterns at substrate temperatures down to 220 °C by first activating the precursor, thus enabling the direct growth of InP even on low thermal budget substrates such as plastics and indium-tin-oxide (ITO)–coated glass. Importantly, the material exhibits high electron mobilities and good optoelectronic properties as demonstrated by the fabrication of high-performance transistors and light-emitting devices. Furthermore, this work may enable integration of III–Vs with silicon complementary metal-oxide-semiconductor (CMOS) processing for monolithic 3D integrated circuits and/or back-end electronics.

III–V semiconductors | InP | growth | low temperature | single crystal

Due to superb electronic and optoelectronic properties, III–V compound semiconductors have been widely used for high-performance photonic and electronic devices. Traditional techniques for growing III–V thin films employ the vapor–solid (VS) growth scheme, e.g., metalorganic chemical vapor deposition (MOCVD) and molecular-beam epitaxy (MBE). However, the adsorbed gas reactants can suffer from low diffusivity on the surface of the growing film compared to the condensation rate when grown at low temperatures and/or on nonepitaxial substrates, leading to polycrystalline or amorphous films instead of single-crystalline ones. In this regard, liquid-phase growth methods have proven to be promising alternatives including vapor–liquid–solid (VLS) (1–8), liquid-phase epitaxy (9), and rapid melt growth (10, 11). In the specific case of VLS growth, a transient liquid phase is introduced that facilitates the kinetics of nucleation and crystal growth, providing an inherent advantage over VS processes and enabling large-area thin-film crystalline growth, even on amorphous substrates (7). In principle, introducing an intermediate liquid phase should allow the growth temperature to be lowered as long as the liquid still has a finite solubility of the gas reactant. For example, InP growth should be achievable down to the melting point of indium (156.6 °C), as liquid indium has a finite solubility of phosphorus at that temperature (12). By separating the phosphine cracking from substrate heating (Fig. 1*A*), we show that the growth temperature of InP can be down to 220 °C.

Fig. 1*B* depicts a schematic of the growth process. Prior to growth, patterned indium metal encapsulated by SiO_x was formed on top of a thin nucleation layer (1 to 5 nm MoO_x or 10 nm Al_2O_3; details in *SI Appendix*, Fig. S1). The InP growth was then conducted in a standard tube furnace flowed with PH_3 as the phosphorus source, diluted by H_2 at a controlled pressure. A source cracking zone with a center temperature of 550 °C allowed the phosphine gas to be converted efficiently into P_2 and P_4 reactants (13), while a calibrated temperature gradient to the substrate prevented phosphorus condensation. Samples were placed at the end of the temperature gradient along the low-temperature region. In this work, the substrate temperature was systematically varied between 220 and 370 °C. During the growth process, phosphorus diffuses through the SiO_x cap and supersaturates the encapsulated liquid indium, resulting in InP nucleation and subsequent growth. Notably, once an InP nucleus is formed in liquid indium, a large phosphorus depletion zone is formed within the vicinity of the nucleus, thus preventing further nucleation events in close proximity. The size of the depletion zone depends on the ratio of the diffusion coefficient of phosphorus in liquid indium to the flux of incoming phosphorus through the solid SiO_x cap (7). In the past, we have shown large depletion zones up to 500 μm in lateral dimension by controlling various process parameters such as phosphorus partial pressure (5). By patterning indium into lateral dimensions smaller than this depletion zone, a high probability of

Significance

A method is developed for enabling direct growth of shape-controlled single-crystal III–Vs on a wide range of substrates, including amorphous and/or low thermal budget substrates. Integration onto such substrates was previously limited by the high growth temperatures and lattice-match requirements of traditional deposition processes. Single-crystalline InP patterns are grown with substrate temperatures down to 220 °C by employing a templated liquid-phase crystallization method. InP grown by this method exhibits high electron mobilities and good optoelectronic properties, as demonstrated by the fabrication of high-performance transistors and light-emitting devices. The growth mode presents important practical implications for a broad spectrum of applications, as high-quality III–Vs can now be grown on virtually any substrate.

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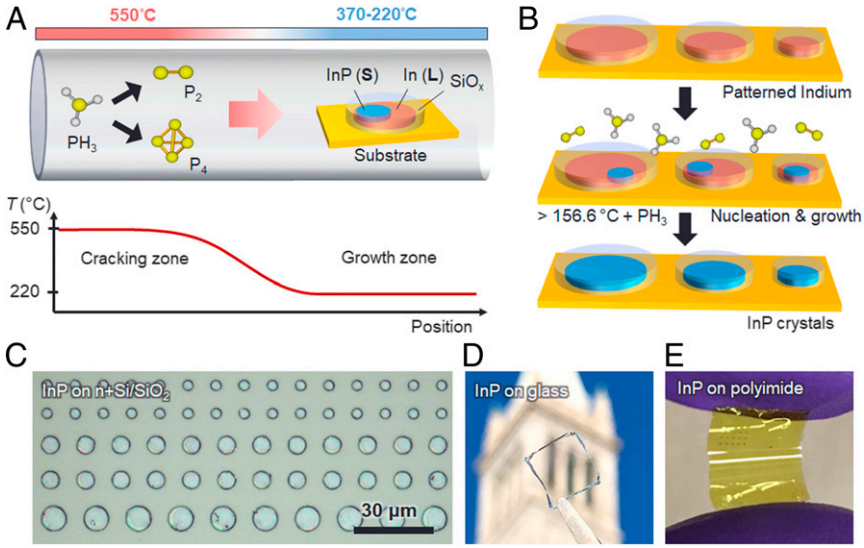

Fig. 1. LT-TLP growth of InP. (*A*) Schematic of the LT-TLP process where the sample is placed at low temperatures while the gas is cracked at high temperature. S indicates the solid phase; L, liquid. (*B*) Schematic of the InP nucleation and growth processes. (*C–E*) Images of as-grown InP patterns on n+Si/SiO_2, ITO-coated glass, and peeled polyimide.

single-crystal patterned growth is enabled with the probability dependent on the ratio of the depletion length to feature size.

Optical images of patterned InP circles (thickness, ∼300 nm; diameter, 3 to 7 μm) grown on Si/SiO_2 at 270 °C are shown in Fig. 1*C*. The low growth temperature characteristic of the LT-TLP method allows for direct growth of InP on an unprecedented range of substrates. As a proof of concept, InP patterns were directly grown on indium-tin-oxide (ITO)-coated soda-lime glass (Fig. 1*D*) and polyimide substrates (Fig. 1*E*), both of which are thermally incompatible with traditional III–V deposition techniques such as MBE and MOCVD. While 220 °C is the lowest growth temperature used in this work to assess material quality, we note that nucleation and growth occur at temperatures as low as 180 °C (*SI Appendix*, Fig. S2*F*), demonstrating the flexibility of this method for a wide range of applications in flexible and transparent electronics. In the past several years, various efforts have explored development of low-temperature grown inorganic semiconductor thin films, including metal oxides and a-Si (14, 15) for glass and plastic-based electronics. The work here presents a viable low-temperature growth technique for III–V compound semiconductors.

X-ray diffraction was performed to identify the zincblende phase of InP patterns grown by low-temperature templated liquid phase (LT-TLP) (*SI Appendix*, Fig. S4). The cross-sectional transmission electron microscopy (TEM) image shown in Fig. 2*A* clearly depicts the crystalline nature of the InP pattern grown atop an amorphous substrate (MoO_x/SiO_2). High-resolution TEM and selected area electron diffraction (SAED) images display twin orientation across the exposed crystal face (Fig. 2 *B* and *C* and *SI Appendix*, Fig. S5). Similar twin boundaries and stacking faults have also been observed in previous reports regarding InP structures grown at higher temperatures (16). Twin-corrected electron backscatter diffraction (EBSD) was further used to examine the lateral dimensions of the crystal domains in our grown samples. A scanning electron microscope (SEM) image of patterned InP crystals grown at 270 °C is shown in Fig. 2*D*, with a corresponding EBSD map (Fig. 2*E* and *SI Appendix*, Fig. S6). The majority of the InP circles with diameters of 3 μm contain a single-crystal domain, with the probability of additional domains per pattern increasing with feature size (*SI Appendix*, Fig. S7*G*). To better understand this behavior, nucleation density for unpatterned thin-film growth was extracted as a function of growth temperature (*SI Appendix*, Fig. S3; a detail discussion is in *SI Appendix*, section 1). By assuming a hexagonal packing geometry (6), the crystal-domain spacing can also be extracted and shows an exponential relationship with growth temperature. A maximum domain size of 8 μm is obtained for the growth temperature 270 °C and PH_3 partial pressure 0.5 torr, consistent with the EBSD measurement (Fig. 3*E* and *SI Appendix*, Fig. S7).

Photoluminescence (PL) measurements were performed to further characterize the material quality of our crystals (17). In Fig. 2*F*, normalized PL spectra are plotted for growth temperatures from 220 to 370 °C. The Urbach tails derived from the spectra show that the Urbach energies of the crystals grown at low temperature are comparable to the values from 500 to 535 °C growth and bulk n-type single-crystal wafer references (7) (*SI Appendix*, Table S1), indicating a low density of defect states near the band edges. Moreover, the maximum PL quantum yield (QY) measured was 10 ± 2% for the samples grown at 220 °C without surface passivation or cladding layers (Fig. 2*G*), demonstrating the high-quality nature of crystals produced by the LT-TLP method. The corresponding normalized PL spectra as a function of excitation power do not show any strong change in spectral shape, which is also indicative of a low defect density (*SI Appendix*, Fig. S8). The QY also shows minimal dependence on the growth temperature in the explored range of 220 to 370 °C (Fig. 2*G*). Overall, optical measurements suggest high material quality, even for the unprecedented low growth temperatures used here.

InP light-emitting devices were fabricated to realize the potential of the LT-TLP method for optoelectronic applications. Here we employed the transient electroluminescent (t-EL) device structure, where high injection levels for bright EL are achieved without the need of forming simultaneous ohmic contacts to electrons and holes (18). InP was grown on n^+ Si (gate)/SiO_2 (gate oxide) and contacted by an evaporated Ti/Au (source) electrode (Fig. 3*A*). During t-EL operation, the source is grounded and a square-wave voltage (V_G) is applied to the gate. Efficient bipolar carrier injection is achieved during each voltage transition. The injected carriers then recombine with the stored charges from the previous cycle, resulting in EL emission. This device architecture has been previously reported in other material systems including monolayer semiconductors (18). The transient EL can be visualized by the time-resolved EL spectrum in Fig. 3*B*,

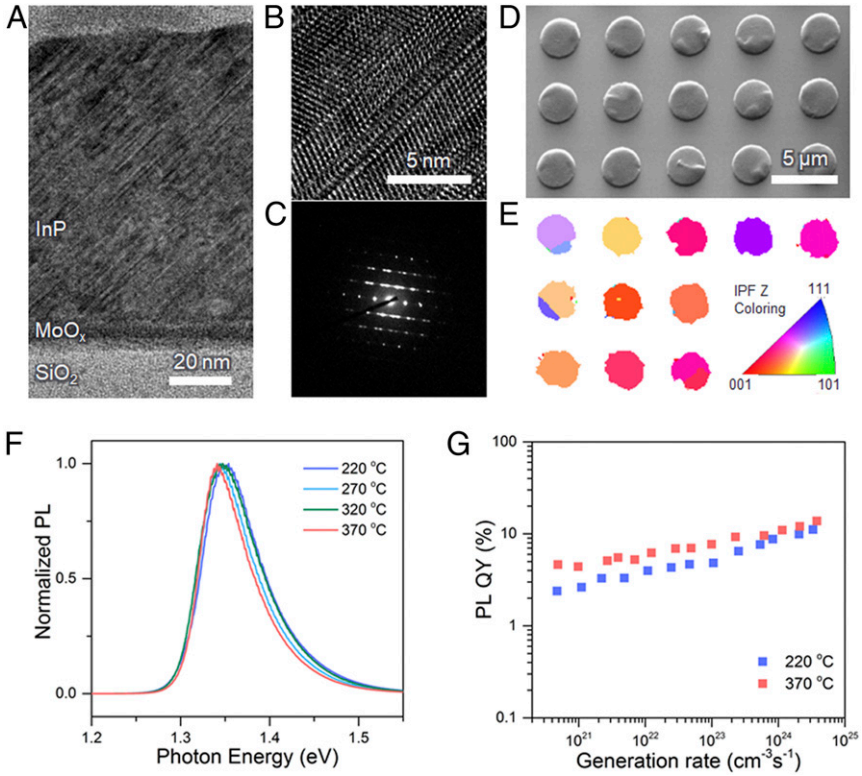

Fig. 2. Characterization of single-crystalline InP. (*A*) TEM. (*B*) HRTEM, and (*C*) SAED of InP crystals grown at 270 °C substrate temperature. (*D*) SEM image and (*E*) corresponding EBSD map for 3-μm circles of InP grown at 270 °C. (*F*) Internal QY for LT-TLP InP grown at 220 and 370 °C. Note that more than 5 samples were measured for each growth temperature. (*G*) Normalized steady-state PL spectra for LT-TLP InP grown at different temperatures.

with emission transients closely following the rising and falling edges of V_G. The transient emission displays greater intensity on the rising edges of each pulse, indicating a lower injection barrier for electrons.

The EL spectrum for a t-EL device closely resembles the PL emission spectrum (Fig. 3*C*). The dependence of EL intensity with respect to gate bias and frequency are presented in Fig. 3 *D* and *E*, respectively. EL is observed when $V_G > 2.5$ V, where the turn-on voltage depends on the bandgap of the InP (1.3 eV) and parasitic resistances in the device. Emission intensity increases linearly with frequency, reflecting the pulsed nature of t-EL operation. EL imaging of the t-EL device is shown in Fig. 3*F*. EL is observed near the source contacts, and the emission region laterally extends from the contact edge by 7 to 9 μm. This successful

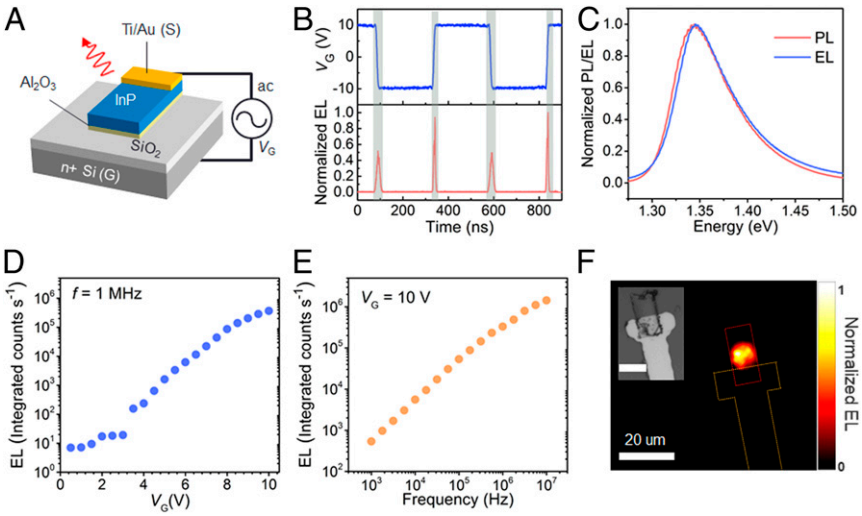

Fig. 3. t-EL devices on silicon substrate. (*A*) Schematic structure of the t-EL device. The growth temperature of InP is 270 °C using an insulating Al_2O_3 layer for nucleation. (*B*) Time-resolved EL spectrum for 1 full cycle of a t-EL device in operation. (*C*) EL and PL spectra for a t-EL InP device. (*D*) Voltage and (*E*) frequency dependence of a representative device. (*F*) EL image of a device modulated with a $V_g = \pm 10$ V, $f = 20$-MHz square wave. (*Inset*) An optical microscope image of a device.

demonstration indicates a promising path toward the implementation of TLP-grown InP in displays and future photonic applications, even on low-thermal-budget substrates.

We also examined the electronic quality of the InP to determine the viability of this method for electronic applications. The measured Hall mobilities as a function of growth temperature are shown in Fig. 4*A*. As-grown InP was patterned into 7×7-μm^2 squares to avoid grain-boundary influence on measurements (see *Materials and Methods* and *SI Appendix*, section 2). The average Hall mobility μ_H is 743 $cm^2\ V^{-1}{\cdot}s^{-1}$ for 370 °C and 236 $cm^2\ V^{-1}{\cdot}s^{-1}$ for 235 °C, for an electron concentration in the range 10^{15} through 10^{16} cm^{-3}. The highest μ_H measured for the 370 °C case is 862 $cm^2\ V^{-1}{\cdot}s^{-1}$, a value approaching 30% of mobilities reported for InP wafers with similar doping concentrations (19, 20).

Field-effect transistors were fabricated using patterned InP microwires as the channel (*W*/*L*, 0.25 to 1 μm/4 to 20 μm; thickness, ∼80 nm). ZrO_2/Ni/Au was deposited as the top gate and Pd/Ge contacts were formed as source/drain (Fig. 4*B*, fabrication details in *Materials and Methods*). I_D-V_G and I_D-V_D characteristics for a device are presented in Fig. 4 *C* and *D*. The device exhibits I_{ON}/I_{OFF} ratio of 1.5×10^4 and I_{ON} of 14 μA/μm at $V_G = V_D = 3$ V. After correcting for contact resistance (see *SI Appendix*, section 2) (20), we extracted a peak effective electron mobility of 663 $cm^2\ V^{-1}{\cdot}s^{-1}$. This effective mobility is comparable with average Hall mobilities for the same growth temperature, and similar to the mobility previously reported for wires grown at 500 to 535 °C (7).

In addition to applications for plastic and glass electronics and lighting, LT-TLP could also present a viable approach toward monolithic integration of high-mobility III–V semiconductors on silicon complementary metal-oxide-semiconductor (CMOS) for 3D integrated circuits and back-end electronics. In this regard, the semiconductor must be processed at temperatures below 400 °C, which is the thermal budget of silicon CMOS (21). Low-temperature growth of high-quality semiconductors has proven extremely challenging (*SI Appendix*, Table S2), thus to date limiting the practical realization of such architectures. LT-TLP growth directly overcomes this fundamental problem. This presents an important future research direction employing LT-TLP.

In summary, we present single-crystalline InP patterned growth at ultralow temperatures down to 220 °C. The crystals exhibit high electron mobility and PL QY, notably without surface passivation or cladding layers. Furthermore, the method presented in this work is compatible with a wide range of substrates without epitaxial growth and transfer requirements (22–25), thus dramatically broadening the application domain of III–V semiconductors. While the patterned structures are single crystalline, the current work does not provide for orientation control. In the future, by controlling the surface energies of the substrate, it may be possible to preferentially nucleate a specific orientation. Additionally, the approach could be universal to other III–V compound semiconductors. In this regard, future exploration of LT-TLP growth of other indium- and gallium-based compounds, including ternary alloys, would be of interest. Finally, while a temperature gradient was used to activate the precursor, in the future, plasma could also be used to perform a similar role in a more controlled environment.

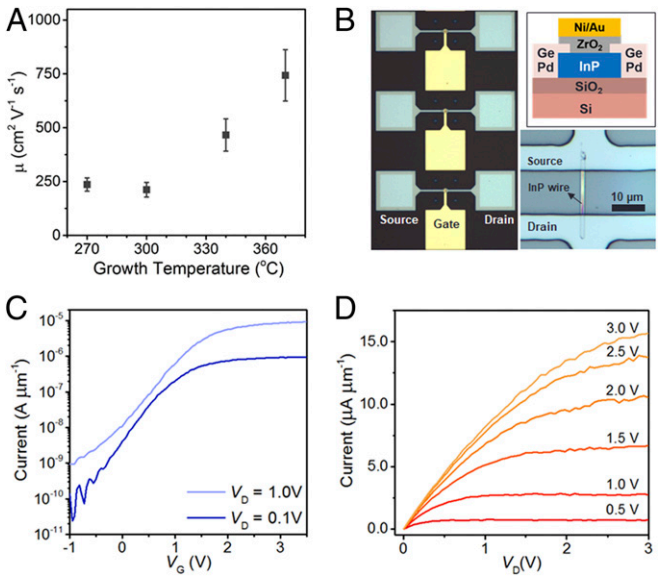

Fig. 4. Electronic characterization of LT-TLP InP. (*A*) Average Hall mobility vs. temperature, with error estimated by measurement geometry indicated by whiskers. Note that more than 3 devices were measured for each growth temperature. (*B*) Schematic and optical images (*Bottom Right*) before gate deposition of single-microwire transistors. (*C* and *D*) Transistor characteristics of an InP transistor with *W*/*L* 1 μm/20 μm and thickness ∼80 nm. InP was grown at 370 °C.

Materials and Methods

Temperature Gradient Calibration. Prior to growth, the temperature gradient from furnace center to furnace end was calibrated using a thermocouple in situ in order to closely approximate the substrate temperature for our typical center set point of 550 °C. The thermocouple was inserted inside the tube via feedthrough, and temperatures were measured under gas flow at different positions. Substrate placement for each growth temperature was dictated by the temperature reading for all calibration conditions.

Substrate Preparation and Growth Method. The substrates used were 50-nm SiO_2/n^+ Si, commercial ITO-coated soda-lime glass (12-Ω·cm square float glass, Sigma-Aldrich), and polyimide substrates prepared using SiO_2/n^+ Si handle wafers and a spun polyimide film (HD MicroSystems, polyimide-2525) cured at 300 °C. Photolithography was used to pattern the substrate, prior to evaporating a thin nucleation layer of material such as MoO_x, followed by indium and confining caps of SiO_x (*SI Appendix*, Fig. S1). The substrate was then heated in a tube furnace in hydrogen to the desired substrate temperature and exposed to PH_3 gas diluted in H_2 to a desired partial pressure. Growth time for patterned InP was 30 to 60 min. The resulting phosphorized films were then etched in hydrofluoric acid to remove the SiO_x caps before further processing. Insulating Al_2O_3 nucleation layers were used for the t-EL devices and MoO_x nucleation layers were used for all other structures shown in this study. Typical film thicknesses, measured by quartz crystal monitor, were 5 to 10 nm for e-beam evaporated Al_2O_3, 0.3 to 1.3 nm for thermally evaporated MoO_x, 40 to 150 nm for e-beam evaporated indium, and 10 to b50 nm for e-beam evaporated SiO_x side caps.

EBSD Measurement. EBSD measurements were performed using an FEI Quanta field emission gun SEM and an Oxford EBSD detector with a fluorescent screen. Oxford Aztec and Tango software were used to analyze the EBSD patterns and maps, and to generate inverse pole figure color schemes for the data shown. Twin-boundary correction was performed in the same software by removing <111> 60° rotational boundaries and replotting grain surface orientation.

Optical Characterization. For PL measurement, a 514-nm Ar ion laser was used to excite each sample at the same power (80 μW), with light collected by a 50× objective lens, passed through a 550-nm long-pass filter, and analyzed by a spectrometer and Si charge-coupled device. PL QY and EL data for this study were collected using a homebuilt optical system (18). Briefly, PL QY measurements were calibrated using a ThorLabs SLS201 calibration lamp reflected off a Lambertian surface under the objective, followed with the measurement of system response by collection of the diffusely reflected excitation beam by the system spectrometer and cross-calibration with the lamp.

t-EL Device Fabrication and Measurement. All transient EL devices were fabricated using InP squares grown at 270 ± 10 °C. Ti/Au contacts patterned by photolithography were used for a typical device, with a forming gas anneal at 270 °C for ∼10 min to improve the contact–InP interface. For all devices, a lower than normal contact anneal temperature was chosen to fit

the maximum growth temperature, maintaining the low-T process window. Measurements were performed in a similar manner to ref. 18, with the Ti/Au source grounded and a square-wave excitation applied to the n^+ silicon back gate. Al_2O_3 was used as an insulating nucleation layer. The square wave was generated by a bipolar-based Agilent 33522A waveform generator, and EL images presented were collected using a microscope system and an Andor Luca camera with excitation in ambient environment.

Hall Device Fabrication and Measurement. Hall measurement devices were fabricated in a square configuration using MoO_x nucleation layers less than 1.4 nm and as-grown thicknesses of ∼85 to 90 nm as estimated by atomic force microscopy and cross-sectional TEM measurements. A square Van der Pauw configuration with devices in the 7 through10-μm range was chosen to limit fabrication and growth complexity, and electron beam lithography was used to pattern contacts to avoid alignment offset error. A Pd/Ge metallization was used to give linear contact behavior for all devices, with rapid thermal annealing in a 5% H_2/95% N_2 ambient to improve contact resistance. The temperature for this step was maintained at a maximum of 10 °C above the growth temperature to avoid annealing effects on the electrical parameters. An Ecopia HMS 300 Hall measurement tool was used with a ∼0.55-T permanent magnet for the presented measurements, with currents in the 10 through 100-nA range. Further details on the measurements and cross-checking procedures, along with geometrical error estimation, can be found in *SI Appendix*.

Transistor Fabrication and Measurement. Transistor devices were fabricated using InP grown at 370 ± 10 °C, given the higher measured Hall mobility at this growth temperature. First, microwires were patterned using e-beam lithography with widths between 250 and 1000 nm. Indium substrates were prepared as previously described, with MoO_x nucleation layer thickness less than 1.2 nm and indium thickness ∼30 to 40 nm. Source and drain contacts of Pd/Ge were then patterned by photolithography on the ∼75 to 85-nm as-grown films, with channel lengths between 4 and 20 μm. To minimize contact resistance, an optimized Pd/Ge rapid thermal alloy process was used in a forming gas ambient, in order to dope a thin surface layer under the contact and provide a spike-free alloyed contact interface with the PdGe alloy metal. The optimum contact annealing conditions were a 225 °C/3 min initial alloy step followed by a 390 °C/3 min anneal step. Following contact annealing, a 15-nm ZrO_2 gate oxide a was thermally deposited at 200 °C using a Cambridge Nanotech atomic layer deposition system and tetrakis (ethylmethylamido) zirconium Zr precursor with water as the oxidizer. The gate metal was then patterned by photolithography, with a Ni/Au gate used to compare to prior InP devices.

Data Availability. All datasets have been deposited in Dryad: https://datadryad.org/stash/dataset/doi:10.6078/D15H5W.

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1. R. S. Wagner, W. C. Ellis, Vapor-liquid-solid mechanism of single crystal growth. *Appl. Phys. Lett.* **4**, 89 (1964).
2. A. M. Morales, C. M. Lieber, A laser ablation method for the synthesis of crystalline semiconductor nanowires. *Science* **279**, 208–211 (1998).
3. X. Duan, Y. Huang, Y. Cui, J. Wang, C. M. Lieber, Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices. *Nature* **409**, 66–69 (2001).
4. K. A. Dick *et al*., Synthesis of branched 'nanotrees' by controlled seeding of multiple branching events. *Nat. Mater.* **3**, 380–384 (2004).
5. R. Kapadia *et al*., Deterministic nucleation of InP on metal foils with the thin-film vapor-liquid-solid growth mode. *Chem. Mater.* **26**, 1340–1344 (2014).
6. R. Kapadia *et al*., A direct thin-film path towards low-cost large-area III-V photovoltaics. *Sci. Rep.* **3**, 2275 (2013).
7. K. Chen *et al*., Direct growth of single-crystalline III-V semiconductors on amorphous substrates. *Nat. Commun.* **7**, 10502 (2016).
8. M. Heiss *et al*., III-V nanowire arrays: Growth and light interaction. *Nanotechnology* **25**, 014015 (2014).
9. H. Nelson, Epitaxial growth from the liquid state and its application to the fabrication of tunnel and laser diodes. *RCA Rev.* **24**, 603–615 (1963).
10. S.-L. Chen, P. B. Griffin, J. D. Plummer, Single-crystal GaAs and GaSb on insulator on bulk Si substrates based on rapid melt growth. *IEEE Electron Device Lett.* **31**, 597–599 (2010).
11. T. J. Trentler *et al*., Solution-liquid-solid growth of crystalline III-V semiconductors: An analogy to vapor-liquid-solid growth. *Science* **270**, 1791–1794 (1995).
12. K. Yamaguchi, K. Itagaki, Y. A. Chang, Thermodynamic analysis of the In-P, Ga-As, In-As and Al-Sb systems. *Calphad* **20**, 439–446 (1996).
13. R. Chow, Y. G. A. Chai, PH_3 cracking furnace for molecular beam epitaxy. *J. Vac. Sci. Technol. A* **1**, 49–54 (1983).
14. K. Nomura *et al*., Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **432**, 488–492 (2004).
15. M.-G. Kim, M. G. Kanatzidis, A. Facchetti, T. J. Marks, Low-temperature fabrication of high-performance metal oxide thin-film electronics via combustion processing. *Nat. Mater.* **10**, 382–388 (2011).
16. J. Bao *et al*., Optical properties of rotationally twinned InP nanowire heterostructures. *Nano Lett.* **8**, 836–841 (2008).
17. J. Wang, M. S. Gudiksen, X. Duan, Y. Cui, C. M. Lieber, Highly polarized photoluminescence and photodetection from single indium phosphide nanowires. *Science* **293**, 1455–1457 (2001).
18. D. H. Lien *et al*., Large-area and bright pulsed electroluminescence in monolayer semiconductors. *Nat. Commun.* **9**, 1229 (2018).
19. W. Walukiewicz *et al*., Electron mobility and free-carrier absorption in InP; Determination of the compensation ratio. *J. Appl. Phys.* **51**, 2659–2668 (1980).
20. D. Hofmann, G. Müller, N. Streckfuß, Semi-insulating electrical properties of undoped InP after heat treatment in a phosphorus atmosphere. *Appl. Phys. A Solids Surf.* **48**, 315–319 (1989).
21. H. Takeuchi, A. Wung, X. Sun, R. T. Howe, T. J. King, Thermal budget limits of quarter-micrometer foundry CMOS for post-processing MEMS devices. *IEEE Trans. Electron Dev.* **52**, 2081–2086 (2005).
22. J. A. Rogers, T. Someya, Y. Huang, Materials and mechanics for stretchable electronics. *Science* **327**, 1603–1607 (2010).
23. M. A. Meitl *et al*., Transfer printing by kinetic control of adhesion to an elastomeric stamp. *Nat. Mater.* **5**, 33–38 (2006).
24. A. Carlson, A. M. Bowen, Y. Huang, R. G. Nuzzo, J. A. Rogers, Transfer printing techniques for materials assembly and micro/nanodevice fabrication. *Adv. Mater.* **24**, 5284–5318 (2012).
25. H. Ko *et al*., Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors. *Nature* **468**, 286–289 (2010).

SI Appendix

Shape-controlled single-crystal growth of InP at low temperatures down to 220 °C

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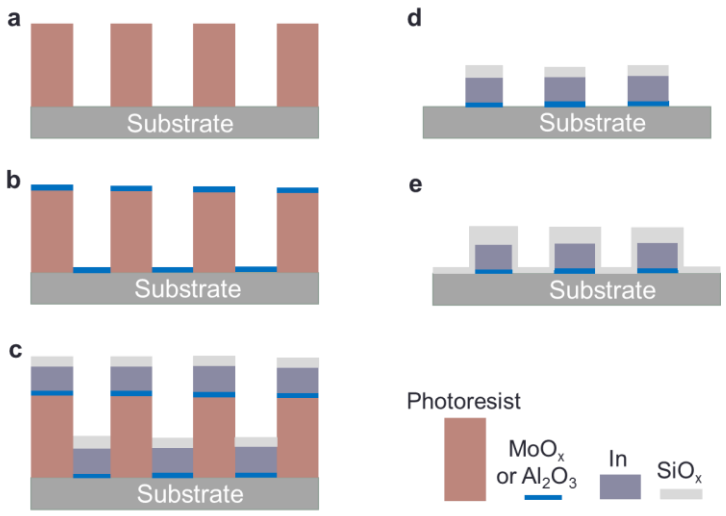
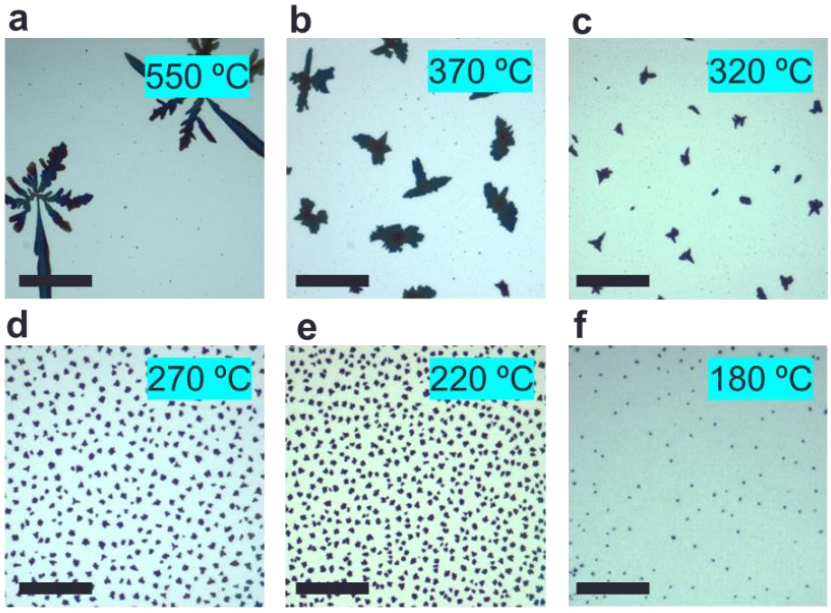
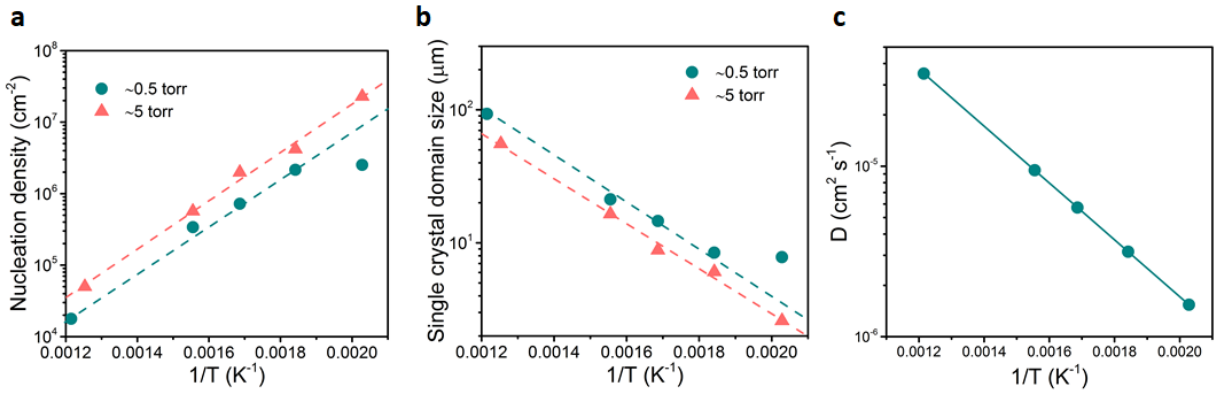


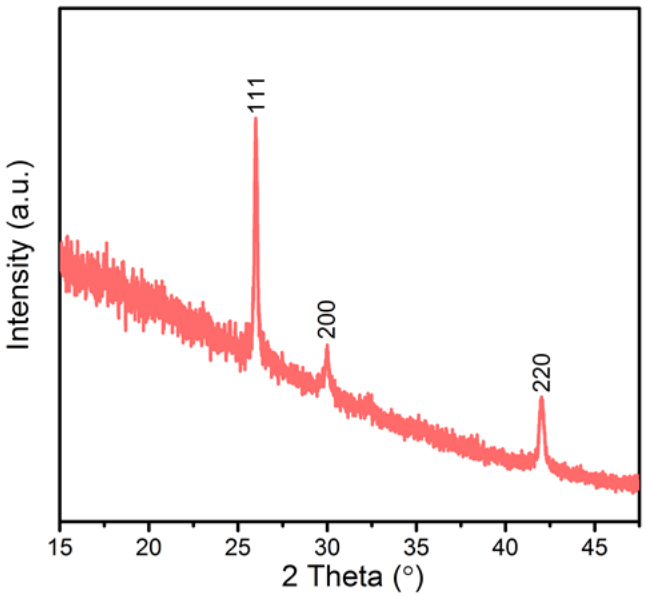
***SI Appendix*, Figure S1. Substrate preparation for LT-TLP crystal growth.** (a) Photolithography is used to pattern the substrate and (b) a thin MoO_x/Al_2O_3 layer is evaporated as the nucleation layer. (c) Then, indium and top confining SiO_x are evaporated. (d) After that, the whole stack is lifted off. (e) Additional SiO_x is evaporated to fully cover the indium.



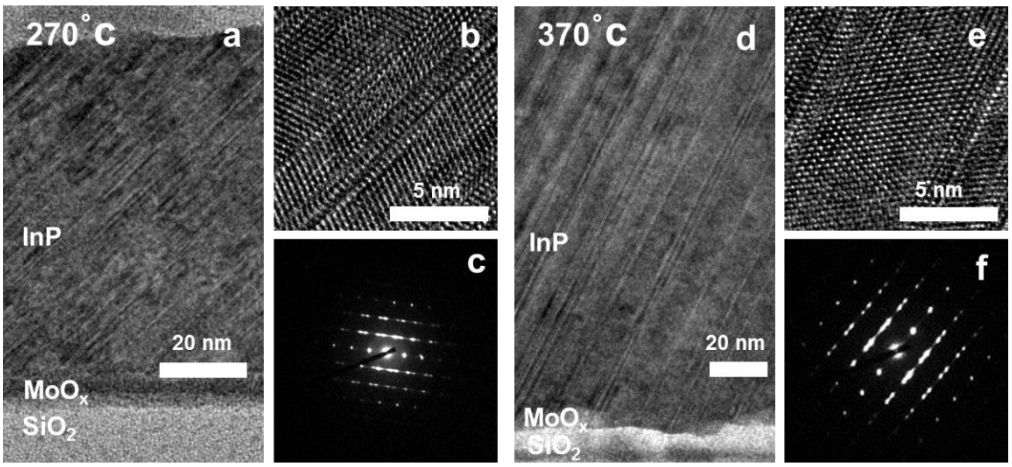
SI Appendix, Figure S2. Unpatterned InP growth. InP nucleation images with unpatterned indium (~100 nm) substrates at growth temperatures of (**a**) 550 °C, (**b**) 370 °C, (**c**) 320 °C, (**d**) 270 °C, (**e**) 220 °C, and (**f**) 180 °C. 3 minute growths were done with a PH_3 partial pressure of 0.5 torr, demonstrating relative growth rate and nucleation density as temperature is lowered. Scale bars for all images are 30 μm.



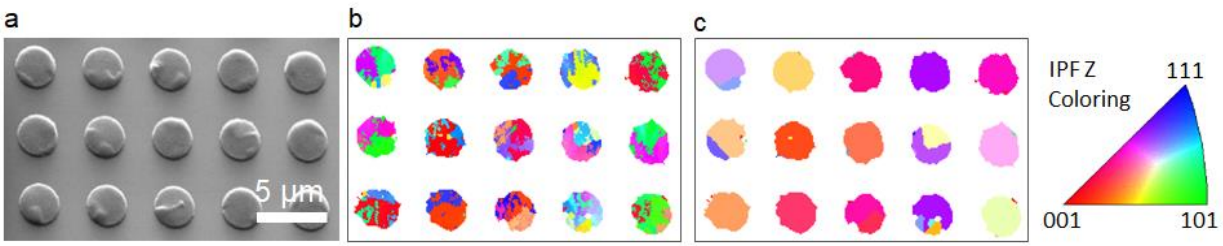
SI Appendix, Figure S3. **Temperature dependence of nucleation density, crystal domain size and diffusivity.** (**a**) Nucleation density and (**b**) crystal domain size at growth temperatures between 220 °C and 550 °C are calculated from SI Appendix, Figure S2. The estimate of domain size is extracted from the corresponding nucleation density data by assuming a hexagonal packing geometry during growth. PH_3 partial pressure varied between 0.5 torr and 5 torr. (**c**) Diffusivity of the phosphorus in liquid indium as a function of 1/T obtained from the literature (*Journal of Crystal Growth* **46** 55-58 (1979)).



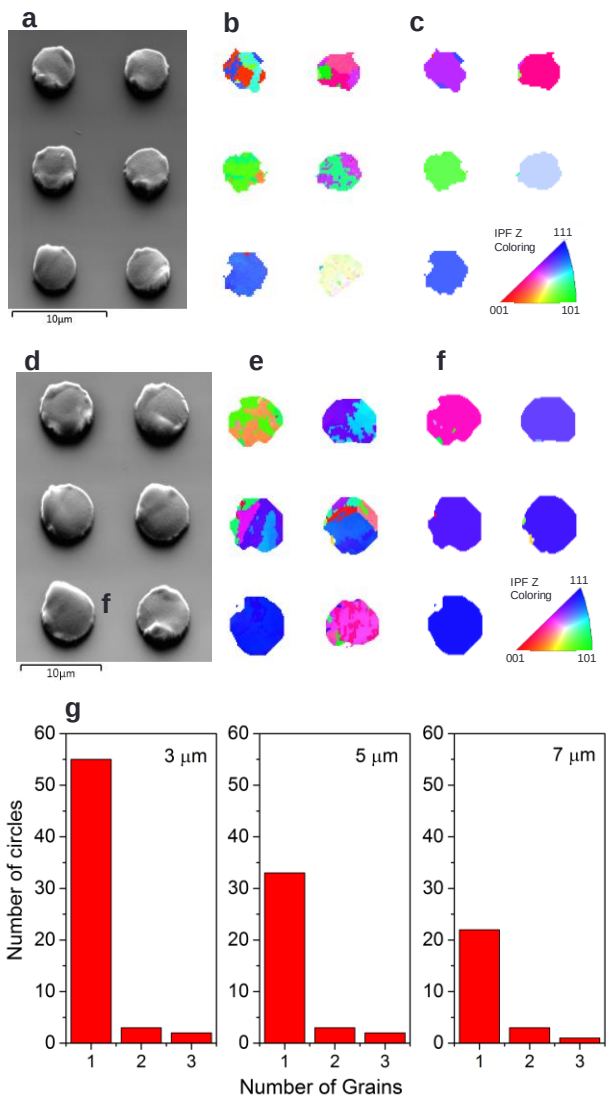
SI Appendix, Figure S4. XRD spectrum of LT-TLP InP patterns grown at 270 °C. Only peaks from the zincblende phase are observed.



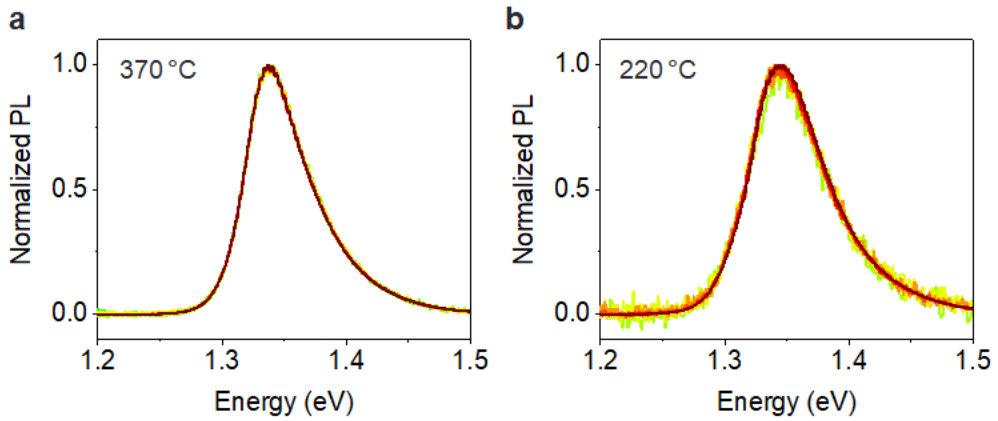
SI Appendix, Figure S5. TEM and SAED images of LT-TLP InP crystals grown at 270 and 370 °C. (**a,d**), TEM, (**b,e**), HRTEM and(**c,f**), SAED of InP crystals grown at 270 ºC and 370 °C substrate temperature.



SI Appendix, Figure S6. Twin correction. (a) SEM image and corresponding EBSD maps before (b) and (c) after twin correction for 3 µm circles grown at 270 ºC.



SI Appendix, Figure S7. SEM images and EBSD maps for LT-TLP InP circles. SEM images of patterned LT-TLP InP circles with diameter **(a)** 5 μm and **(d)** 7 μm (growth temperature 270 °C, PH_3 partial pressure 0.5 torr), along with corresponding EBSD maps (**b, e**) before and (**c, f**) twin boundary correction. (**g**) The statistical distribution of the number of LT-TLP InP circles vs. number of grains plotted as histograms (growth temperature 270 °C, PH_3 partial pressure 0.5 torr) for circles of diameter 3 μm, 5 μm and 7 μm.



SI Appendix, Figure S8. Normalized PL spectra over 4 orders of magnitude of generation rate. Growth temperature of (**a**) 370 °C and (**b**) 220 °C.

SI Appendix, Table S1. Urbach tail parameter values of LT-TLP InP vs. growth temperature.

Growth Temperature (°C)	220	270	320	370	550	n-InP wafer reference (doping level 5×10^{16})
Urbach Tail Parameter (mV)	9.5	9.16	9.11	8.85	9.44	8.10

Doping concentrations referenced for extraction of the Urbach tail parameter were extracted assuming a Burstein-Moss shift due to band filling in the InP. Using a parabolic band model, the doping estimated from band edge shift is given to be:

$$n = 10^{19} cm^{-3} \left(\frac{\Delta E_g}{16.9} \frac{m}{m_0}\right)^{\frac{3}{2}}$$

Here, m/m_0 is the ratio of the InP electron effective mass to the free electron mass, and Urbach energy ΔE_g is taken with reference to a wafer with a low nominal doping concentration, in our case a reference wafer with doping concentration 5×10^{16} cm^{-3}.

SI Appendix, Table *S*2. Comparison of III-V growth techniques.

Material	Morphology	Growth technique	Substrate temperature (°C)	Substrate	μ ($cm^2 V^{-1} s^{-1}$)	PL QY	Reference
	single crystalline patterned films	**This work**	**220-370**	**Si/Glass/ Polyimide**	**663**	**10 %**	**This work**
	nanostructure	Solution growth	111-203	N/A	N/A	N/A	*. Science **270**, 1791-1794 (1995).*
	patterned film	Templated liquid-phase	500-535	SiO_2/Si	675	N/A	*Nat. Commun*. **7**, 10502 (2016)
	film	Chemical beam epitaxy	550	N/A	N/A	N/A	*Appl. Phys. Lett*. **45**, 1234 (1984)
InP	film	MBE	450-650	InP (100)	N/A	N/A	*Appl. Phys. Lett*. **41**, 467 (1982)
	nanowire	MOCVD	420	InP (111)	570-730	N/A	*Nano Lett*. **12**, 5325−5330 (2012)
	nanowire	VLS	430-490	Ge (111)	N/A	N/A	*Nature Mater*. **3**, 769 (2004)
	nanowire	MOCVD	450-460	Si (111)	N/A	30 %	*Nano Lett*. **15**, 7189−7198 (2015)
	nanowire	MOCVD	750	InP (111)	200-500	3 %	*Nano Lett*. **17**, 6287-6294 (2017)
	nanowire	CVD	950	Si	43.6	N/A	*Nano Energy* **15**, 293-302 (2015)
InGaAs	nanowire	MOCVD	670	SiO_2/Si	1170	N/A	*Nature* **488**, 189 (2012)
	film	Migration-enhanced epitaxy	350	GaAs	2000	N/A	*J. Appl. Phys.* **67**, 589 (1990)
	nanostructure	Solution growth	111-203	N/A	N/A	N/A	*. Science **270**, 1791-1794 (1995).*
GaAs	nanowire		450	Si	N/A	N/A	*Nano Lett.* **16**, 4032−4039 (2016)
	films	MOCVD	650	Graphene	N/A	N/A	*Nature* **544**, 340 (2017)
	nanowire	MOCVD	790	Si (111)	10.3-67.5	N/A	*Nano Lett*. **12**, 4484−4489 (2012)
GaN	nanosheet	MOCVD	675	Graphene	N/A	N/A	*Nature Mater*. **15**, 1166 (2016)
	nanosheet	CVD	800	SiO_2/Si	N/A	N/A	*J. Am. Chem. Soc*. **141**, 104(2019)

SI Appendix, Section 1. Growth Process Nucleation Density vs. Temperature

In the TLP growth process, the nucleation and growth of InP from a supersaturated solution of P in In follows directly from the In-P phase diagram. Control of nucleation density is given due to the limited amount of phosphorus that can make it through the SiO_x cap, as when a nucleus is formed the growth of that crystal starves available phosphorus from the surrounding area by a diffusion-based "depletion zone." As PH_3 is cracked separately in our process, the nucleation density at a given temperature therefore depends on how much phosphorus can still get through the cap and on the width of this depletion zone. In prior work (*Chem. Mater.* **26**, 1340-1344 (2014)), it was determined that the density of InP nuclei can be expressed as the following equation:

$$N_{Total} = \frac{A}{h^2}\left(\frac{Fh^4}{D}\right)^{\alpha} \qquad (1)$$

In this equation, D is the diffusivity of phosphorus in indium, F is the flux of indium through the cap, h is the height of the indium, α (~0.88 for our system) is related to the number of atoms in a critical nucleus η, and A is a fitting parameter related to the capture cross section of phosphorus atoms for both nucleation on existing islands and as new domains. In SI Appendix Figure S3, the data shows that the nucleation rate increases linearly with 1/T and the crystal domain size decreases with 1/T. The diffusivity (*D*) of the phosphorus in liquid indium as a function of 1/T can be obtained from the literature (*Journal of Crystal Growth* **46** 55-58 (1979)) (SI Appendix Figure S3c). The data shows that *D* decreases with 1/T, indicating *D* is indeed the determining factor for nucleation density. From *D*(1/T), the value of α can be extracted ($\alpha = 0.88$), which is sensible and in agreement with the value previously reported in literature (*Chem. Mater*. **26**, 1340-1344 (2014)).

SI Appendix, Section 2. Electronic Measurement and Extraction Details

Hall Measurement Cross-Checking and Geometrical Error Estimation

For Hall measurements in the typical 4-point Van der Pauw geometry, a Hall voltage error is introduced due to influence of the forced current on the voltage measurement probes when contacts are larger than the idealized "point" configuration. With a square Hall pattern and triangular contacts, it is estimated that a value of $l_c/l_s = 1/6$ gives an error of approximately 15% in the final Hall voltage, leading to systematic error in the measurement of Hall mobility. In particular, the values of the resistivity correction factor and Hall resistance (and therefore mobility) correction values follow these expressions for a square geometry (Look, D. C., Electrical characterization of GaAs materials and devices. (Wiley, 1989)):

$$\frac{\Delta\rho}{\rho} \propto \frac{{l_c}^2}{{l_s}^2} \qquad \frac{\Delta R_H}{R_H} \propto \frac{l_c}{l_s} \qquad \text{(per contact)}$$

Errors from the original finite difference calculation referenced here were included in our mobility plots. With our device geometries designed to a ratio of ~0.16-0.17 as-patterned, our final error is ~15%. A 16% error was assumed for the plotted data based on an overestimate of contact overlap, though statistics on multiple measured devices (N = 10) also give a Std. error of 15.1%. In addition to geometrical error, cross-checking was performed to compare measurements from different tools and tools and rule out internal systematic error – while an Ecopia HMS-3000 Hall Effect tool was used for the presented data, resistivities extracted from Van der Pauw 4-point measurements were cross-checked and confirmed with an Agilent B1500 parameter analyzer, and reference mobility samples were confirmed on each tool prior to measurement. For all measurements, contact linearity was confirmed in the measurement range by the parameter analyzer, and the ratio of vertical to horizontal conductivity was minimized for accepted data to avoid misalignment error.

Transistor Contact Engineering

It should be noted that in this case contact resistance is a severe limiting factor for performance of these devices, as indicated by the significant roll-off of the I_D-V_G curve at high V_G. The contact resistance can be extracted from this structure by assuming the resistance at high V_G is dominated by the contacts, giving $R_{tot} \approx 2R_C$ at high V_G-V_T. Extracting the contact resistance for this transistor (See below for extraction details), we find that a relatively large R_C of approximately 44 kΩ-μm is present in our device, possibly due to the small contact area overlap present or the low-temperature contact anneal used to match the growth range. Utilizing the standard MOSFET equation and including contact resistance, the expression for I_D becomes:

$$I_D = \mu C_{ox} \frac{W}{L} (V_G - V_T - I_D R_C)(V_D - 2I_D R_C)$$

Using this expression and the I_D-V_G curve presented above yields a peak contact-resistance corrected mobility of 663 $cm^2\ V^{-1}\ s^{-1}$.

Transistor Contact Resistance Extraction and Effective Mobility Correction

For contact resistance extraction, a polynomial model was used in the high gate overdrive region of the $I_D V_G$ curve at low V_D (0.1V) for a given transistor device:

$$b_1 + \frac{b_2}{x} + \frac{b_3}{x^2} \qquad b_1 = 2R_C$$

As V_G goes to infinity, R_{Total} in the transistor approaches $2R_C$ as the channel resistance becomes negligible. However, in many cases the device will break down before the curve becomes sufficiently flat, so a fit of the decay above can be used. For the devices presented in Figure 4b, the following values were extracted:

	Value	Standard Error
$b_1 = 2R_C$	87666.32025	1097.52441
b_2	20739.40394	3221.6751
b_3	42435.74789	2104.6578

Accuracy of PL QY measurement

For PL QY measurement, a detailed overview of the precision of the measurement is provided in our previous work. The QY is calculated by dividing the CCD counts (N) by the product of pump power (P) and coupling factor (F), i.e.: QY = N / (F * P). The uncertainty or standard deviation of PL QY can be written as

$$\sigma_{QY} = QY\sqrt{\frac{\sigma_P^2}{P^2} + \frac{\sigma_N^2}{N^2} - 2\frac{2\sigma_{PN}}{PN} + \frac{\sigma_F^2}{F^2}}$$

where P and σ_P is the measured laser power and the corresponding uncertainty, N and σ_N is the measured CCD counts and corresponding uncertainty. Note that the laser power and the CCD counts are correlated, so their covariance must be considered. The variances σ_N, σ_P and covariance σ_{PN} can be extracted from control measurements. Combining all the components described above, the relative error in PL QY has been calculated to be $\sigma_{QY}/QY = 7\%$.