

Large-scale, heterogeneous integration of nanowire arrays for image sensor circuitry

Zhiyong Fan*^{†‡}, Johnny C. Ho*^{†‡}, Zachery A. Jacobson*[†], Haleh Razavi*, and Ali Javey*^{†§}

*Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 and [†]Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, CA 94720

Edited by George M. Whitesides, Harvard University, Cambridge, MA, and approved June 2, 2008 (received for review February 28, 2008)

We report large-scale integration of nanowires for heterogeneous, multifunctional circuitry that utilizes both the sensory and electronic functionalities of single crystalline nanomaterials. Highly ordered and parallel arrays of optically active CdSe nanowires and high-mobility Ge/Si nanowires are deterministically positioned on substrates, and configured as photodiodes and transistors, respectively. The nanowire sensors and electronic devices are then interfaced to enable an all-nanowire circuitry with on-chip integration, capable of detecting and amplifying an optical signal with high sensitivity and precision. Notably, the process is highly reproducible and scalable with a yield of $\approx 80\%$ functional circuits, therefore, enabling the fabrication of large arrays (i.e., 13×20) of nanowire photosensor circuitry with image-sensing functionality. The ability to interface nanowire sensors with integrated electronics on large scales and with high uniformity presents an important advance toward the integration of nanomaterials for sensor applications.

nanomaterials | printable electronics | devices | transistors | imager

Chemically derived, synthetic nanomaterials with low dimensionality and well defined atomic composition present a unique route toward miniaturization of electronic and sensor components while enhancing their performance and functionality (1–5). To date, a broad spectrum of single crystalline nanomaterials with tailored properties have been synthesized, and have been successfully demonstrated as the building blocks of various high-performance device elements, such as transistors (6–17), optical devices (18–20), sensors (21–26), energy-scavenging devices (27), and simple circuit structures (7, 17, 19, 28). These synthetic materials present a number of key advantages over their bulk counterparts. For instance, downscaling of the active sensing material to the nanoscale regime has been shown to enhance the sensitivity of chemical, biological, and optical sensors by orders of magnitude (21–26). To enable the implementation of nanosensors for various technological applications, on-chip integration with electronics is needed to enable automated and accurate processing of the signal. Here, we demonstrate an all-integrated, heterogeneous nanowire (NW) circuitry, capable of detecting and amplifying an optical signal with high sensitivity and responsivity. By implementing our recently developed contact printing technology (29, 30), large arrays of optically active CdSe NWs and high-mobility core/shell Ge/Si NWs are assembled at well defined locations on substrates, and configured as integrated sensor and electronic active components of an all-nanowire circuitry with image-sensing capability.

Results and Discussion

In this work, direct band gap CdSe NWs were used as a model system for the optical sensor elements, capable of detecting visible light with high sensitivity. CdSe- and CdS-based nanomaterials such as quantum dots and NWs have been extensively explored in the past, and their superb optical and opto-electrical properties have been reported in detail by various groups (31–33). Notably, NWs (for instance, in the case of ZnO NWs)

have been shown to be ideal materials for photodetection with significantly higher sensitivities than their bulk counterparts, arising from their high surface area-to-volume ratio that results in high density of surface states (21, 33). The surface states trap the photogenerated holes and, therefore, effectively increase the electron carrier lifetime that results in the enhancement of the photocurrent (21). To implement CdSe NWs as optical sensors, Schottky devices were fabricated by contacting the NWs with high work function Ni/Pd (5/45 nm) source (S) and drain (D) electrodes (Fig. 1A). NWs were grown intrinsically without any intentional doping by using the previously reported vapor-liquid-solid process (see *Methods*; 34), and as expected they exhibited *n*-type behavior (Fig. 1B) because of their surface Fermi level pinning. From photoluminescence measurements, a band gap of ≈ 1.76 eV was extracted (see [supporting information \(SI\) Fig. S1](#)), which is consistent with the reported bulk value, and is indicative of stoichiometric composition. The electrical characteristic of a representative CdSe NW Schottky device is shown in Fig. 1B. The device exhibits large dark resistance $R_{\text{dark}} \approx 140$ G Ω because of the Schottky barriers at the S/D interfaces that severely limit the carrier injection from the metal into the chemically intrinsic semiconductor NWs. On white light illumination (halogen light source, 4.4 mW/cm²), a drastic decrease of ≈ 100 times in the device resistance ($R_{\text{light}} \approx 2$ G Ω) is observed that is attributed to the efficient electron/hole photogeneration and field-induced carrier separation in CdSe NWs (Fig. 1A). The photocurrent gain in our NW devices is comparable to the best reported values in literature for physical vapor-deposited CdSe thin films. However, for such thin-film devices, the exact gain (ranging from 10 to 1,000 times for ≈ 80 mW/cm² illumination) is shown to highly depend on the annealing and deposition temperature conditions that effectively control the film stoichiometry, morphology, and crystallinity (35). In distinct contrast, NWs are single crystalline with controlled composition, and require only ambient temperature processing for their deposition (i.e., assembly) on substrates, making them highly compatible with a wide range of substrates, including plastics and papers.

To further characterize the CdSe NW photosensors, transient and illumination intensity-dependent measurements were performed. Time-resolved photoresponse measurements were conducted for multiple illumination cycles as depicted in Fig. 1C. Each photoresponse cycle consists of three transient regimes—a sharp rise ($\tau \approx 0.7$ sec), steady state, and sharp decay ($\tau \approx 0.7$ sec). We note that our time constants are larger than the best reported values for nanowires in the literature (21, 33). We attribute this

Author contributions: Z.F., J.C.H., Z.A.J., H.R., and A.J. designed research; Z.F., J.C.H., Z.A.J., and H.R. performed research; Z.F., J.C.H., Z.A.J., H.R., and A.J. analyzed data; and Z.F., J.C.H., Z.A.J., H.R., and A.J. wrote the paper.

The authors declare no conflict of interest.

This article is a PNAS Direct Submission.

[‡]Z.F. and J.C.H. contributed equally to this work.

[§]To whom correspondence should be addressed. E-mail: ajavey@eecs.berkeley.edu.

This article contains supporting information online at www.pnas.org/cgi/content/full/0801994105/DCSupplemental.

© 2008 by The National Academy of Sciences of the USA

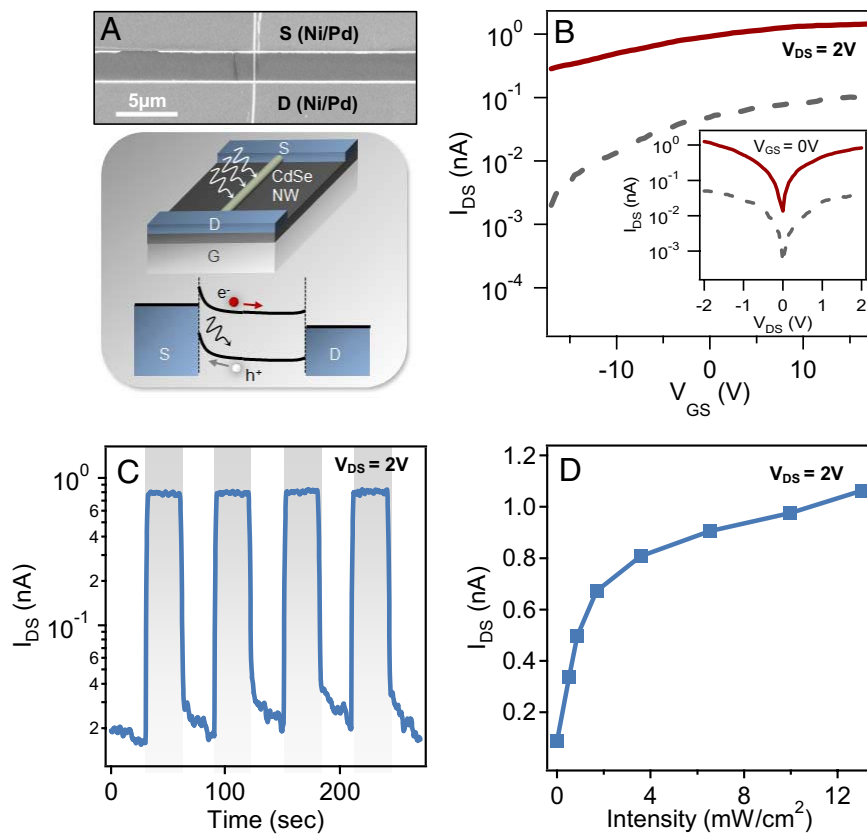


Fig. 1. Highly sensitive, direct band-gap NW photodiodes. (A) SEM (Top), schematic (Middle), and the band diagram (Bottom) of a CdSe NW photodetector with Ni/Pd Schottky S/D contacts. (B) I_{DS} - V_{GS} and I_{DS} - V_{DS} (Inset) curves of a representative CdSe NW device before (dashed, gray line) and after (solid, red line) white light illumination, exhibiting ≈ 100 times the current modulation. (C) Transient of a single CdSe NW device with an illumination intensity of $4.4 mW/cm^2$. (D) Illumination intensity-dependent measurements of a CdSe NW device, showing a nonlinear behavior.

to (i) the quality of our nanowires, which can be readily improved in the future through growth optimization, and (ii) the measurement setup. However, this response time is adequate for the purpose of this work, and in principle it can be drastically improved in the future, if desired. Importantly, a nearly identical response is observed for multiple cycles which demonstrates the robustness and reproducibility of the NW optical sensors. The illumination power dependence of the photoresponse is shown in Fig. 1D, exhibiting two distinct regimes with the transition intensity of $\approx 2 mW/cm^2$. This nonlinear photoresponse has also been reported in other NW photodetectors, and has been attributed to the charge-trapping and recombination processes due to the dominant surface states in the forbidden gap of NWs (35, 36).

Although the miniaturized nanosensor elements, such as the CdSe NW photodetectors shown here, provide high sensitivity to the environment with high spatial resolution, they are inherently limited to low signal amplitude (i.e., current), and therefore require an eventual signal amplification via electronic circuitry to enable effective data processing. To date, this important requirement has not yet been addressed. Here, we report direct, on-chip amplification of the nanosensor signal by using an all-NW circuitry without any external wiring. The schematic, SEM, and optical images of a fabricated all-nanowire circuit is shown in Fig. 2, consisting of three active device elements: (i) optical nanosensors (NSs) based on either a single or parallel arrays of multiple CdSe NWs, (ii) a high-resistance field-effect transistor (FET) (T1) based on parallel arrays of 1–5 Ge/Si core/shell NWs, and (iii) a low-resistance buffer FET (T2) with the channel consisting of parallel arrays of $\approx 2,000$ NWs. The

all-nanowire circuitry utilizes T1 to match the output impedance of the NS in a voltage divider configuration. Once the illumination-dependent NS current is translated into potential V_{G2} , the output current of T2 is modulated according to its transfer characteristics, resulting in ≈ 5 orders of magnitude amplification of the NS current signal.

To enable the successful fabrication of the all-integrated, heterogeneous NW circuitry, it is essential to assemble highly regular NW arrays with high uniformity at well defined locations on the substrate. Recently, we have developed a contact printing technology for direct transfer of highly ordered and aligned NW arrays on various receiver substrates with high reproducibility over large areas (29, 30). In this approach, a dense “lawn” of single crystalline NWs with controlled composition is first grown on a growth substrate by using the vapor–liquid–solid process, followed by the transfer of NWs to a receiver substrate by a directional sliding. Before the printing process, the receiver substrate is coated with a photolithographically patterned resist layer that enables for patterned NW assembly on resist removal in acetone. We incorporated this assembly approach for enabling the fabrication of the all-nanowire sensor circuitry. First, highly aligned CdSe and Ge/Si NW arrays were assembled at pre-defined locations on a Si/SiO₂ (50 nm, thermally grown) substrate by using a two-step printing process (see Methods). Ni/Pd S/D electrodes were then patterned on NW arrays followed by atomic layer deposition (ALD) of 8- to 9-nm-thick HfO₂ film as the high- κ gate dielectric. Finally, the HfO₂ layer was selectively etched in hydrofluoric acid at the bonding pads and vias, and the top gate electrodes (Ni/Pd) were patterned on Ge/Si NWs while simultaneously forming the vias between the two metal layers

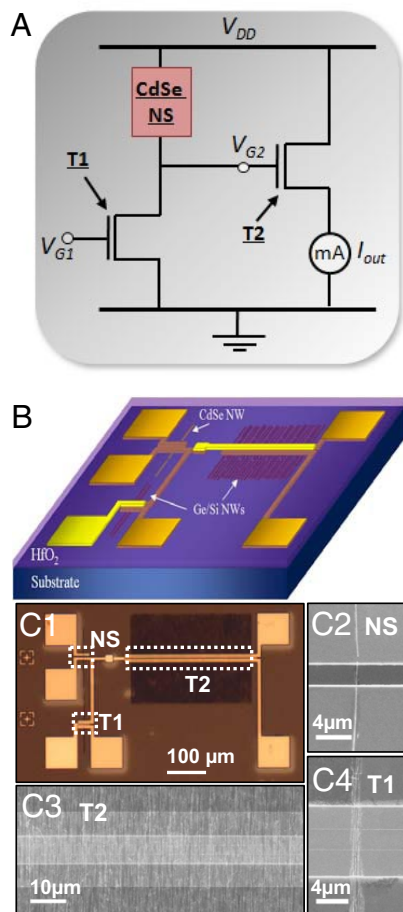


Fig. 2. Heterogeneous NW assembly for an all integrated, sensor circuitry. (A) Circuit diagram for the all-nanowire photodetector, with high-mobility Ge/Si NW FETs (T1 and T2) amplifying the photoresponse of a CdSe nanosensor. (B) Schematic of the all-nanowire optical sensor circuit based on ordered arrays of Ge/Si and CdSe NWs. (C1) An optical image of the fabricated NW circuitry, consisting of a CdSe nanosensor [NS (C2)] and two Ge/Si core/shell NW FETs [T2 and T1, (C3) and (C4)] with channel widths $\approx 300 \mu\text{m}$ and $1 \mu\text{m}$, respectively. Each device element within the circuit can be independently addressed for dynamics studies and circuit debugging.

(see *Methods*). Fig. 2C shows an optical microscopy image of a fabricated circuit and scanning electron microscopy (SEM) images of each individual component, clearly demonstrating the highly ordered NW positioning and the on-chip integration. The achieved NW alignment is highly desirable for high-performance and highly uniform transistor and sensor arrays. For transistors, a high degree of alignment, without NW crossing, is needed to reduce variation in gate electrostatics coupling and NW channel length, both of which directly affect the switching performance. Similarly, for CdSe optical sensors, the alignment is critical for uniform response of the devices, but also more uniquely to enable well defined polarized sensitivity that arises from the 1D nature of NWs (18). The polarization-dependent photoconduction measurements of single and parallel arrays of CdSe NWs are depicted in Fig. S2. In particular, near-identical polarization-dependent response is observed for various printed CdSe NWs with similar minima and maxima polarization angles, which further illustrates the highly aligned assembly of NWs by contact printing. This is in distinct contrast to the randomly aligned NWs assembled by the drop-casting method that show different polarized response depending on the orientation of the particular wire.

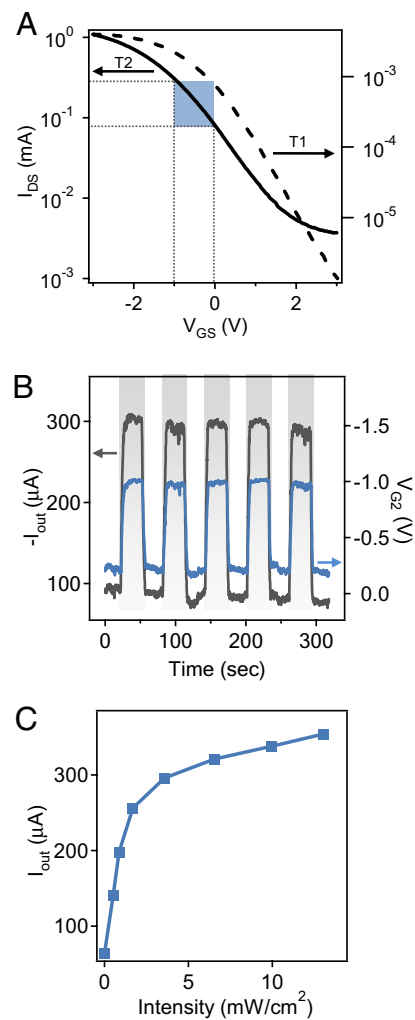


Fig. 3. All-integrated NW sensor circuitry. (A) Transfer characteristics of parallel array Ge/Si NW FETs with channel width of $\approx 1 \mu\text{m}$ (dashed line, T1) and $\approx 300 \mu\text{m}$ (solid line, T2) with $V_{DS} = 3\text{V}$. The blue box represents the active operation regime in which the photosensor circuit is being operated. (B) Circuit output current (blue curve) and voltage divider output voltage (gray curve) response to light illumination (4.4 mW/cm^2). (C) Light-intensity-dependent measurement of the circuit output current.

The all-nanowire photosensor circuits were measured at both the single-device component and circuit levels to characterize their operational performance. Fig. 3A shows the transfer characteristics of T1 and T2, both exhibiting clear *p*-type switching characteristics with $I_{ON} \approx 4 \mu\text{A}$ and 1 mA , respectively. Further detailed characterization of representative Ge/Si NWs FETs is presented in Fig. S3. In summary, the Ge/Si NW FETs showed minimal hysteresis ($< 200 \text{ mV}$) owing to the passivation from the environment (i.e., humidity) by the top gate stacks, and the high-quality gate dielectrics deposited by ALD (38). A hole mobility range of $\mu_p = 30\text{--}120 \text{ cm}^2/\text{V}\cdot\text{s}$ is extracted from the standard square law model (Fig. S3D). Although the highest μ_p of our NWs is comparable to that of Si *p*-metal oxide semiconductor FETs, the mobility is ≈ 7 times lower than the best reported value for Ge/Si NW FETs (9, 37). We attribute this to the nonideal high- κ /NW interfaces and/or non-ohmic metal contacts in our fabricated device structures.

Ge/Si NW FETs were found nonresponsive to white light illumination which guaranteed no undesired interference (see Fig. S4). For the circuit level operation, the operating bias, V_{DD} was maintained at -3V for all measurements. The gate electrode

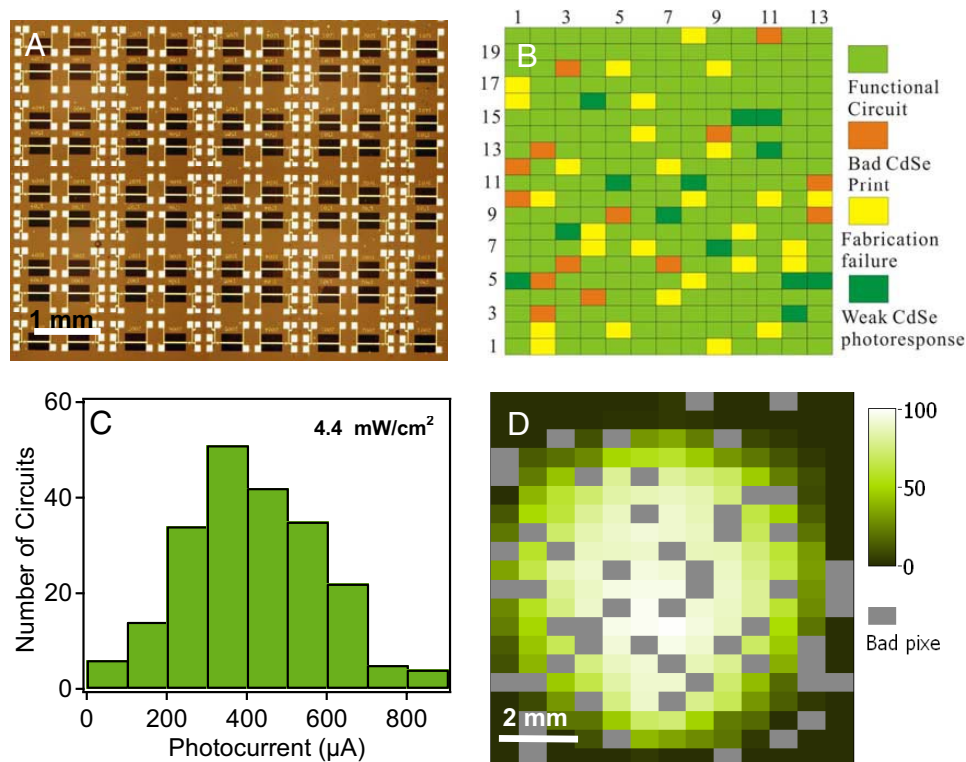


Fig. 4. Large-scale and heterogeneous integration of NWs for image sensing. (A) Optical image of an array of all-nanowire photodetector circuitry with each circuit element serving as an independently addressable pixel. (B) A defect analysis map showing the functional and defective NW photodetector circuit elements. (C) A histogram of the photocurrent for all functional circuit elements of the fabricated array. (D) An output response of the circuit array, imaging a circular light spot. The contrast represents the normalized photocurrent, with the gray pixels representing the defective sites (see *SI Text*).

for T1 was biased at $V_{G1} = 3V$ (corresponding to $R_{T1} = 1\text{--}2\text{ G}\Omega$) to match the output impedance of the CdSe NS. The output signal of a circuit for multiple white light illumination cycles (4.4 mW/cm^2) is depicted in Fig. 3B, showing average dark and light currents of $\approx 80\text{ }\mu\text{A}$ and $\approx 300\text{ }\mu\text{A}$, respectively. Importantly, this output current is quantitatively consistent with the value that is estimated based on the circuit layout and the electrical properties of the single-device components. The output current of the circuit can be estimated from the transfer characteristics of T2 and the output voltage of the voltage divider, which is also the input to T2. The output of the voltage divider, V_{G2} can be estimated as $V_{G2} = V_{DD} \times R_{T1}/(R_{T1} + R_{NS})$, corresponding to $V_{G2} \approx -0.02V$ and $-1.11V$ for dark and light ($R_{NS\text{-dark}} \approx 140\text{ G}\Omega$ and $R_{NS\text{-light}} \approx 2\text{ G}\Omega$; Fig. 1B) scenarios, respectively, which is in good agreement with the measurements (blue curve, Fig. 3B). The V_{G2} swing defines the operation regime of T2 as depicted in the transfer characteristics (Fig. 3A). This operation regime corresponds to an output current swing of $87\text{--}310\text{ }\mu\text{A}$, consistent with the measured values and the PSpice modeling (see Fig. S5).

The intensity-dependent photoresponse measurements were conducted as shown in Fig. 3C to further characterize the integrated circuits. The trend is nearly identical to the photoresponse of the single CdSe NW device (Fig. 1D), suggesting that the signal amplification by the circuit is nearly linear for the illumination intensity of $0\text{--}13\text{ mW/cm}^2$. The circuit level measurements demonstrate the successful operation of NW circuits for effective amplification of the small photocurrent generated by the NS elements.

To further demonstrate the versatility of our approach, we fabricated large arrays (i.e., 13×20) of the all-nanowire circuits on a chip (Fig. 4A), and measured the photoresponse of each individual circuit element. Rather than single CdSe NWs, parallel arrays of $5\text{--}10$ NWs were used as the active element of each

NS to enhance the yield and reduce the variation by taking advantage of the averaging effect (see Fig. S6). It was found that $\approx 80\%$ of the circuits demonstrated successful photoresponse operation as depicted in the failure analysis map (Fig. 4B). The functional circuits exhibited a mean photocurrent of $\approx 420\text{ }\mu\text{A}$ with a standard deviation of $\pm 165\text{ }\mu\text{A}$. The reasonably small circuit-to-circuit variation arises from the uniformity of the assembled nanowire arrays. The three major causes for circuit failure were (i) fabrication defects (i.e., poor metal lift-off and gate dielectric breakdown), (ii) failed CdSe printing, and (iii) weak photoresponse from CdSe NWs (i.e., defective NWs), which represent $\approx 10\%$, 5% , and 5% of the fabricated circuits accordingly. The high yield of the operational circuits with a high level of complexity proves the potential of the NW technology and our parallel array assembly approach for large-scale sensor and electronic integration. In the future, this yield can be further enhanced through NW synthesis and fabrication-processing optimization.

The large NW circuit matrix can readily function as an image sensor. To demonstrate this feasibility, as a proof of concept, a halogen light source was focused and projected onto the center of the matrix. The output current was measured for each individual working circuit and digitized into a $0\text{--}100$ scale with “0” and “100” representing the maximum and minimum measured intensity, respectively (see *SI Text*). Each of the circuits was regarded as a pixel and the measured intensity levels of the circuits were incorporated into a 2D plot to generate a contrast map shown in Fig. 4D. The contrast map clearly demonstrates the spatial intensity variation from the center to the outer edge of the circuit matrix, precisely matching the intensity profile of the projected light source, thus showing a preliminary imaging function with an all-nanowire circuit array. In future, significant downscaling of the pixel size can be achieved by reducing the

feature size (for instance, channel length and width) of the Ge/Si NW FETs and the metal interconnects.

In summary, the large-scale assembly of NWs for heterogeneous, sensor circuitry with on-chip integration was demonstrated. The sensory and electronic functionalities of NWs have been interfaced through heterogeneous integration of direct band gap CdSe NWs and high-mobility Ge/Si NWs. Active elements consisting of both single and parallel arrays of NWs were incorporated to enable the circuit operation, involving 5 orders of magnitude current amplification of the nanosensor's signal. Importantly, by using parallel arrays of NWs as the active component of each device, the reliability and uniformity was significantly enhanced, therefore, enabling a reliable large-scale integration path for the demonstration of an image sensor. In the future, the process can be expanded to other optically active NWs, which combined with the scaling of the fabricated devices may enable high-resolution and multicolor imaging. This work not only demonstrates the nanowire device integration at an unprecedented scale, but also illustrates and presents a system based on printed NW arrays that may enable a number of technological applications by using NWs as the building blocks.

Methods

Nanowire Growth. Ge/Si core/shell NW growth process can be found in ref. 9. CdSe nanowires were grown in a custom-made CVD system with a single zone, resistive heating furnace (Lindburg Blue), which accommodates one-inch diameter quartz tubes. Gold nanoparticles with 30-nm diameter were deposited on Si/SiO₂ substrates and served as catalysts for the vapor–liquid–solid growth process. Before the growth, 1.5 g of CdSe powder (Alfa Aesar, 99.999%) was placed in a quartz boat and loaded into the center of the heating zone in the furnace. Then, the growth substrate was placed at the downstream, ≈9.5 cm away from the center of the furnace. The nanowire growth was carried out with the furnace temperature (precursor tempera-

ture) at 700°C and 50 standard cubic centimeters per minute continuous flow of hydrogen. The system pressure was stabilized at 30 torr with a pressure controller and the growth was carried out for 1.5 h.

Nanowire Contact Printing. An alignment mark layer was first created on a Si/SiO₂ substrate. Then a layer of photoresist (Shipley 1805 diluted in propylene glycol monomethyl ether acetate with 1:3 volume ratio) was spin-coated on the substrate, and lithographically patterned to define printing channels for the CdSe nanowire assembly. The details of the printing process can be found in ref. 29. After CdSe nanowire printing, the photoresist was removed in acetone followed by a second printing step for Ge/Si nanowires by using an identical process flow.

Device Fabrication. After contact printing of CdSe and Ge/Si nanowires, source-drain contact electrodes were patterned with photolithography. Then Ni (5 nm)/Pd (45 nm) was evaporated with an electron beam evaporator followed by lift-off. HfO₂ high-κ gate dielectric film was then deposited by using an atomic layer deposition tool. In this process, tetrakis(dimethylamino) hafnium maintained at 110°C and water were used as the precursors. HfO₂ was deposited for 85 cycles (≈9 nm thick) at 140°C, with each cycle consisting of a 1-sec tetrakis(dimethylamino) hafnium precursor pulse, 20-sec nitrogen purge, 1-sec water vapor pulse, and 40-sec nitrogen purge. Thereafter, etching windows on source-drain bonding pads and the bridges (vias) between the Ge/Si transistors were photolithographically patterned, and the HfO₂ was chemically etched with 5% HF for 35 sec. Finally, Ni (5 nm)/Pd (45 nm) for the top metal gate electrodes of T1 and T2, and the vias were fabricated by photolithography, metallization, and lift-off.

ACKNOWLEDGMENTS. We thank A. M. Peczkalski for insightful discussions, and Professor M. Wu and Dr. K. Yu for help with optical measurements. All fabrication was performed in the Berkeley Microfabrication Laboratory. This work was supported by Defense Advanced Research Projects Agency/Microsystems Technology Office, Intel, and Materials Structures and Device Focus Center. The nanowire synthesis was supported by a Laboratory Directed Research and Development Project from Lawrence Berkeley National Laboratory. J.C.H. received a graduate fellowship from Intel Foundation.

- Lieber CM, Wang ZL (2007) Functional nanowires. *MRS Bull* 32:99–108.
- Lieber CM (2003) Nanoscale science and technology: Building a big future from small things. *MRS Bull* 28:486–491.
- Avouris, P. Chen J (2006) Nanotube electronics and optoelectronics. *Mater Today* 9:46–54.
- McEuen PL (2000) Single-wall carbon nanotubes. *Phys World* 13:31–36.
- Rogers JA (2007) Slice and dice, peel and stick: Emerging methods for nanostructure fabrication. *ACS Nano* 1:151–153.
- Bryllert T, Wernersson LE, Froberg LE, Samuelson L (2006) Vertical high-mobility wrap-gated InAs nanowire transistor. *IEEE Electron Device Lett* 27:323–325.
- Javey A, Nam S, Friedman RS, Yan H, Lieber CM (2007) Layer-by-layer assembly of nanowires for three-dimensional, multifunctional electronics. *Nano Lett* 7:773–777.
- Javey A, Guo J, Wang Q, Lundstrom M, Dai HJ (2003) Ballistic carbon nanotube transistors. *Nature* 424:654–657.
- Xiang J, et al. (2006) Ge/Si nanowire heterostructures on high-performance field-effect transistors. *Nature* 441:489–493.
- Ahn, J. H., et al. (2006) Heterogeneous three-dimensional electronics by use of printed semiconductor nanomaterials. *Science* 314:1754–1757.
- Chen ZH, et al. (2006) An integrated logic circuit assembled on a single carbon nanotube. *Science* 311:1735.
- Kang SJ, et al. (2007) Printed multilayer superstructures of aligned single-walled carbon nanotubes for electronic applications. *Nano Lett* 7:3343–3348.
- Kang SJ, et al. (2007) High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes. *Nature Nanotech* 2:230–236.
- Bachtold A, Hadley P, Nakanishi T, Dekker C (2001) Logic circuits with carbon nanotube transistors. *Science* 294:1317–1320.
- Wang D, Sheriff B, Heath JR (2006) Complementary symmetry silicon nanowire logic: Power-efficient inverters with gain. *Small* 2:1153–1158.
- Ju S, et al. (2007) Fabrication of fully transparent nanowire transistors for transparent and flexible electronics. *Nat Nanotech* 2:378–384.
- Friedman RS, McAlpine MC, Ricketts DS, Ham D, Lieber CM (2005) High-speed integrated nanowire circuits. *Nature* 434:1085.
- Wang J, Gudiksen MS, Duan X, Cui Y, Lieber CM (2001) Highly polarized photoluminescence and photodetection from single indium phosphide nanowires. *Science* 293:1455–1457.
- Tian B, et al. (2007) Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature* 449:885–889.
- Lewis NS (2007) Toward cost-effective solar energy use. *Science* 315:798–801.
- Soci C, et al. (2007) ZnO nanowire UV photodetectors with high internal gain. *Nano Lett* 7:1003–1009.
- Cui Y, Wei Q, Park H, Lieber CM (2001) Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. *Science* 293:1289–1292.
- Patolsky F, et al. (2006) Detection, stimulation, and inhibition of neuronal signals with high-density nanowire transistor arrays. *Science* 313:1100–1104.
- McAlpine MC, Ahmad H, Wang D, Heath JR (2007) Highly ordered nanowire arrays on plastic substrates for ultrasensitive flexible chemical sensors. *Nat Mater* 6:379–384.
- Zhang DH, et al. (2004) Detection of NO₂ down to ppb levels using individual and multiple In₂O₃ nanowire devices. *Nano Lett* 4:1919–1924.
- Stern E, et al. (2007) Label-free immunodetection with CMOS-compatible semiconducting nanowires. *Nature* 445:519–522.
- Wang ZL, Song J (2006) Piezoelectric nanogenerators based on zinc oxide nanowire arrays. *Science* 312:242–246.
- Ju S, et al. (2008) Transparent active matrix organic light-emitting diode displays driven by nanowire transistor circuitry. *Nano Lett* 8:997–1004.
- Fan Z, et al. (2008) Wafer-scale assembly of highly ordered semiconductor nanowire arrays by contact printing. *Nano Lett* 8:20–25.
- Yerushalmi R, Jacobson ZA, Ho JC, Fan Z, Javey A (2007) Large scale, highly ordered assembly of nanowire parallel arrays by differential roll printing. *Appl Phys Lett* 91:203104.
- Chan EM, Mathies RA, Alivisatos AP (2003) Size-controlled growth of CdSe nanocrystals in microfluidic reactors. *Nano Lett* 3:199–201.
- Gudiksen MS, Maher KN, Ouyang L, Park H (2005) Electroluminescence from a single-nanocrystal transistor. *Nano Lett* 5:2257–2261.
- Jie JS, et al. (2006) Photoconductive characteristics of single-crystal CdS nanoribbons. *Nano Lett* 6:1887–1892.
- Ma C, Wang ZL (2005) Road map for the controlled synthesis of cdse nanowires, nanobelts, and nanosaws—A step towards nanomanufacturing. *Adv Mater* 17:2635–2639.
- Raturi AK, Thankaraj R, Sharma AK, Tripathi BB, Agnihotri OP (1982) Structural, optical, and photoconducting properties of sprayed CdSe Films. *Thin Solid Films* 91:55–64.
- Rose A (1963) *Concepts in Photoconductivity and Allied Problems* (Interscience, New York).
- Hu Y, Xiang J, Liang G, Yan H, Lieber CM (2008) Sub-100 nanometer channel length Ge/Si nanowire transistors with potential for 2 THz switching speed. *Nano Lett* 8:925–930.
- Javey A, et al. (2002) High-κ dielectrics for advanced carbon nanotube transistors and logic. *Nat Mater* 1:241–246.

Supporting Information

Fan *et al.* 10.1073/pnas.0801994105

SI Text

Polarization-Dependent Photoconduction. Because of the 1D feature of semiconductor nanowires, they demonstrate unique polarized photoconduction properties as reported for single NW devices (1). In this work, polarization-dependent photoconduction was measured for contact-printed (highly aligned) and drop-casted (random orientation) CdSe nanowires in both single NW and parallel array configurations. A randomly polarized 10 mW He-Ne ($\lambda = 633$ nm) laser was used as the light source in conjunction with a linear polarizer. By rotating the polarizer, the polarization angle of the incident light was tuned from 0 to 180° with respect to the edge of the source/drain electrodes. **Supporting information (SI) Fig. S2 A and B** shows the polarized photoconduction of single CdSe NW devices made by contact printing and drop casting of NWs, respectively. Although the contact-printed NW devices exhibit near-identical response with the photocurrent minimum at 90° and maxima at 0 and 180° polarization (angle in respect to the normal of S/D electrodes), the drop-casted (random orientation) NW devices exhibit a nonuniform response with a large device-to-device variation in their minima and maxima polarization angles. This result illustrates the highly oriented nanowire assembly achieved by the contact-printing process, in clear contrast to the random alignment obtained from drop casting of nanowires on substrates. Furthermore, polarized photoconduction measurements were conducted on parallel arrays of nanowires assembled by contact printing. As shown in **Fig. S2C**, the devices exhibit a minimum photocurrent at 90° and maxima at 0 and 180°, once again illustrating the high degree of alignment attained by the contact printing process.

Electrical Characterization of Ge/Si NW FETs. Low- and high-bias transfer characteristics of a single Ge/Si NW FET (top gated, 8–9 nm HfO₂ gate dielectric, $d \approx 30$ nm, $L \approx 3$ μ m) is shown in **Fig. S3 A and B** for backward and forward gate voltage-sweeping directions. The transistors exhibit minimal hysteresis. From the transfer characteristics, the field-effect mobility of holes was obtained by using the square law model. The gate capacitance, $C = 3.2 \times 10^{-15}$ F, was obtained from simulation by using version 4.0.1 of Finite Element Method Magnetics software. In the low-bias linear-triode region (i.e., $V_{DS} = 10$ mV) the hole mobility, μ_h can be deduced from

$$\mu_h = \frac{g_m L^2}{V_{DS} C},$$

where g_m is the transconductance, $g_m = dI/dV_{GS}|_{V_{DS}}$. A plot of mobility as a function of gate voltage is shown in **Fig. S3D**, illustrating a peak mobility of ≈ 100 cm²/V·s for this device. The mobility range for the studied NW devices was 30–120 cm²/V·s with a peak transconductance range (normalized by diameter) of 100–400 S/m. In the future, key transistor metrics, such as transconductance, can be improved by downscaling of the channel length and gate dielectric thickness (2–4).

SPICE Modeling. After single-device component measurements, Pspice (OrCAD Version 9.1) modeling was carried out to simulate the circuit output performance (**Fig. S5**). The simulation used the previously mentioned values (in the text) for resistance of NS and T1. For T2, PMOS model 1 was used with $K_p = 1.235 \times 10^{-4}$ F·cm⁻²(V·s)⁻¹ and $V_T = 1.13$ V. The simulation output is shown in **Fig. S5B**. Interestingly, the simulation results match well with the experimental data.

Sensor Circuitry with Parallel Arrays of CdSe NWs. To improve the uniformity, parallel arrays of CdSe NWs (5–10 NWs) were printed as light sensor elements for the large matrix fabrication as shown in **Fig. S6A**. **Fig. S6B** represents the time domain photoresponse of the CdSe NWs, demonstrating ≈ 100 pA dark current and ≈ 8 nA photocurrent with an illumination intensity of 4.4 mW/cm² and $V_{DS} = 3$ V. The output current of the circuit is shown in **Fig. S6C**, showing ≈ 5 orders of magnitude current amplification by the all-NW circuitry.

Image Construction with Sensor Circuit Array. To demonstrate the image-sensing function with the nanowire circuit array, a halogen light spot (diameter: ≈ 6 mm, peak intensity at the center: ≈ 4 mW/cm²) from a microscope on the probe station was projected at the center of the circuit array and the current output (I_{out}) from each circuit was measured pixel by pixel.

The measured current from each circuit pixel was digitized to an integer (Z) between 0 and 100 according the following equation:

$$Z = \text{Integer} \left(100 \times \frac{I_{out} - I_{min}}{I_{max} - I_{min}} \right)$$

where I_{max} and I_{min} correspond to the light current at 4 mW/cm² illumination and the dark current, respectively, which were measured for each circuit during a calibration step before the image-sensing experiment. Eventually, a 13×20 intensity matrix was formed from the Z values with each circuit corresponding to a single pixel (**Fig. 4D**).

1. Wang J, Gudixsen MS, Duan X, Cui Y, Lieber CM (2001) Highly polarized photoluminescence and photodetection from single indium phosphide nanowires. *Science* 293:1455–1457.
2. Xiang J, *et al.* (2006) Ge/Si nanowire heterostructures on high-performance field-effect transistors. *Nature* 441:489–493.

3. Hu Y, Xiang J, Liang G, Yan H, Lieber CM (2008) Sub-100 nanometer channel length Ge/Si nanowire transistors with potential for 2 THz switching speed. *Nano Lett* 8:925–930.
4. Javey A, *et al.* (2002) High-k dielectrics for advanced carbon nanotube transistors and logic. *Nat Mater* 1:241–246.

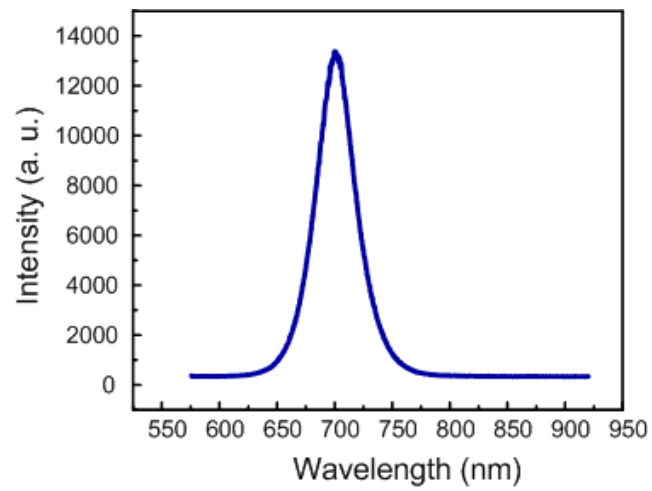


Fig. S1. A representative photoluminescence of a single CdSe NW ($d \approx 60$ nm), excited with a 1-mW green laser (532 nm) at room temperature. The extracted band gap is ≈ 1.76 eV (peak intensity ≈ 704 nm) which is consistent with the reported bulk value.

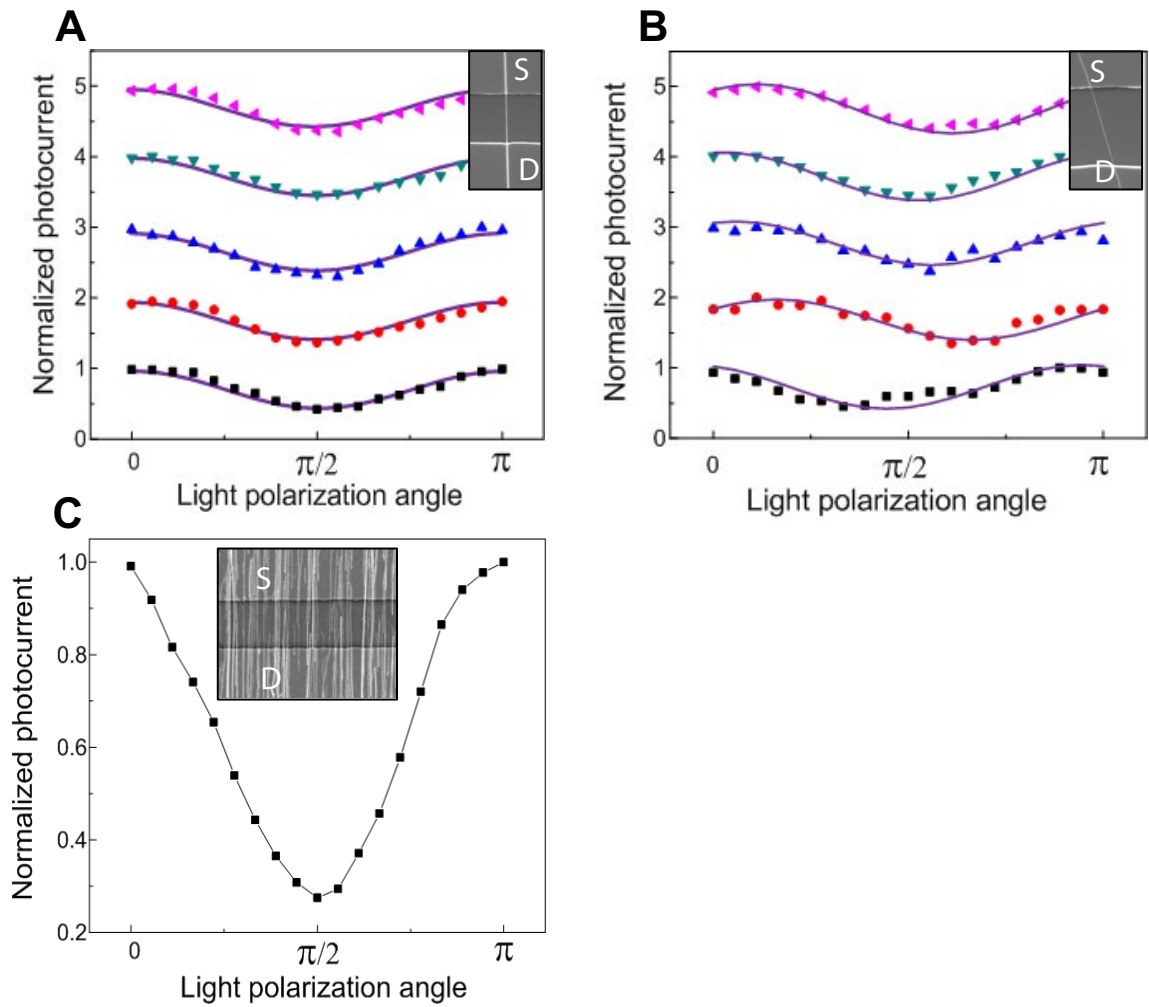


Fig. S2. Polarization-dependent photoconduction measurement for five single CdSe nanowires assembled by contact printing (*A*), five randomly orientated single CdSe nanowires assembled by drop casting (*B*), and parallel arrays of aligned CdSe NWs (≈ 40 NW) assembled by contact printing (*C*). (*Insets*) Optical images of representative devices. The curves in *A* and *B* have been shifted by units of 1 in the normalized photocurrent axis for clarity.

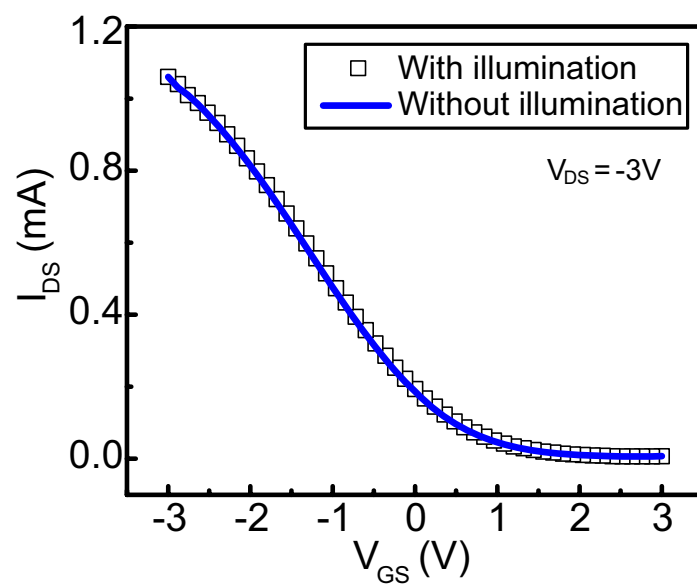


Fig. S4. Transfer characteristics of a parallel array Ge/Si nanowire transistor T2 obtained with and without illumination (4 mW/cm²). It can be clearly seen that Ge/Si nanowire FETs do not respond to the visible light, which confirms that the photoresponse of the circuits originates from CdSe NS elements.

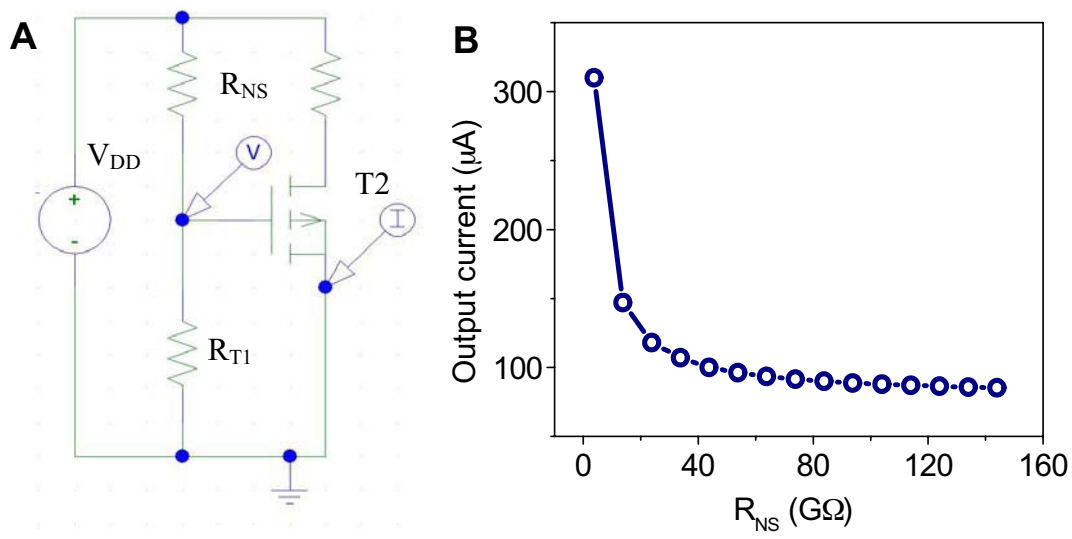


Fig. S5. PSpice modeling for circuit level performance evaluation. (A) Equivalent circuit used for PSpice modeling. (B) Modeled output current versus CdSe NW sensor resistance.

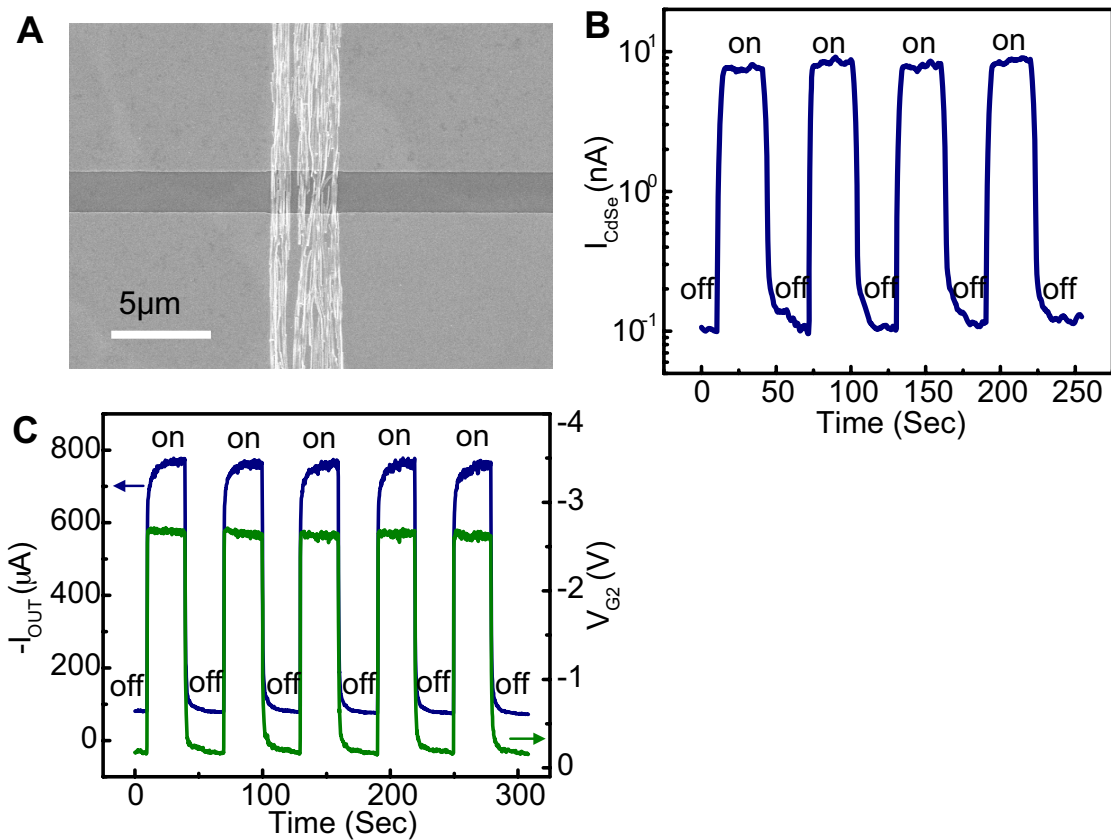


Fig. S6. SEM image of a parallel array CdSe NW device used for light sensing of the image sensor array (A) (Fig. 4), and its time domain photoresponse (B). (C) Output current (blue curve) and voltage divider output voltage (green curve) dynamic response to visible light illumination.