effective hole mobilities extracted for the temperature range 77–300 K show no temperature dependence indicating that this parameter is critically limited by the grain boundary in the Te films. Therefore, the reported p-type Te films together with the mature low-temperature processed n-type semiconductors may offer a potential solution for realizing high performance large area flexible CMOS platforms. To illustrate the potential of the presented concept, Javey and co-workers show the realization of various flexible logic gates and computational circuits, such as an inverter, NAND gate (Fig. 1), full adder and multiplier composed of dozens of transistors through conventional semiconductor processing[9]. These demonstrations were not possible with other emerging p-type candidates. Furthermore, the authors construct monolithic three-dimensional (3D) integrated circuits and back-end-of-line electronics achieving high density integration.

In the future, more feasible strategies enabling the realization of improved flexible complementary ICs will be needed for even higher integration density, better device-to-device uniformity, high operating speed and low power consumption. Currently, the deposition of Te, which takes place at –80 °C, is not industrially compatible. However, this work clearly indicates that the approach of employing thermally evaporated Te films is beneficial in terms of providing sufficient electrical performance to match the available n-type semiconductors. In addition, existing facilities for fabricating conventional silicon-based electronics can be utilized with high reliability in batch manufacturing, which allows the realization of complex computational circuits and monolithic 3D integrated circuits based on CMOS technology with minimized additional costs. For tellurium, to qualify as a promising p-type material, further studies should focus on ensuring higher quality (for example, crystallinity, domain size and impurities) of thermally evaporated Te thin films and better CMOS compatibility of the deposition process (for example, substrate temperature). If these requirements can be met, this approach could accelerate the coming of the Internet of Things world connected by energy-efficient flexible 3D electronics. □

Seungjun Chung[1] and Takhee Lee[2]
[1]*Photo-Electronic Hybrids Research Center, Korea Institute of Science and Technology, Seoul, Korea.*
[2]*Department of Physics and Astronomy, Seoul National University, Seoul, Korea.*
e-mail: seungjun@kist.re.kr; tlee@snu.ac.kr

Published online: 16 December 2019
https://doi.org/10.1038/s41565-019-0596-6

References

1. Myny, K. *Nat. Electron.* **1**, 30–39 (2018).
2. Hussain, A. M. & Hussain, M. M. *Adv. Mater.* **28**, 4219–4249 (2016).
3. Tang, J. et al. *Nat. Electron.* **1**, 191–196 (2018).
4. Park, J. W., Kang, B. H. & Kim, H. J. *Adv. Func. Mater.* https://doi.org/10.1002/adfm.201904632 (2019).
5. Kim, Y.-H. et al. *Nature* **489**, 128–132 (2012).
6. Wang, Z., Nayak, P. K., Caraveo-Frescas, J. A. & Alshareef, H. N. *Adv. Mater.* **28**, 3831–3892 (2016).
7. Manzeli, S., Ovchinnikov, D., Pasquier, D., Yazyev, O. V. & Kis, A. *Nat. Rev. Mater.* **2**, 17033 (2017).
8. Giri, G. et al. *Nature* **480**, 504–508 (2011).
9. Zhao, C. et al. *Nat. Nanotechnol.* https://doi.org/10.1038/s41565-019-0585-9 (2019).
10. Wang, Y. et al. *Nat. Electron.* **1**, 228–236 (2018).