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Analysis of the interface characteristics of CVD-grown monolayer MoS_2 by noise measurements

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Abstract

We investigated the current–voltage and noise characteristics of two-dimensional (2D) monolayer molybdenum disulfide (MoS_2) synthesized by chemical vapor deposition (CVD). A large number of trap states were produced during the CVD process of synthesizing MoS_2, resulting in a disordered monolayer MoS_2 system. The interface trap density between CVD-grown MoS_2 and silicon dioxide was extracted from the McWhorter surface noise model. Notably, generation–recombination noise which is attributed to charge trap states was observed at the low carrier density regime. The relation between the temperature and resistance following the power law of a 2D inverted-random void model supports the idea that disordered CVD-grown monolayer MoS_2 can be analyzed using a percolation theory. This study can offer a viewpoint to interpret synthesized low-dimensional materials as highly disordered systems.

Supplementary material for this article is available online

Keywords: transition metal dichalcogenides, molybdenum disulphide, electrical noise, percolation behavior, disordered system, chemical vapor deposition

(Some figures may appear in colour only in the online journal)

1. Introduction

Two-dimensional (2D) transition metal dichalcogenides (TMDCs) composed of a single atomic layer have been extensively studied in recent years [1–4]. Among them, monolayer molybdenum disulfide (MoS_2) has shown a variety of interesting features, such as good electrical mobility, photosensitivity, and high quantum yield [5–7]. In this context, synthesis methods such as chemical vapor deposition (CVD) allows the growth of large-area, uniform, monolayer MoS_2 films which can be used in various ultra-thin optical and electrical device applications [8–10]. However, a number of defects, such as sulfur vacancies and dielectric impurities, are created during the synthesis process [11, 12]. These defects which can work as trap states affect the transport properties of CVD-grown MoS_2 based field-effect transistors (FETs).

When atomically thin 2D TMDC films are used as active channels in FET devices, the charge carriers are vulnerable to the defects inside the TMDC materials and at the dielectric interface. The interface properties between the TMDC film and underlying dielectric layer play an important role in determining the electrical performance because of their extremely high surface to volume ratio [6, 13]. Therefore, scrutinizing the interface properties is highly desirable for

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understanding the charge transport behavior in 2D TMDC materials.

In this regard, low-frequency noise (LFN) or $1/f$ noise can be used to investigate the interface properties of CVD-grown monolayer TMDC materials [14–17]. $1/f$ noise, which indicates the decreasing electrical noise power as frequency increases, has been widely reported in various systems [18–20]. The electrical noise analysis on mechanically exfoliated MoS_2 flakes or CVD-grown monolayer MoS_2 films has been reported [21–24], but the relation between the charge transport and the electrical noise behavior originating from interface properties of CVD-grown monolayer MoS_2 system requires further study.

In this work, we report on the interface characteristics of CVD-grown monolayer MoS_2 studied by the electrical noise measurements. The current–voltage and noise characteristics were measured under various bias conditions in vacuum and in a temperature range from 80 K to room temperature. The charge trap density was extracted from the McWhorter surface noise model. In addition, the relation between the relative noise and resistance followed the power law of the percolation behavior and was analyzed with the 2D inverted random void (IRV) model.

2. Experimental details

2.1. Synthesis of monolayer MoS_2

The monolayer MoS_2 was synthesized on a SiO_2/Si substrate by a CVD system (Teraleader Co., Korea). The monolayer MoS_2 domains were grown directly on the Si wafer with a thermally grown 270 nm-thick SiO_2 layer. One boat with sulfur powder and the other boat with MoO_3 powder were placed upstream and around the middle of the tube, respectively. The SiO_2 substrates with pre-deposited marker array were used for designing electrodes via an electron-beam lithography system. The detailed synthesis process of monolayer MoS_2 has previously been explained [9].

2.2. Device fabrication process

After designing the contact electrodes by an electron beam lithography system, the source and drain electrodes were deposited with Au (50 nm)/Ti (5 nm) layers by an electron beam evaporator with a deposition rate of $\sim$0.2 Å s^{-1} at a pressure of $\sim10^{-7}$ Torr. Figure 1(a) shows the optical image of a FET device made with CVD-grown single-grain monolayer MoS_2. The dark violet triangular shapes are the CVD-grown monolayer MoS_2. To exclude the possible electrical degradation arising from the grain boundaries, a single-grain CVD-grown MoS_2 domain was used in this study [10, 25, 26]. The inset in this figure shows a schematic of the MoS_2 FET device structure composed of Ti/Au as the source and drain electrodes, heavily doped p-type silicon (Si) as the gate electrode, and thermally grown 270 nm thick SiO_2 as the gate dielectric. To verify the number of layers of the CVD-grown MoS_2 domains, Raman and photoluminescence (PL) spectra were acquired (figure 1(b)). The Raman spectra showed two peaks near 384.2 cm^{-1} and 405.2 cm^{-1}, which represent the in-plane E^1_{2g} and the out-of-plane A_{1g} vibrations, respectively [27]. In addition, a strong A1 peak ($\sim$1.83 eV) was observed in the PL spectra. The values of the frequency difference between the two Raman spectra peaks ($\sim$21 cm^{-1}) and the prominent A1 peak in the PL spectra strongly support that these CVD-grown MoS_2 domains are monolayer [28, 29].

2.3. Current–voltage (I–V) characteristics

The electrical properties of the monolayer MoS_2 FETs were measured in the dark in a vacuum ($\sim10^{-3}$ Torr) using a semiconductor parameter analyzer (Keithley 4200, USA). Before the measurement, the MoS_2 FETs were placed on a heating stage at 400 K in a vacuum for 16 h to remove the adsorbates from the MoS_2 surface, such as water, oxygen molecules, and polymer residue. The surface adsorbates could induce charge trapping states, which can result in hysteresis in the transfer curves (drain current *versus* source–gate voltage, $I_{DS}-V_{GS}$) of the MoS_2 FETs [30]. No $I_{DS}-V_{GS}$ hysteresis was observed after the heating process, which indicates the effect of surface adsorbates was negligible in this measurement (online supplementary figure S1, available at stacks.iop.org/NANO/28/145702/mmedia).

2.4. Electrical noise characteristics

The power spectral density (S_I) was measured using a spectrum analyzer (Stanford Research SR780, USA) and ground-isolated 16-bit analog-digital converter (ADC). To amplify the noise signal, a battery-powered low-noise current amplifier (Ithaco1211, USA) was used. A 16-bit digital-analog converter (DAC) and a digital multimeter (Agilent 34401 A, USA) were used to apply bias and to obtain the average electric current, respectively [17].

3. Results and discussion

The $I_{DS}-V_{GS}$ characteristics (figure 1(c)) exhibited typical n-type semiconductor behavior. The field-effect mobility and on/off current ratio of the monolayer MoS_2 FETs at room temperature were found to be $\sim$5.5 $cm^2\,V\,s^{-1}$ and $\sim10^6$, respectively. The output characteristics (drain current *versus* source–drain bias, $I_{DS}-V_{DS}$) are displayed in the inset of figure 1(c). Figure 1(d) shows the $I_{DS}-V_{GS}$ curves measured in a temperature range from 80 K–300 K at a fixed V_{DS} of 0.5 V. The same transfer characteristics on the linear scale are also included in the inset. The I_{DS} decreased with decreasing temperature, indicating that the amount of thermally activated charges reduced as the temperature decreased. The fabricated CVD-grown monolayer MoS_2 FETs showed good electrical characteristics comparing to the previously reported results [9, 21–24].

The relative noise (S_I/I^2) measured at V_{DS} ranging from 0.5 to 2.5 V and at V_{GS} ranging from −30 to 40 V showed

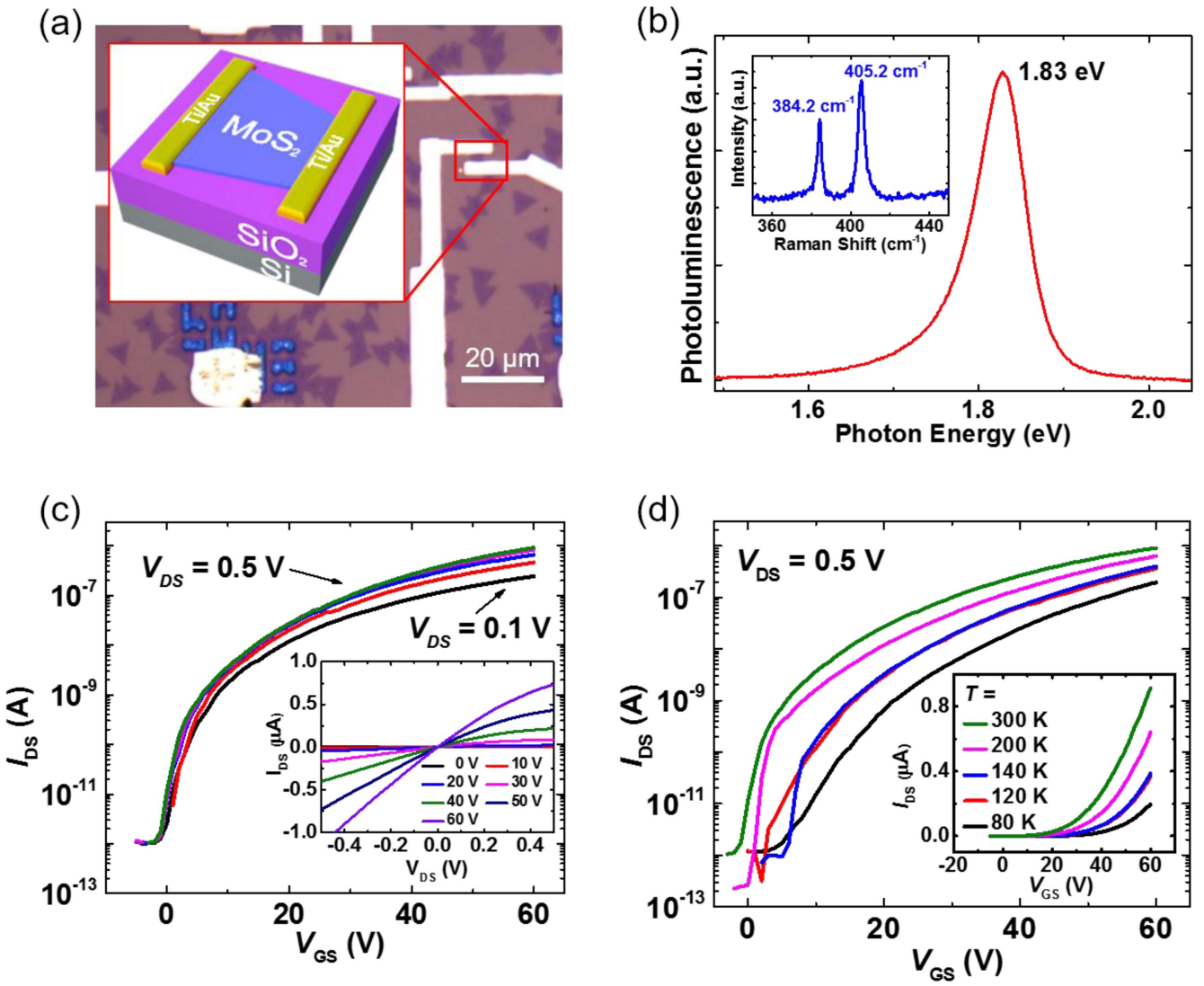

Figure 1. (a) Optical image showing a CVD-grown monolayer MoS_2 FET. The inset shows the schematics of the device. (b) Raman and PL spectra of a CVD-grown monolayer MoS_2. (c), (d) Representative electrical characteristics of the CVD-grown monolayer MoS_2 FET. (c) $I_{DS}-V_{DS}$ curves measured for different gate voltages at room temperature. (d) $I_{DS}-V_{GS}$ curves measured at a fixed $V_{DS} = 0.5$ V for various temperatures.

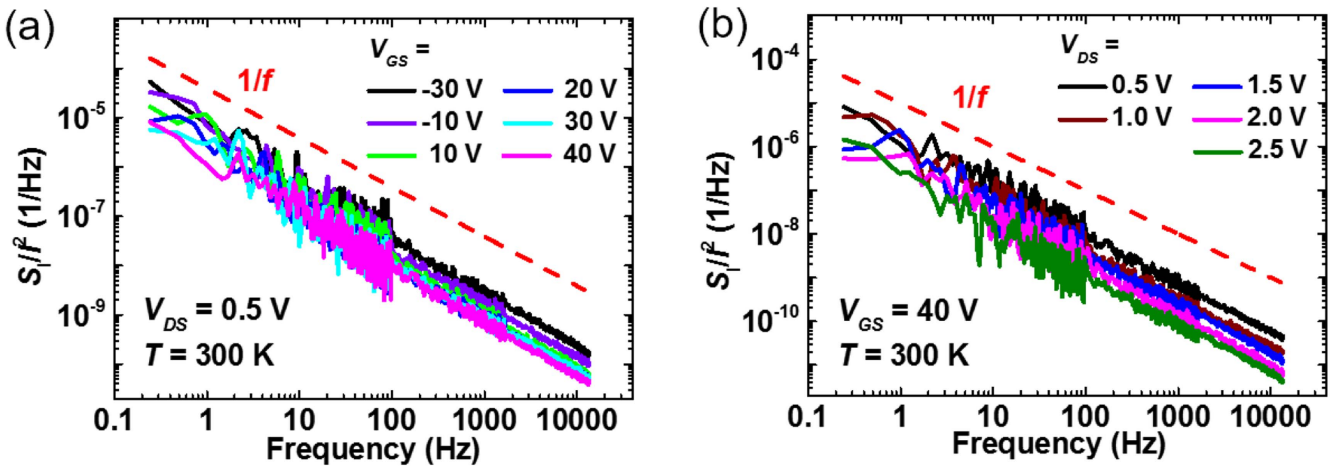

Figure 2. Relative noise of a CVD-grown monolayer MoS_2 at 300 K for (a) different gate voltages at a fixed $V_{DS} = 0.5$ V and (b) different source–drain voltages at a fixed $V_{GS} = 40$ V.

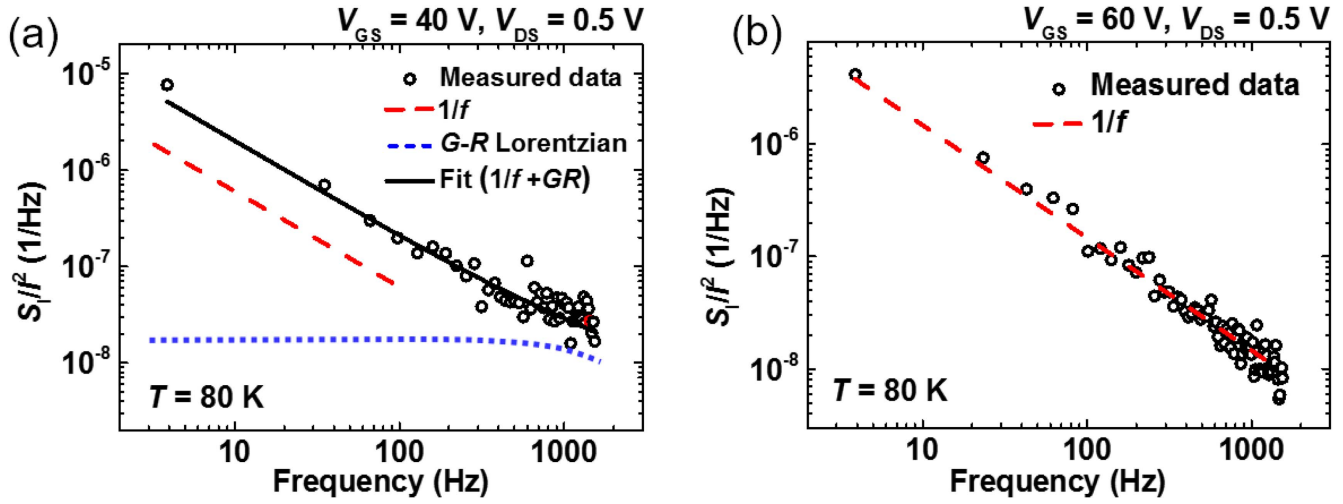

Figure 3. (a) Relative noise of a CVD-grown monolayer MoS_2 FETs at (a) $V_{GS} = 40$ V and (b) $V_{GS} = 60$ V at low temperature (80 K).

typical flicker noise (1/f) behaviors at low frequency regime (figures 2(a) and (b)). Similar noise characteristics have been observed for mechanically exfoliated monolayer MoS_2 flakes [21, 22]. Note that the power spectral density shows the amount of resistance (or current) fluctuation from the stationary state in a microscopic level which is averaged out in a macroscopic level [31]. In general, two theories have been proposed to explain the physical origin of the $1/f$ noise behavior; one is the carrier number fluctuation and the other is the mobility fluctuation [32]. In particular, the McWhorter carrier number fluctuation model (or surface noise model) explains the origin of $1/f$ noise as the carrier number fluctuation [19, 32, 33]. From the McWhorter carrier number fluctuation model, the trapping and detrapping of the charge carriers leads to the current (or resistance) fluctuation. Because the charge trapping and detrapping will be important at the interface of atomically thin CVD-grown monolayer MoS_2 films, the McWhorter model can be applied to CVD-grown monolayer MoS_2 [22]. According to this model, the contribution of the channel and contacts to the relative noise for the estimation of the charge trap density can be expressed by following equation [22, 32]

$$\frac{S_I}{I_{DS}^2} = \frac{S_{ch}}{R_{ch}^2}\frac{R_{ch}^2}{(R_{ch}+R_c)^2} + \frac{S_c}{R_c^2}\frac{R_c^2}{(R_{ch}+R_c)^2}, \quad (1)$$

where S_{ch}, S_c, R_{ch} and R_c denote the noise from the channel, noise from the contact, resistance of the channel, and resistance of the contact, respectively. When a large enough V_{GS} is applied, the contribution of the channel resistance can be ignored (online supplementary figure S2). So, from the total resistance calculated from Ohm's law, R_c and R_{ch} can be calculated. And, the relative noise can be described by

$$\frac{S_{ch}}{R_{ch}^2} = \frac{k_B T N_t}{\gamma f W L n_s^2}, \quad (2)$$

where k_B, T, n_s, γ, f, W, L, and N_t denote the Boltzmann constant, temperature, carrier density, tunneling parameter, frequency, channel width, channel length, and charge trap density, respectively [34]. The charge trap density N_t value was extracted from equations (1) and (2) to be $\sim 2 \times 10^{21}\,eV^{-1}cm^{-3}$ at 300 K. The N_t value was approximately two orders of magnitude higher than the reported values for mechanically exfoliated MoS_2 devices [22]. The larger charge trap density in CVD-grown monolayer MoS_2 indicates the creation of a large number of trap states during the synthesis process. These trap states can originate from the structural defects or sulfur vacancies generated during the harsh CVD synthesis process at high temperature (~700 °C) and low pressure (~10 Torr).

For further investigation of the trap states under low-frequency regime, the relative noise was measured at $V_{GS} = 40$, 50, and 60 V at low temperature (80 K). In general, the LFN can be expressed as a sum of $1/f$ noise and a series of Lorentzian curves (equation (3)). Especially, the generation and recombination (G–R) noise appears when a certain type of trap corresponding to certain frequencies dominates [20].

$$S_I(f) \cong \frac{1}{f} + \sum_{i=1}^{N} \frac{1}{1+\left(\frac{f}{f_{0i}}\right)^2} \quad \text{with} \quad f_{0i} = \frac{1}{2\pi\tau_i}, \quad (3)$$

where f_{0i}, τ_i, and N denote the cut-off frequency, lifetime of the carriers of the G–R noise, and the number of trap sites, respectively. Figure 3(a) shows the relative noise, $1/f$ noise, Lorentzian curve, and fitting line at $V_{GS} = 40$ V. In this figure, the circular symbols, red-dashed line, and blue-dotted line indicate measured relative noise, fitted $1/f$ noise line, and Lorentzian curve, respectively. The black line is a fitting line which is the sum of $1/f$ and Lorentzian curves. The relative noise at $V_{GS} = 40$ V was well-fitted with the sum of $1/f$ line and Lorentzian curve with the estimated cut-off frequency f_0 of ~2900 Hz and the lifetime of the carriers τ_0 of ~340 μs. Figure 3(b) shows the relative noise and the $1/f$ fitting line at $V_{GS} = 60$ V. The red-dashed line is the $1/f$ fitting line with the slope of -1 and the statistical coefficient R^2 (>0.94), indicating that the data was well-fitted only with $1/f$ line (i.e., without Lorentzian curve). Here, as R^2 is close to 1, the data fits the equation. This implies that the contribution of the charge trapping and detrapping coming from the trap states is

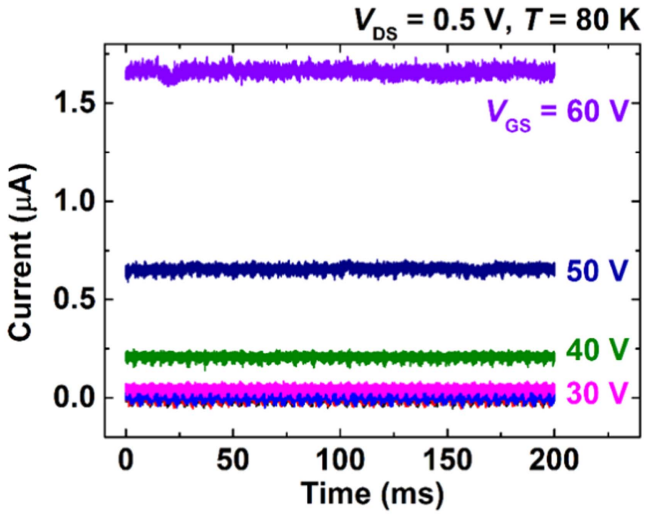

Figure 4. Time domain current fluctuations at low temperature (80 K) for various V_{GS} conditions at a fixed $V_{DS} = 0.5$ V.

relatively weak in the high V_{GS} region due to the fully induced channel. These results support the theory that a large number of traps exist in the CVD-grown monolayer MoS_2 and at the dielectric interface and these traps have a more significant influence at the low V_{GS} regime.

G–R noise can often be revealed in random telegraph noise (RTN) measurements when there is a dominating single two-level fluctuations [20]. So, we performed the time trace measurements for CVD-grown monolayer MoS_2 FETs at low temperature (80 K). Figure 4 shows the current fluctuations in time domain of a CVD-grown monolayer MoS_2 device at 80 K for V_{GS} ranging from 20 to 60 V at a fixed $V_{DS} = 0.5$ V. The current fluctuation increased as V_{GS} increased, however, the time domain current fluctuations did not show any noticeable signal of RTN [21].

Because of the large trap density, the CVD-grown monolayer MoS_2 can be regarded as a highly disordered system that has randomly distributed charge puddles when the carrier density is low. The behavior in a highly disordered system can be explained by a percolation theory. Since a disordered system can be considered as a random network of resistors, the fraction of conductive component p determines the conducting properties. Specifically, when p exceeds the percolation threshold p_c, current can flow through the conducting channel. The electrical noise originating from the constituent resistors can be expressed as [35, 36]

$$\frac{S_I}{I^2} = \frac{S_R}{R^2} = \tilde{s}(f)\frac{\sum_m i_m^4}{\left(\sum_m i_m^2\right)^2} \propto R^w \text{ at } p > p_c, \qquad (4)$$

where S_I, S_R i_m, $\tilde{s}(f)$, and R denote the power spectral density originating from the current fluctuation, the power spectral density originating from the resistance fluctuation, the current through a certain constituent resistor (m is the index of the mth resistor), a prefactor, and the resistance of the whole network system, respectively. The percolation behavior of the randomly distributed network should follow a power law with exponent w [15, 36, 37]. For a highly disordered system, due to a large number of trap states, the charges can hop through the accumulated charge regions (or charge puddles), acting as conducting paths (figure 5(a)) [38, 39]. From this point of view, an inverted-random void (IRV) model, which is a model used to explain dispersed conducting puddles in the insulating matrix, has been used to describe the percolation behavior of disordered systems [15, 37]. Based on the IRV model, the exponent w has been estimated as ~0.87 and ~2.4 for 2D and 3D disordered systems, respectively [40]. As depicted in figure 5(b), our CVD-grown monolayer MoS_2 showed the percolation behavior of a 2D system, with an exponent w of 0.65 and 0.95 at $V_{DS} = 0.5$ V and 2.5 V, respectively. As V_{DS} increased, the fraction of the conductive component p increased and the relative noise closely followed equation (4). Therefore, the CVD-grown monolayer MoS_2 can be considered as a highly disordered 2D system which follows the percolation model.

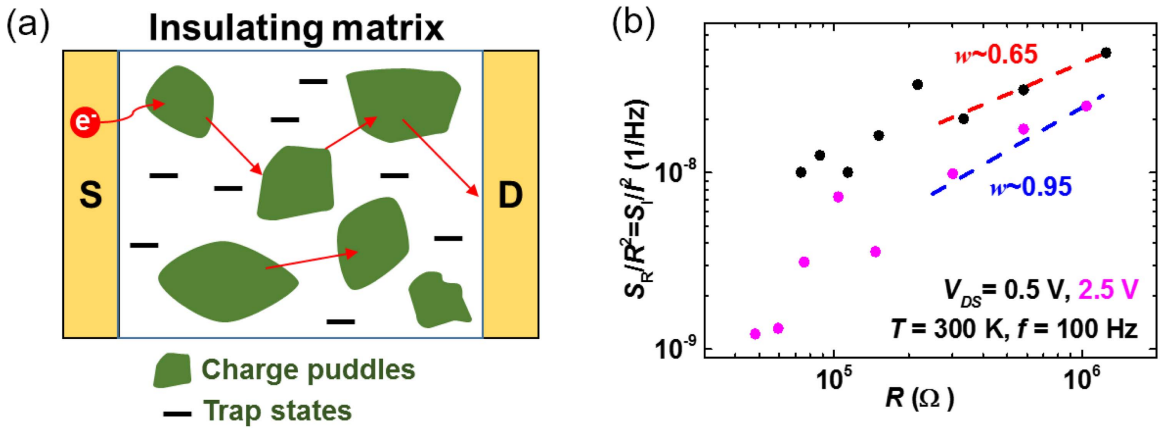

Figure 5. (a) Schematic illustration of carrier hopping through randomly distributed charge puddles (accumulated charges). The red circles, green pebble shapes, and yellow rectangles indicate the charge carriers (electrons), charge puddles, and source–drain electrodes, respectively. (b) The relation between the relative noise and the resistance for various V_{DS}. The red and blue dashed lines indicate the fitted line at $V_{DS} = 0.5$ V and 2.5 V, respectively.

4. Conclusions

In summary, the current–voltage and noise characteristics of CVD-grown monolayer MoS_2 were investigated in a temperature range from 80 to 300 K. The CVD-grown monolayer MoS_2 could be regarded as a disordered system due to the large number of trap states in MoS_2 created during the CVD synthesis. According to the McWhorter carrier number fluctuation model, a high trap density was extracted for the CVD-grown MoS_2. The relation between the relative noise and resistance following the power law of the 2D inverted-random void model also supported the disordered MoS_2 system. This study provides a better understanding of monolayer MoS_2 as a highly disordered system in terms of noise characteristics.

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References

[1] Jariwala D, Sangwan V K, Lauhon L J, Marks T J and Hersam M C 2014 *ACS Nano* **8** 1102
[2] Wang Q H, Kalantar-Zadeh K, Kis A, Coleman J N and Strano M S 2012 *Nat. Nanotechnol.* **7** 699
[3] Allain A, Kang J, Banerjee K and Kis A 2015 *Nat. Mater.* **14** 1195
[4] Chhowalla M, Shin H S, Eda G, Li L-J, Loh K P and Zhang H 2013 *Nat. Chem.* **5** 263
[5] Radisavljevic B, Radenovic A, Brivio J, Giacometti V and Kis A 2011 *Nat. Nanotechnol.* **6** 147
[6] Lopez-Sanchez O, Lembke D, Kayci M, Radenovic A and Kis A 2013 *Nat. Nanotechnol.* **8** 497
[7] Amani M *et al* 2015 *Science* **350** 1065
[8] Zhang W, Huang J K, Chen C H, Chang Y H, Cheng Y J and Li L-J 2013 *Adv. Mater.* **25** 3456
[9] Kim T-Y, Amani M, Ahn G H, Song Y, Javey A, Chung S and Lee T 2016 *ACS Nano* **10** 2819
[10] van der Zande A M *et al* 2013 *Nat. Mater.* **12** 554
[11] Zhu W, Low T, Lee Y H, Wang H, Farmer D B, Kong J, Xia F and Avouris P 2014 *Nat. Commun.* **5** 3087
[12] Kim I S *et al* 2014 *ACS Nano* **8** 10551
[13] Yu Z *et al* 2014 *Nat. Commun.* **5** 5290
[14] Rammal R, Tannous C, Breton P and Tremblay A-M S 1985 *Phys. Rev. Lett.* **54** 1718
[15] Planes J and Francois A 2004 *Phys. Rev.* B **70** 184203
[16] Conrad B R, Cullen W G, Yan W and Williams E D 2007 *Appl. Phys. Lett.* **91** 242110
[17] Song Y, Jeong H, Jang J, Kim T-Y, Yoo D, Kim Y, Jeong H and Lee T 2015 *ACS Nano* **9** 7697
[18] Ralls K S, SkocpolW J, Jackel L D, Howard R E, Fetter L A, Epworth R W and Tennent D M 1984 *Phys. Rev. Lett.* **52** 228
[19] Vandamme L K J and Hooge F N 2008 *IEEE Trans. Electron Devices* **55** 3070
[20] Balandin A A 2013 *Nat. Nanotechnol.* **8** 549
[21] Sangwan V K, Arnold H N, Jariwala D, Marks T J, Lauhon L J and Hersam M C 2013 *Nano Lett.* **13** 4351
[22] Renteria J, Samnakay R, Rumyantsev S L, Jiang C, Goli P, Shur M S and Balandin A A 2014 *Appl. Phys. Lett.* **104** 153104
[23] Sharma D *et al* 2014 *Nanotechnology* **25** 155702
[24] Na J *et al* 2014 *Nanoscale* **6** 433
[25] Najmaei S, Liu Z, Zhou W, Zou X, Shi G, Lei S, Yakobson B I, Idrobo J C, Ajayan P M and Lou J 2013 *Nat. Mater.* **12** 754
[26] Dumcenco D *et al* 2015 *ACS Nano* **9** 4611
[27] Lee C, Yan H, Brus L E, Heinz T F, Hone J and Ryu S 2010 *ACS Nano* **4** 2695
[28] Mak K F, Lee C, Hone J, Shan J and Heinz T J 2010 *Phys. Rev. Lett.* **105** 136805
[29] Splendiani A, Sun L, Zhang Y, Li T, Kim J, Chim C-Y, Galli G and Wang F 2010 *Nano Lett.* **10** 1271
[30] Late D J, Liu B, Matte H S S R, Dravid V P and Rao C N R 2012 *ACS Nano* **6** 5635
[31] Reggiani L, Kuhn T and Varani L 1992 *Appl. Phys.* A **54** 411
[32] Balandin A A 2002 *Noise and Fluctuation Control in Electronic Devices* (Los Angeles, CA: American Scientific)
[33] McWhorter A L 1955 1/f noise and related surface effects in germanium *PhD Thesis* Massachusetts Institute of Technology (https://dspace.mit.edu/handle/1721.1/4786)
[34] McWhorter A L 1957 *Semiconductor Surface Physics* (Philadelphia, PA: University of Pennsylvania Press)
[35] Kogan S 1996 *Electronic Noise and Fluctuations in Solids* (Cambridge: Cambridge University Press)
[36] Lee S B *et al* 2009 *Appl. Phys. Lett.* **95** 122112
[37] Balberg I, Wagner N, Hearn D W and Ventura J A 1988 *Phys. Rev. Lett.* **60** 1887
[38] Lo S T, Klochan O, Liu C H and Wang W H 2014 *Nanotechnology* **25** 375201
[39] Qiu H *et al* 2013 *Nat. Commun.* **4** 2642
[40] Tremblay A-M S, Feng S and Breton P 1986 *Phys. Rev.* B **33** 2077