Nanoscale

PAPER

View Article Online
View Journal | View Issue

Cite this: *Nanoscale*, 2016, **8**, 19876

Fully gravure printed complementary carbon nanotube TFTs for a clock signal generator using an epoxy-imine based cross-linker as an n-dopant and encapsulant†

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Received 3rd October 2016,
Accepted 11th November 2016

DOI: 10.1039/c6nr07762e

www.rsc.org/nanoscale

Printed p-type single walled carbon nanotube (SWCNT) based circuits exhibit high power dissipation owing to their thick printed dielectric layers (>2 μm) and long channels (>100 μm). In order to reduce the static power dissipation of printed SWCNT-base circuits while maintaining the same printing conditions and channel lengths, complementary metal–oxide-semiconductor (CMOS) based circuits are more ideal. These circuits, however, have not been successfully implemented in a scalable printing platform due to unstable threshold voltages of n-doped SWCNT based thin film transistors (TFTs). In this work, a thermally curable epoxy-imine-based n-doping ink is presented for achieving uniform doping and sealing of SWCNT layers by gravure printing. After printing the n-doping ink, the ink is cured to initiate a cross-linking reaction to seal the n-doped SWCNT-TFTs so that the threshold voltage of the n-doped SWCNT-TFTs is stabilized. Flexible CMOS ring oscillators using such n-doped SWCNT-TFTs combined with the intrinsically p-type SWCNT-TFTs can generate a 0.2 Hz clock signal with significantly lower power consumption compared to similarly printed p-type only TFT based ring oscillators. Moving forward, this CMOS flexible ring oscillator can be practically used to develop fully printed inexpensive wireless sensor tags.

Introduction

The popularity of printed electronics has drawn many efforts in developing printing systems where printers, materials and device designs are well matched to meet the demand for inexpensive, disposable, and flexible devices. Among these devices, the printed wireless cyclic voltammetry (CV) tag[1] has been considered as a prototype for realizing printed thin film transistor (TFT) integrated commercial products, integrating sensors, signage, amplifiers, logic circuits, and a power source all on one single relatively large area device at a low operating frequency. Furthermore, the required level of registration accuracy and pattern resolution to integrate TFTs in the wireless CV tag can be achievable on plastic or paper foils using gravure, flexographic, or offset printing.[2,3] In order to expedite the practical usage of such fully printed devices, a less-power-consuming printed ring oscillator for generating low frequency clock signals (<1 Hz) is necessary[4–6] and should be fully printed through a scalable printing system such as gravure on flexible foils.

Previously, p-type single-walled carbon nanotube (SWCNT) based TFTs (SWCNT-TFTs) have been utilized to develop a ring oscillator with operation frequencies ranging between 0.1 Hz to greater than 1 GHz in the wide range of operation power.[7–9] Such large differences in the operation frequency and voltage are dependent on the quality of the deposited SWCNT networks as well as the quality and dimensions of the deposited electrodes and dielectric layers for the construction of TFTs on rigid or flexible substrates.[10] For devices fabricated on smooth, rigid substrates such as Si/SiO_2, excellent percolating networks of SWCNTs can be obtained. In addition, a wide range of electrode and dielectric layer materials that can be deposited using vacuum processes allows for better ohmic contacts and high quality interfaces with the SWCNTs, enabling higher operation frequencies (>1 MHz). On the other hand, the rougher surfaces of printed substrates such as polyethylene terephthalate (PET) typically result in lower quality SWCNT networks. In particular, to enable direct gravure printing of SWCNTs, a polymer matrix is typically required to increase the

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†Electronic supplementary information (ESI) available: Experimental details, photos, SEM, and comparative tables. See DOI: 10.1039/c6nr07762e

viscosity of the inks for compatibility with gravure printing, which also leads to significantly lower device performances. In addition, a limited range of metal and dielectric inks makes it difficult to create ohmic contacts to SWCNTs. Unlike vacuum based processes such as atomic layer deposition (ALD), printed dielectric layers also cannot be easily controlled down to angstrom level roughnesses and generally contain mobile or fixed charges at the interfaces, leading to reduced performance.[11] All of these factors, in addition to larger source/drain to gate overlap capacitances due to alignment tolerances, lead to lower device performance and lower operating frequencies.

However, even with these limitations, printed SWCNT-TFTs have shown to be a promising candidate for large area electronics and disposable devices where performance requirements may not be as high as in traditional electronics systems. The high throughput of gravure printing allows for the mass production of electronics at a very low cost per area, making it an ideal platform for achieving these goals.

Currently, most of the printed SWCNT-TFT circuits have been based upon PMOS only architectures, which have much higher static power dissipation compared to CMOS. In order to reduce the power dissipation of printed SWCNT-based ring oscillators while maintaining the same printing system and device structure, CMOS SWCNT-based ring oscillators,[12,13] printed by a scalable printing method, are strongly demanded. However, fully printed CMOS circuits have not yet been demonstrated as most printing compatible n-type doping schemes such as poly(ethylene imine) (PEI),[14] poly(ethylene oxide),[15] or piperidine[16] typically exhibiting large threshold voltage variations.

Here, we demonstrate a thermally curable epoxy-imine-based ink for n-type doping of printed SWCNTs as well as encapsulating the SWCNT layers from the surroundings by one simple printing process. Fully gravure-printed CMOS ring oscillators printed utilizing this doping scheme can successfully generate a stable clock signal at an operating voltage of 5 V with lower power dissipation compared to PMOS only printed signal generators. Such fully printed CMOS ring oscillators can be used in developing CMOS printed digital circuits, particularly for constructing inexpensive and disposable wireless sensor tags[1,17,18] where less than 50 TFTs are integrated and the operation frequency is less than 1 Hz.[19,20]

Experimental section

Materials

A 100 μm thick poly(ethyleneterephtalate) (PET) film with 200 mm width was purchased from SKC, Korea and used without further surface treatment. Silver nanoparticle based ink (PG-007 BB) was obtained from Paru Co. Korea and formulated by adding dipropylene glycol methyl ether (Aldrich) to obtain the appropriate viscosity (500 cp) and surface tension (47 mN m^{-1}) for printing the gate and drain–source electrodes using roll-to-plate gravure. $BaTiO_3$ nanoparticle based ink (PD-100, Paru Co., Korea) was purchased from Paru Co. Korea and further formulated to obtain a viscosity of 73 cp and a surface tension of 32 mN m^{-1} using ethyl 2-cyanoacrylate (Aldrich) for printing the dielectric layers. For printing the channel, single walled carbon nanotube (SWCNT) based ink (PR-040, Paru Co., Korea) was obtained and diluted by using diethylene glycol monobutyl ether (Daejung Co., Korea). For n-doping and encapsulation, SU-8 (Microchem) was formulated using diethylene glycol (Aldrich).

Printing process

A roll-to plate (R2P) gravure printer (Fig. 1a) manufactured by i-PEN, Korea was used in the printing of the SWCNT-TFTs. For printing the gate electrodes, the roll pressure of the R2P gravure was maintained at 5 kgf cm^{-2} with a printing speed of 18 m min^{-1}. The printed gate electrode layer was annealed for 1 min at 150 °C and then, the dielectric layer was printed using a printing speed of 20 m min^{-1} and a roll pressure of 7.5 kgf cm^{-2}. The printed dielectric layer was also annealed for 1 min at 150 °C. SWCNT layers were printed with a printing speed of 30 m min^{-1} and a roll pressure of 4 kgf cm^{-2} and then annealed for 1 min at 150 °C. The drain–source electrodes were printed with a speed of 20 m min^{-1} and a roll pressure of 5 kgf cm^{-2} and then annealed for 1 min at 150 °C as well. Finally, n-doping was carried out using a blade coating method with the formulated SU-8 based ink, and the resulting n-doped ink was cross-linked by thermal treatment for 1 min at 150 °C. This heat treatment also encapsulates the n-doped channel to provide device stability by preventing exposure of the SWCNT layers to the surrounding environment.

Measurements

All inks were characterized using a DCAT21 (Dataphysics Co., Germany) and SV-10 Vibro viscometer for measuring the surface tension and viscosity of the inks, respectively. All measurements in this work were carried out under ambient conditions. The printed SWCNT-TFTs were characterized using a semiconductor parameter analyzer (4155C, Agilent, USA) and a digital phosphor oscilloscope (DPD 4054, Tektronix, USA) was used to characterize the fully printed inverters and ring oscillators.

Results and discussion

In this work, roll-to-plate (R2P) gravure (Fig. 1a) has been used to fully print the gate, dielectric, active, and drain–source layers to integrate ten SWCNT-TFTs into a five stage CMOS ring oscillator. A back-gated TFT device architecture with a channel length of 150 μm and a width of 4000 μm is explored so that the active SWCNT channel is accessible for doping.

For the printing of the TFTs, the gate electrodes are first printed onto PET foil using a silver nanoparticle based ink (PG-007, Paru, Korea). The electrodes were measured to have an average thickness of 700 ± 50 nm with a surface roughness of approximately 64 ± 10 nm (Fig. 1b) and a sheet resistance of 3 ± 0.1 mΩ sq^{-1} mil^{-1}. A $BaTiO_3$ nanoparticle based dielectric

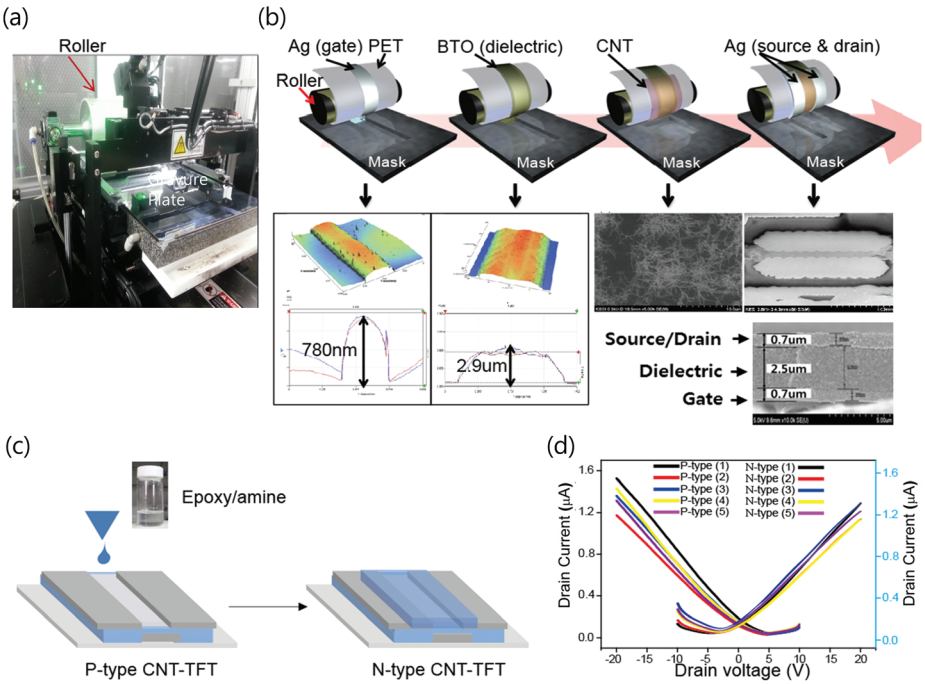

Fig. 1 Printing process of a printed CMOS circuit. (a) Image of the R2P gravure printer used in this work and (b) a schematic view of the R2P gravure printing process for printing the gate, dielectric, active and drain–source layers along with their respective 3D images, cross-sectional profiles, and SEM image. (c) Descriptive illustration of the n-doping process and (d) I_d–V_g characteristics before and after the n-type doping of the SWCNT-TFTs.

ink (PD-100, Paru, Korea) is then printed onto the gate electrodes with a resulting thickness of 2.7 ± 0.2 μm and a surface roughness of 94 ± 10 nm (Fig. 1b). From the capacitance–voltage (*C*–*V*) measurements on metal/insulator/metal test structures, the printed dielectric layers show a capacitance of 7 nF cm^{-2} (see Fig. S1a in the ESI†). A SWCNT-based ink (PR-040, Paru, Korea) is printed onto the dielectric layer as the active channel material. As the n-doping process slightly lowers the on-current of the TFTs, two different SWCNT loading concentrations are utilized to generate two different current levels (see Fig. S2 in the ESI†). For the NMOS portion of the ring oscillators, undiluted SWCNT ink is used to obtain the maximum on-current. For the PMOS portion, a diluted SWCNT ink is used to lower the on-current so as to match the n-doped NMOS TFTs. After printing on the SWCNT inks, the drain–source layers are printed using silver ink to complete the printing of the TFTs. *C*–*V* measurements of printed metal/insulator semiconducting (MIS) SWCNT test structures show the characteristic capacitance behaviour of MIS devices (20.5 nF cm^{-2} at −20 V, dropping down to 7.3 nF cm^{-2} at 20 V) with small hysteresis (see Fig. S1b in the ESI†). No short circuiting is observed for the 10 TFTs.

The conversion from p-type to n-type SWCNT-TFTs is carried out by simple blade coating of an epoxy-imine-based n-doping ink, formulated using a commercially available epoxy based photoresist (SU-8 from Microchem) as shown in Fig. 1c. The converting mechanism from p-type to n-type SWCNT-TFTs will be the same as the previously reported one[14,21] where SWCNT can be n-doped by replacing the absorbed oxygen with a nitrogen group of the polyethylene imine (PEI). We speculate that the nitrogen group in SU-8 will play the same role which can provide electrons from the unbound electron pairs of nitrogen.[14,21] The transfer characteristics of the ten p-type and n-type SWCNT-TFTs in a representative 5-stage ring oscillator are shown in Fig. 1d. The PMOS TFTs exhibit an average on-current of 1.36 ± 0.13 μA and an on/off ratio of 10^3 while the NMOS TFTs have an average on-current of 1.06 ± 0.13 μA with an on/off ratio of 10^2 (see Fig. S3 in the ESI†). The lower on/off ratios in the NMOS TFTs originate from the higher SWCNT loading, which leads to more percolation of metallic SWCNTs within the channel. The threshold voltages (V_{th}) for the PMOS and NMOS SWCNT-TFTs range from 0 to 4 V and 0 to −2 V, respectively (see Fig. S2 and S3 in the ESI†).

For almost all device applications using SWCNT-based circuits, air stability is crucial. Therefore, re-adsorption of oxygen or moisture which diffuses through the adsorbed PEI layers has been considered to be one major factor for the electrical variations and air stability in PEI doped n-type SWCNT-TFTs.[22] Due to the excellent passivation in our SU-8 based n-doping ink, our n-doped SWCNT-TFTs show high air stability for up to 3 months (Fig. 2a).

For proper operation of the ring oscillators, the variation in V_{th} and on-currents (see Fig. S4 in the ESI†) in the SWCNT-TFT is critical. In order to understand the amount of variation that can be tolerated for this system p-spice simulations were conducted using experimentally extracted parameters from the

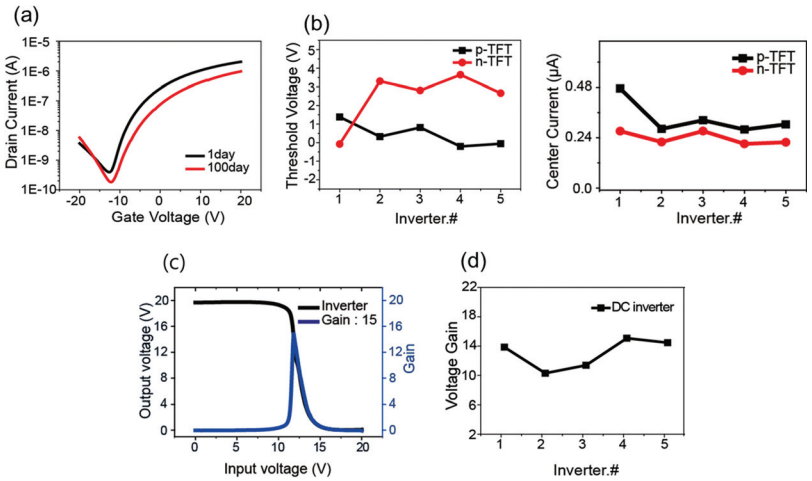

Fig. 2 Electronic performance of printed n-type and p-type SWCNT-TFTs (a) Stability of the printed n-type SWCNT-TFTs was proved by measuring the transfer characteristics of the converted n-type SWCNT-TFTs stored under an ambient atmosphere just after printing (black line) and after 100 days (red line). (b) Threshold voltage and on-currents of 5 n-type SWCNT-TFTs and 5 p-type SWCNT-TFTs within a 5-stage CMOS ring oscillator. (c) Voltage transfer curve of a CMOS inverter with high voltage gains at an input voltage of 20 V. (d) The voltage gains of 5 CMOS inverters within the ring oscillator.

printed n and p-type SWCNT-TFTs. From the simulations, a maximum of 30% variation in the on-currents can be tolerated before significant reductions in the clock speed occur (refer to the p-spice simulation results in Fig. S4 in the ESI†). These results show that the printed CMOS ring oscillators are more tolerant to on-current variations when compared with their PMOS only counterparts.

To reduce device-to-device variation, any parameter of the printing system that influences the parasitic capacitances in the SWCNT-TFTs has to be well controlled. For printed electronics, the inaccuracy of the drain–source electrode alignment with respect to the printed gate electrodes has been known as a major factor that must be better controlled.[2,3] In our system, an overlay printing registration accuracy of ±10 μm is achieved. In addition, by maintaining a constant rheology among the employed inks (silver ink, $BaTiO_3$ ink, SWCNT ink, and n-doping ink) and optimizing printing conditions (printing speed, impression roller pressure, and blade angle) the surface roughness of the printed dielectric layers, evenness of the printed SWCNT network density, thickness of the printed dielectric layers, and the edge roughness of the printed drain–source electrodes are all maintained to be stochastically constant with less than 10% variation across different

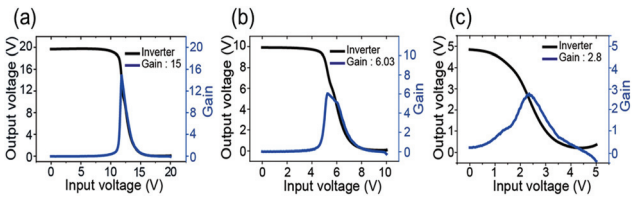

Fig. 4 Voltage transfer curves of a CMOS inverter at input voltages of (a) 20 V, (b) 10 V, and (c) 5 V.

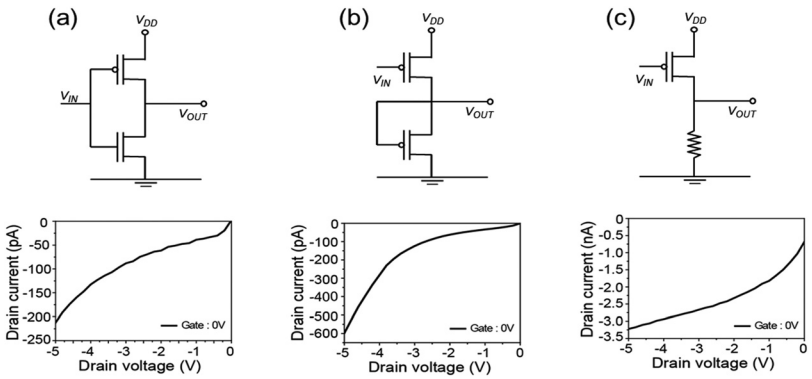

Fig. 3 Circuit schematics and ID–VD curves for the (a) CMOS, (b) PMOS-only, and (c) resistive load inverters to compare their respective static power consumptions.

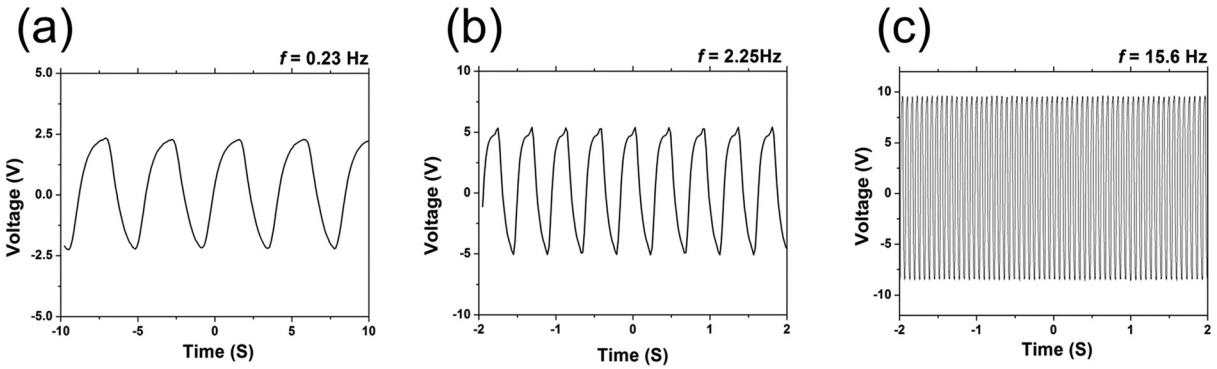

Fig. 5 Output characteristics of a five-stage CMOS ring oscillator (a) displaying output frequencies of 0.2 Hz at 5 V, (b) 2.3 Hz at 11 V, and (c) 15.6 Hz at 18 V.

devices.[24] The V_{th} and average on-currents of the gravure-printed n-type and p-type SWCNT-TFTs are listed in Fig. 2b. Although one out of the 10 SWCNT-TFTs do not fall within a 30% variation range, good switching behaviour and clock signal generation can still be obtained as shown later. Fig. 2c shows the voltage transfer curve of a representative CMOS inverter, with a gain of 15 V/V at an operating voltage of 20 V and Fig. 2d shows the gains of all 5 inverters within the 5-stage ring oscillator.

One important advantage of CMOS inverter designs is that there is lower static power dissipation. To prove this, we printed and measured 3-different types of SWCNT-TFT based inverters including CMOS, PMOS-only and PMOS with a resistive load to compare their relative static power consumptions (Fig. 3). The static power consumptions for each of the inverters at $V_{ds} = -5$ V were respectively estimated to be 1.06 nW, 2.99 nW and 16.1 nW for the CMOS, PMOS-only, and resistively loaded PMOS architectures. As such, the implementation of CMOS ring oscillators can potentially reduce the power consumption of printed SWCNT-TFT based electronic devices by 3 to 15 times over traditional PMOS only designs.

In addition to lower current draw, lower operating voltages are also important to achieve lower power consumption. The input voltage dependent voltage gains of the CMOS inverters ranging from 20 to 5 V are shown in Fig. 4. Based on the results of our previous fully printed RF 1-bit tone generating tags[25] and full adders,[26] a voltage gain of 3 is sufficient for operating simple TFT circuits (less than 50 TFTs) with a reasonable degree of functionality. Based on this requirement, the fully gravure-printed CMOS inverters demonstrated in this work can be operated at as low as 5 V. As shown in Fig. 5a, a 0.2 Hz clock signal can be successfully generated from our fully printed 5 stage CMOS ring oscillator with a 5 V input (Fig. 5a), while 2.3 Hz and 15.6 Hz clock signals can be generated with 10 V and 20 V inputs, respectively (Fig. 5b and c). Although the performance of our gravure-printed CMOS ring oscillators is lower than SWCNT-based CMOS ring oscillators fabricated using vacuum processes,[27,28] the attained clock signals at relatively low operating voltages is a good starting point for further development in the field of printed wireless CV tags.

Conclusions

In summary, for the first time, a CMOS ring oscillator has been realized with a fully printed, scalable gravure printing method using three different nanomaterial (silver nanoparticles, $BaTiO_3$ nanoparticles, and SWCNTs) based inks and a convenient n-doping ink through R2P gravure printing on PET foils. The n-doping ink based upon an epoxy-imine based resin has been specifically designed to convert p-type SWCNT-TFTs to n-type SWCNT-TFTs by simply printing onto a p-type SWCNT channel. The epoxy-imine-based n-doping ink has been designed to encapsulate the SWCNTs from being exposed to the surroundings after curing to provide air stability. Utilizing this doping scheme, SWCNT-TFT based CMOS flexible ring oscillators capable of generating a 0.2 Hz clock signal at DC 5 V can be realized. This operation voltage can be further decreased (~1.5 V) by employing the pure semiconducting SWCNTs[29] or monochiral SWCNTs.[30] Consequently, this R2P gravure system including the inks and circuit design to print a CMOS-type flexible ring oscillator can be practically used to develop a new field of fully printed wireless CV tags.

Acknowledgements

This research was supported by a grant (16163MFDS001) from the Ministry of Food and Drug Safety in 2016 and RIC at Sunchon National University. A. J. acknowledges support from the NSF NASCENT Center.

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