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Thermally Stable Ruthenium Contact for Robust *p*-Type Tellurium Transistors

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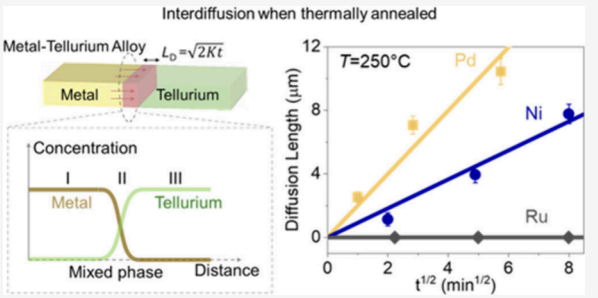
ABSTRACT: Tellurium (Te) is attractive for *p*-channel transistors due to its high hole mobility. Despite having a low thermal budget suitable for back-end-of-line (BEOL) monolithic integration, the practical realization of Te transistors is hindered by its thermal stability. In this work, we investigate thermal stability for Te thin films grown via scalable thermal evaporation. Our findings identify ruthenium as a more thermally stable contact for *p*-type Te transistors, capable of withstanding temperatures up to 250 °C. Ruthenium exhibits significantly lower diffusivity in Te compared to other contact metals commonly used such as nickel and palladium. Using the transfer-length method, we measured a contact resistance of 1.25 kΩ·μm at the ruthenium−tellurium interface. Additionally, the incorporation of high-κ ZrO_2 encapsulation not only suppresses the sublimation of the Te channel at elevated temperatures but also serves as the gate dielectric in top-gate devices operating at 1 V, achieving an on/off current ratio of 10^5.



KEYWORDS: *tellurium, interdiffusion, contact resistance, thermal stability, p-type FET, ALD encapsulation*

Elemental tellurium (Te) is attractive as a channel material for *p*-type thin film transistors due to its high hole mobility over 700 $cm^2V^{-1}s^{-1}$, surpassing other conventional 3D materials like silicon and germanium, van der Waals materials such as transition metal dichalcogenides and exhibiting comparable performance to black phosphorus.[1−5] Numerous studies have highlighted Te's potential for both electronic and optoelectronic applications.[6−14] Single crystalline Te can be obtained by solution processes,[2,7,15] physical vapor deposition[14,16,17] and liquid phase exfoliation,[10] though these methods lack scalability. In contrast, scalable techniques like molecular beam epitaxy[3,9,18] and thermal evaporation[1,8,19] often yield films with poor crystallinity. Among these, low temperature evaporated Te stands out as a particularly promising approach, offering scalability to full wafer uniformity while maintaining respectable switching characteristics.[1] The prospect of a high performance Te *p*-type field effect transistor (FET) opens up opportunities for implementing complementary architectures with the existing *n*-type counterparts like amorphous indium gallium zinc oxide (*a*-IGZO), indium oxide, cadmium sulfide and cadmium selenide.[4,20−23] Moreover, the low processing temperature of Te meets the stringent thermal requirement for back-end-of-line (BEOL) monolithic three-dimensional integration where the maximum process temperature must remain below 300 to 400 °C to protect the underlying silicon electronics. However, most metals investigated to date as an electrode for Te-based transistors, such as palladium, nickel and gold, have high diffusivity into the Te channel.[24,25] This prohibits the practical utility of Te in transistor applications partly due to interdiffusion at the metal-Te interface and thermal instability of the Te film.[25] Therefore, it is imperative to explore other metals as contact material to Te which are robust against thermal diffusion.

Te inherently exhibits *p*-type conduction, so the Fermi level resides close to the valence band edge, as supported by theoretical calculations.[26,27] The most commonly employed metal contacts for Te-based transistors are palladium (Pd) and nickel (Ni). Although the high work function of Pd or Ni promotes superior *p*-channel electrical transport, their stability becomes poor when subjected to temperatures above 200 °C.[25] Diffusion of Pd into the Te channel can take place during evaporation-induced heating.[17] Thermally stable metal contacts for scalable application of Te-FETs have not been achieved. This becomes a major drawback in BEOL integration, which includes certain annealing steps greater than 200 °C. The metal diffusion into the Te channel poses a

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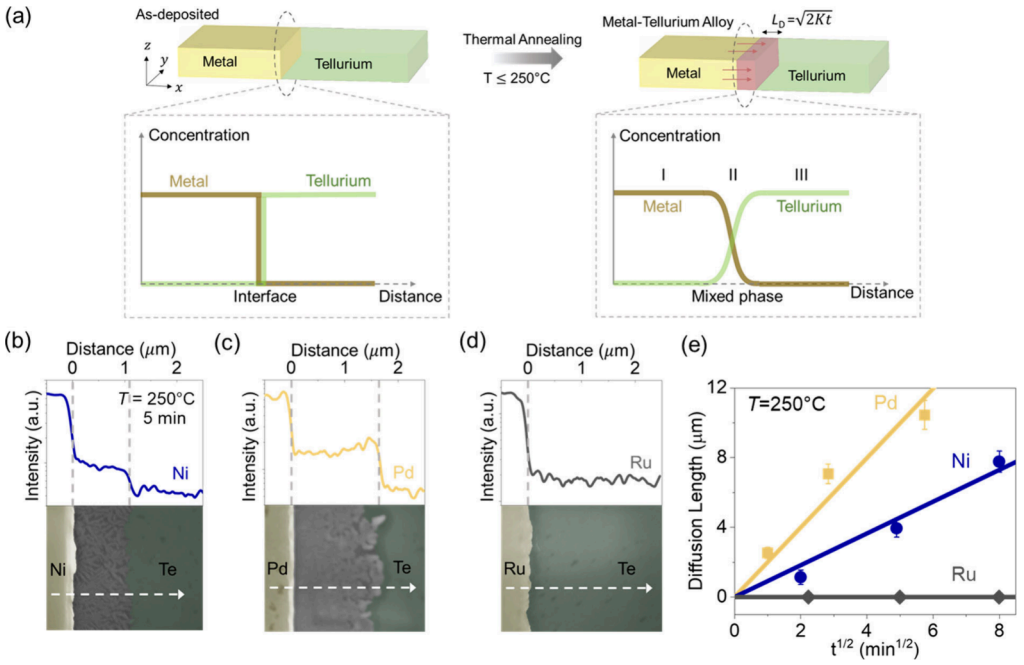

Figure 1. Diffusion of metal into Te. (a) Schematic diagram showing interdiffusion between metal-Te interface when thermally annealed at temperatures up to 250 °C. The interface transforms into a mixed phase containing concentrations of both metal and Te (Region II). The diffusion length is labeled as L_D. EDS line profile perpendicular to the metal-Te interface after annealing at 250 °C for 5 min and the corresponding false color top-down SEM image, showing metal diffusion into the Te film for (b) Ni, (c) Pd, and (d) Ru. White arrow represents the direction of the EDS scan. Two different steps can be seen in the intensity of Ni and Pd in the perpendicular direction, coming from the metal-alloy interface and the alloy-Te interface. Diffusion of Ru is not observed at this temperature. (e) Extracted diffusion length from optical images as a function of diffusion time ($t^{1/2}$) for Pd, Ni, and Ru.

severe limitation for ultrascaled transistors with short channel lengths.

Here, we propose ruthenium (Ru) as a thermally stable electrode for the Te channel. Ru is shown to have very low diffusivity into Te at elevated temperatures after annealing at 250 °C for 2 h. This allows headroom for functional Te-FETs that can withstand temperatures up to 250 °C without degradation in contact resistance and on−off current ratio. A low contact resistance of 1.25 kΩ•μm is extracted using the transfer-length method (TLM). A top-gated Te transistor is demonstrated using a high-κ ZrO_2 dielectric operating under low gate bias of 1 V, where the gate dielectric also serves as an encapsulant to prevent sublimation of Te at high process temperatures. This work highlights the feasibility of tellurium for BEOL integration in emerging technologies for high-performance scaled transistors.

Solid-state diffusion between two materials in contact can occur spontaneously, as dictated by the laws of thermodynamics, due to the negative free energy of mixing (ΔG_{mix}). This process promotes a phase transition into a more stable mixed phase that incorporates both materials (Figure 1(a)).[28,29] For the metal-Te interface, the diffusion of metal and Te atoms at the interface becomes significant at temperatures up to 250 °C, leading to growth of the stable mixed phase, herein referred to as an alloy. To investigate this phenomenon, we first patterned the Te film and then deposited the metal contact using standard photolithography and evaporation to achieve a thin film of known thickness (see Methods). The crystallinity of the Te film was characterized using Raman spectroscopy (Figure S1). The polycrystalline Te film exhibits three vibrational modes at 105 cm^{-1} (E_1), 131 cm^{-1} (A_1) and 147 cm^{-1} (E_2) respectively, consistent with previous reports.[2] Given Te's high vapor pressure at temperatures above 200 °C, sublimation poses a challenge during thermal processes.[25] To mitigate this, the metal-Te stack was encapsulated with 5 nm of zirconium dioxide (ZrO_2) deposited by atomic layer deposition (ALD). The metal-Te stack was then subjected to rapid thermal annealing (RTA) in a nitrogen ambient.

The diffusion kinetics of metal atoms into the channel material in FETs have been previously studied in the literature.[30,31] We adopted a similar approach to quantify the diffusion of Ni, Pd, Au, Pt and Ru into Te using optical dark-field microscopy. Figure S2 shows the bright-field and the corresponding dark-field optical images of Ni−Te interface after different annealing times at 250 °C. The growth of the Ni−Te, Pd−Te and Au−Te mixed phases involves an alloying reaction and exhibits visual changes in both bright-field and dark-field optical images. The progression of the alloy-Te interface with annealing time is used to extract the diffusion length (L_D) of the metal into Te, which corresponds to the length of the mixed phase. The diffusion length of the Au−Te interface cannot be measured due to high solubility of Te into Au (Figure S3). To further clarify the presence of metal atoms in the alloy near the interface, energy-dispersive spectroscopy (EDS) is used after the annealing treatment. As shown in Figure 1(b, c), an EDS line scan perpendicular to the interface reveals the presence of Ni or Pd after annealing for 5 min. Two different steps can be seen in the line scan for the metal intensity, originating from the metal-alloy interface and the alloy-Te interface. The diffusion of metal is observed to be nonisotropic due to the polycrystalline nature of the Te film. To determine the diffusion length from optical images, we measured across 20 interfaces to calculate the average length

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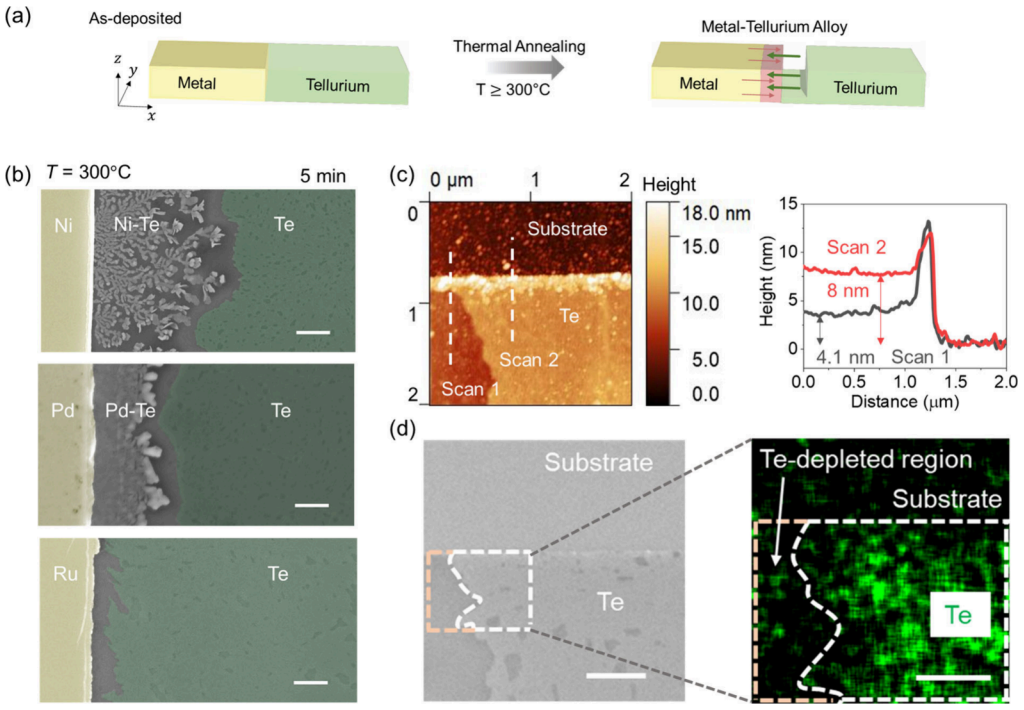

Figure 2. Metal-Te interfaces at higher temperatures. (a) Schematic diagram illustrating interdiffusion at the metal-Te interface during thermal annealing at temperatures of 300 °C and above. At these temperatures, significant diffusion of Te into the metal occurs, resulting in a Te-depleted region near the interface. (b) False color top-down SEM image of metal-Te interface after annealing at 300 °C for 5 min. Dendritic growth of Ni−Te and Pd−Te alloy can be seen at these temperatures. Diffusion of Ru into Te is not observed at 300 °C. However, the Te-depleted region can be seen for all cases. Scale bar: 1 μm. (c) AFM image and the height profile of 8 nm Te film near the Ni−Te alloy region after annealing at 300 °C for 5 min. Scan 1 reveals the height of the Te-depleted region is reduced by half. (d) Top-down SEM image and EDS mapping of Te near the Ni−Te alloy interface. Scale bar: 500 nm (left), 250 nm (right).

for each annealing time. Assuming the alloying reaction of the metal-Te interface is diffusion limited, the diffusion length is proportional to the square root of time according to the parabolic growth relation shown in eq 1,[28]

$$L_D = \sqrt{2Kt} \tag{1}$$

where K is the temperature-dependent parabolic growth constant that is proportional to the interdiffusion coefficient for the mixed phase, and t is the diffusion time. The observed linear trend in Figure 1(e) confirms that the alloying reaction is instantaneous and governed by the rate at which the atoms are transported to the interface. The parabolic growth constants of Pd and Ni at different temperatures are shown in Table S1. Pt shows very little diffusion while Ru shows no measurable interdiffusion when thermally annealed at 250 °C for 2 h. This is expected, as Ru has demonstrated resistance to diffusion in both dielectrics and conventional semiconductors like silicon, even at relatively high temperatures.[32−34]

At elevated temperatures ($T \geq 300$ °C), Te atoms gain sufficient energy to migrate within the film. Alongside the diffusion of metal atoms into Te, the diffusion of Te into the metal becomes pronounced, leading to Te-depletion near the alloy interface as depicted in Figure 2(a). To gain insight into the interdiffusion phenomenon, we analyzed the binary phase diagram for Te with various metals.[35−39] Of the five binaries, only Pd and Au show a finite solubility of Te at low temperatures. All five metals, however, form intermetallic compounds. In the case of Pd, Ni and Pt, there are multiple intermetallic phases accessible to the alloy system. For Ru−Te there is a single stable intermetallic compound with approximately 65 atomic percent of Te. These observations suggest that all five alloys will form intermetallic precipitates or films at the interface. Notably, Ni−Te and Pd−Te systems develop a dendritic alloy microstructure near the interface at higher temperatures. Ru atoms, however, do not diffuse into the Te film, rather Te diffuses into Ru as shown in Figure 2(b). Scanning electron microscopy (SEM) images of the metal-Te interface at this temperature clearly show the Te-depleted regions at the edge of the interdiffusion alloy. To confirm Te-depletion, we examined the surface morphology of the affected interface using atomic force microscopy (AFM). Line scans across the Te film, as shown in Figure 2(c), reveal a significant reduction in Te film thickness near the interface. Additionally, EDS mapping of Te for a representative Ni−Te alloy interface annealed at 300 °C (Figure 2(d)) further confirms the deficiency of Te near the interface.

Ru has a work function of 4.78 eV, which is lower than that of Ni or Pd.[15,40] From the energy band alignment of Te with various metals, Ru should theoretically form an Ohmic contact with Te, given that the work function of Ru is greater than the valence band maximum of Te.[26] However, Fermi level pinning at the metal−semiconductor junction can induce a Schottky barrier height, resulting in increased contact resistance.[41] To evaluate Ru as a contact electrode, we fabricated back-gated FET using 50 nm SiO_2 as the gate dielectric and p^+ Si as the gate electrode (Figure 3(a)). The I_d-V_d plot in Figure 3(b) shows a linear increase in drain current at low drain bias, providing preliminary evidence of Ohmic contact from Ru. The transfer curve in Figure 3(c) highlights the ability of the Ru-contact to deliver a higher on-current while maintaining the on−off current ratio at a drain bias of −1 V.

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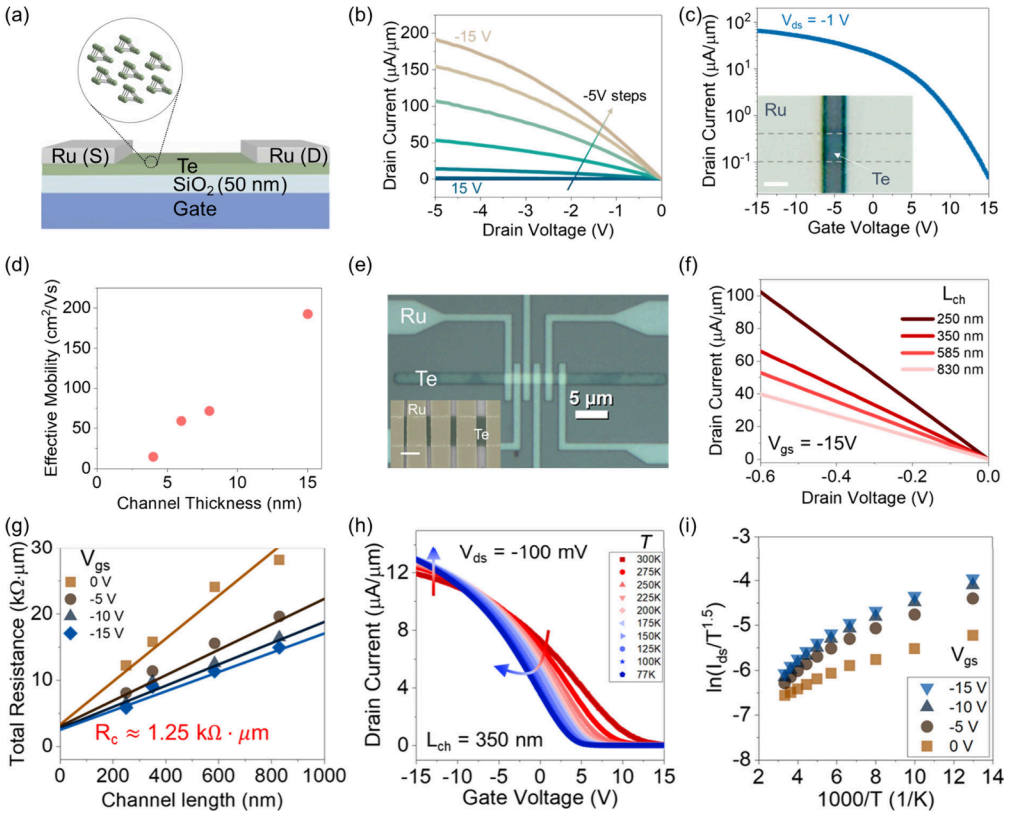

Figure 3. Te transistor with Ru contacts. (a) Schematic diagram showing a back-gated transistor fabricated from an evaporated Te film. Magnified region shows a schematic of the crystal structure of Te. (b) I_d-V_d plot of back-gated Te (8 nm) transistor with Ru contacts. Channel length and width are both 1.5 μm. (c) I_d-V_g plot of the same device at a drain bias of −1 V. Inset figure illustrates the optical image of a Te-FET with Ru contacts, fabricated using photolithography. Inset scale bar: 1.5 μm. (d) Effective mobility of the Ru-contact Te-FET for the different channel thicknesses studied in this work. (e) Optical image of the TLM structure with 8 nm thick Te for extraction of contact resistance. Inset figure shows false color top-down SEM image of the electrodes in the TLM device. Inset scale bar: 1 μm. (f) Drain current of short channel Te transistors in the on-state. (g) Total resistance−channel length plot showing an extracted R_c of 1.25 kΩ·μm. (h) I_d-V_g of a short channel Te transistor at different temperatures. (i) Arrhenius plot of Ru-contact Te-FET at different gate biases.

Thin film materials formed by physical vapor deposition typically exhibit an amorphous structure when deposited on unheated substrate, necessitating high-temperature postdeposition annealing to induce crystallization. Interestingly, Te undergoes an amorphous-to-crystalline phase transition near ambient temperature.[19] By carefully controlling the crystallization temperature, it is possible to suppress nucleation site formation, thereby leading to larger grain size (>6 μm^2) with high hole mobility. Here, we utilized this lower crystallization temperature to take advantage of the high effective mobility. The effective mobility (μ_{eff}) is evaluated from the transfer characteristics using the relation,

$$\mu_{eff} = \frac{dI_{ds}}{dV_{ds}} \frac{L}{WC_{ox}(V_{gs} - V_t)} \quad (2)$$

where L and W are the Te channel length and width, respectively, C_{ox} is the gate capacitance and V_t is the threshold voltage extrapolated from the linear portion of the I_d-V_g. The mobility enhancement is exhibited across a range of Te thicknesses (Figure 3(d) and Figure S6), similar to that previously observed for Te-FETs made with high work function metals such as Ni. This highlights the utility of Ru as a contact material for high-performance p-type thin film transistors.

We further explored the Ru−Te interface by extracting the contact resistance using the transfer-length method. The optical image and false-color SEM image of the short channel Te-FET with Ru contact are shown in Figure 3(e). The on-current increases as the channel length is scaled down (Figure 3(f)). The drain current shows a linear dependence with the applied drain bias for all channel lengths in the on-state at V_{gs} = −15 V (Figure S7). In a three-terminal FET, the total resistance (in units of kΩ·μm) comprises the contact resistance (R_c) from the source and drain ends and the channel resistance (R_{ch}) of the Te thin film, which is expressed as,

$$R_{total} = 2R_c + R_{ch} = 2R_c + R_{sh}L_{ch} \quad (3)$$

where R_{sh} is the sheet resistance of Te, independent of the channel dimensions and L_{ch} is the channel length of the transistor. As the channel length approaches zero, the entire resistance is comprised of just the contact resistance of the source and drain. The total resistance as a function of channel length is plotted in Figure 3(g) for various gate biases. A contact resistance of 1.25 kΩ·μm is calculated from the extrapolated curves, the accuracy of which can be verified from the convergence at the y-intercept. To corroborate our previous observation of Schottky-barrier-free transport at the source-drain interface, temperature-dependent transfer curves are shown in Figure 3(h). Mobility enhancement is evident from the evolution of the I_d-V_g curve as temperature decreases, which arises from suppressed phonon scattering. There is an associated shift in the threshold voltage in the negative

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direction, which has been previously observed for single crystalline Te nanoflakes.[7] The Arrhenius plot ($\ln(I_{ds}/T^{3/2})$ versus $1000/T$) in Figure 3(i) shows a positive slope, saturating at lower temperatures. Based on the thermionic emission model for two-dimensional Schottky FETs, a positive slope in the Arrhenius plot indicates mobility enhancement in the low-temperature regime while the saturation trend implies zero barrier at the contact.[42] This provides additional evidence of Ohmic contact at the Ru−Te interface.

To explore the thermal stability of the contact metal for Te-FETs, we used the same back-gated transistor having a channel width/length ratio of W/L = 1.5/1.5 μm followed by an additional encapsulation of 5 nm ALD ZrO_2. The ALD encapsulation has a negligible effect on the mobility of the Te-FET as shown in Figure S8. The transistors were annealed using RTA for 15 s at each temperature step and measured immediately afterward. The contact resistance was extracted from the transfer curves using the Y-function approach (see Supporting Information).[43,44] The on−off current ratio was obtained from the same transfer curve at V_{gs}=∓15 V. As shown in Figure 4(a), Ni and Ru-contacted Te-FETs initially have

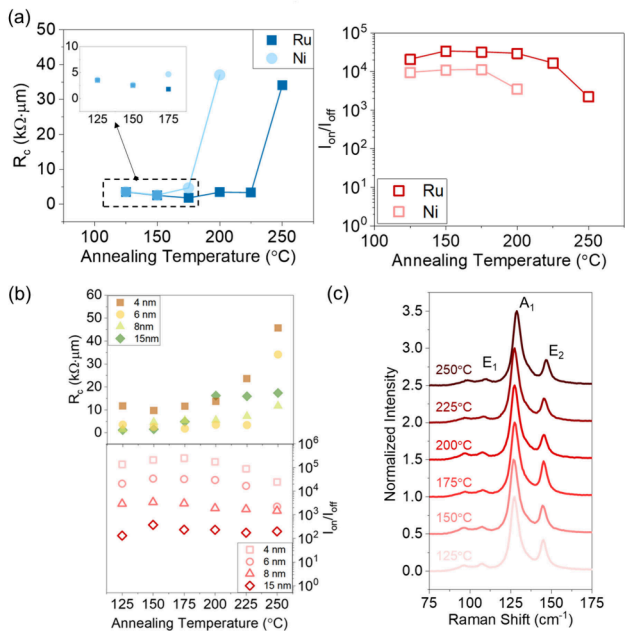

Figure 4. Thermal stability of Ni- and Ru-contacted Te transistors. (a) Contact resistance and on−off current ratio for Ni- and Ru-contacted Te-FET as a function of annealing temperature. The Te channel thickness is 6 nm. Inset shows a magnified scale of R_c in the 125−175 °C temperature range; axes have the same units as the main figure. (b) Evolution of contact resistance and on−off current ratio degradation with annealing temperature for Ru-contact Te transistor with various channel thicknesses. (c) Raman spectra of the Te thin film (6 nm) after different annealing temperatures, showing the Te channel is not degraded for the range of temperatures studied.

comparable contact resistance, matching the R_c extracted using the TLM method. The Ni-contacted devices are stable up to 175 °C, after which both R_c and the on−off current ratio degrades. Beyond 200 °C, the Ni−Te alloying progresses across the entire channel length, leading to transistor shorting (Figure S9). In contrast, Ru shows no diffusion into the Te channel below 250 °C, maintaining low contact resistance throughout the annealing steps without forming any alloy. At higher annealing temperatures, the Te film becomes unstable, resulting in the formation of Te-depleted regions near the contact edge, as previously discussed. For high-diffusivity metals such as Pd or Ni, the initial degradation is accommodated by the alloying reaction, followed by wicking of Te atoms into the adjacent metal near the alloy interface (Figure 2(b)).

The stability of Ru-contacts was investigated across a range of Te thicknesses and prolonged annealing times (Figure 4(b) and Figure S11). The thinner Te channel (4 nm) shows a higher contact resistance than thicker channels due to the larger optical bandgap arising from quantum confinement effects.[1] This suggests the introduction of an energy barrier at the contact for very thin Te films. The larger bandgap suppresses off-state current from thermal generation, as exhibited by the better on−off current ratio for a channel thickness of 4 nm. There is no significant improvement in contact resistance for channels ranging from 6 to 15 nm in thickness. For thicker channels, the on−off current ratio is reduced due to the difficulty in fully depleting the Te channel of charge carriers. Te transistors operate in accumulation mode, meaning the transistor turns off when the channel is depleted of charge carriers. As channel thickness increases, gate control over the electrostatic charges weakens. This trend has been previously observed in both Te-based and transition metal dichalcogenide-based transistors.[45,46] For the range of annealing temperatures studied, Ru contacts are shown to be resistant to degradation from metal diffusion across various thicknesses. Figure 4(c) shows the Te channel sustains no damage from annealing, as revealed by the Raman signal intensity of the annealed Te film.

Te stands out as a promising candidate for switching applications, which require low off-state current to minimize static power dissipation. Apart from thermally stable metal contacts, encapsulation of the Te channel is vital for operation at elevated temperatures. We demonstrated that the same capping layer can be used as a top-gate dielectric (Figure 5(a)). A double-gate architecture offers greater control over the channel current. Here, we used ZrO_2 as the top-gate dielectric in addition to SiO_2 as the back-gate oxide. Figure 5(b) portrays the transfer characteristics of a dual-gate Te-FET with different back-gate biases. Since the top-gate electric field is screened over the source-drain contact, using the top-gate in conjunction with the global back-gate enables higher on-current by modulating the Te channel underneath the metal contacts. This highlights the potential of Te thin-film transistors for use in a multilayer stacked configuration for improved channel electrostatics. As can be seen in Figure 5(c, d), the top-gate Te-FETs demonstrate low contact resistance for an annealing temperature of up to 275 °C with a trade-off in on−off current ratio.

In summary, this study examined the thermal stability of Te-FETs with various metal contacts. We found the device degradation at lower temperatures (<250 °C) is primarily limited by metal diffusion from the contacts, while the solubility of Te into the contact metal is the limiting factor at higher temperatures (>300 °C). Our investigation identified Ru as a promising alternative contact material for more stable Te-FETs, providing low contact resistance and compatibility with wafer-scale processing of evaporated Te. This work underscores the importance of stable electrode contacts for high-performance Te transistors and charts a path toward the

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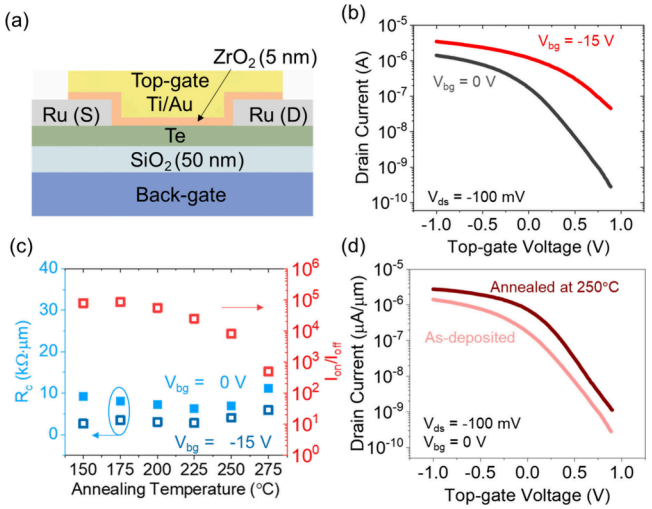

Figure 5. Top-gate operation of thin-film Te transistor. (a) Schematic diagram of a top-gate Te transistor using the ZrO_2 layer as the gate dielectric. The thickness of Te and ZrO_2 are both 5 nm. (b) Drain current as a function of top-gate voltage for different back-gate biases. (c) Thermal stability of the top-gate Te transistor. Contact resistance is extracted for different back-gate biases. (d) Drain current as a function of top-gate voltage for as-deposited Te-FET and after 250 °C annealing for 15 s.

feasible integration of durable *p*-channel transistors BEOL with silicon electronics.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.4c06553.

Methods for thermal evaporation of Te thin film, device fabrication and measurement, Raman characterization, optical bright-field and dark-field images of annealed interfaces, degradation of Au−Te and Pt−Te interface, statistical distribution of extracted diffusion length, transfer curves for different channel thickness and length, effect of ALD encapsulation, contact resistance degradation with thermal annealing, hysteresis of top-gate and back-gate transistors, data for parabolic growth constant, R_c extraction using Y-function, diffusion length extraction (PDF)

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Author Contributions

I.K.M.R.R., N.H., T.K., and A.J. conceived the idea for the project and designed the experiments. I.K.M.R.R., I.K., S.W., S.W., and H.M.K. fabricated the devices. I.K.M.R.R. performed the electrical measurements. I.K.M.R.R, T.K., S.W., and V.A. imaged the samples. I.K.M.R.R., N.H., T.K., J.B., J.W.A., D.C.C. and A.J. analyzed the data. I.K.M.R.R., T.K., and A.J. wrote the manuscript. All authors discussed the results and commented on the manuscript.

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Notes

The authors declare no competing financial interest.

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