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# Low Contact Resistance $WSe_2$ *p*-Type Transistors with Highly Stable, CMOS-Compatible Dopants

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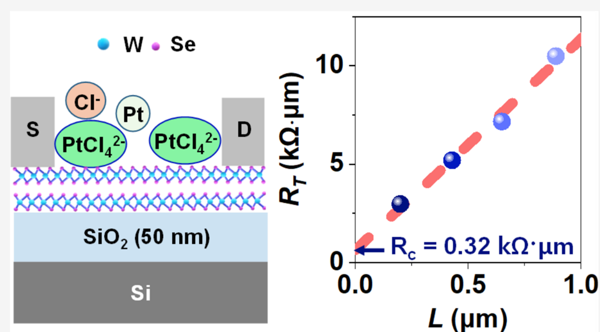
**ABSTRACT:** High contact resistance has been a bottleneck in developing high-performance transition-metal dichalcogenide (TMD) based *p*-type transistors. We report degenerately doped few-layer $WSe_2$ transistors with contact resistance as low as 0.23 ± 0.07 kΩ·*μ*m per contact by using platinum(IV) chloride ($PtCl_4$) as the *p*-type dopant, which is composed of ions compatible with the complementary metal-oxide-semiconductor (CMOS) fabrication process. Top-gated devices with a gate length of 200 nm showed good switching behaviors, implying that the dopant diffusion into the gate stack is not significant. The devices showed nearly identical performance after being kept in air for 86 days without any encapsulation while retaining the degenerately doped states at 78 K with pressure lower than $10^{-5}$ Torr, highlighting the stability of the dopants. The presented method sets forth the availability of highly stable methods for pattern doping the transistors with a thinned Schottky barrier width for low contact resistance devices.




**KEYWORDS:** *tungsten diselenide, charge transfer doping, FETs, two-dimensional material, high stability*

Transition-metal dichalcogenides (TMDs) are highly promising semiconducting materials for the next-generation field-effect transistors (FETs) as their nature of being two-dimensional enables the development of transistors with the ultimate thickness limit at the atomic scale.[1,2] Hence, utilizing TMDs as the channel material of the complementary FETs[3] (CFETs) will result in the most aggressive vertical dimensional scaling of future FETs. While the CFETs require both the *p*-type FETs (*p*-FETs) and their *n*-type counterparts, the *p*-FETs are more challenging due to the unfavorable band alignments between most metals used as contacts and the TMD material. Still, out of these materials, $WSe_2$ shows the highest potential for developing *p*-FETs since its valence band alignment with high work function metals is superior[4] to most other TMDs, which can lead to higher hole injection efficiency between the contacts and the channel. As such, there have been reports of $WSe_2$ *p*-FETs with high hole mobility above 100 $cm^2$/V·s, subthreshold swing near 60 mV/dec, and $10^8$ on−off current ratio.[5−8]

Still, one of the major issues with the TMD-based FETs is the high contact resistance due to the large Schottky barrier (SB) height between the metal contacts and the semiconductor channel.[9] With the SB height being fixed by the material properties, it is essential to achieve SB width thinning by degenerately doping the regions either beneath or contiguous to the metal contacts to minimize the contact resistance. Different methods to degenerately dope the TMDs have been studied in the field such as substitutional doping[10−14] and charge transfer doping.[15−19] Substitutional doping for this case is not feasible, as it can only be done during the material growth stage. On the other hand, many charge transfer methods utilize dopants that are either incompatible with the complementary metal-oxide-semiconductor (CMOS) processes or show highly diffusive behavior such that they require extremely fine-sized patterns for them to selectively dope the regions near the contacts. Although other notable reports of low resistance *p*-type FETs were made while only using CMOS-compatible methods and processes,[20−22] we still need different methods that can lower the contact resistance of the device down to a few hundred Ω·*μ*m.

Here, we present a charge-transfer-based *p*-type doping method using platinum(IV) chloride ($PtCl_4$), which is composed of ions compatible with the CMOS fabrication process. The dopants are observed to be highly stable in air while showing low diffusion between the prepatterned gate stacks of the few-layered $WSe_2$ FETs. We report the contact resistance of a bilayer $WSe_2$ device with $R_c$ = 0.23 ± 0.07

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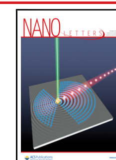

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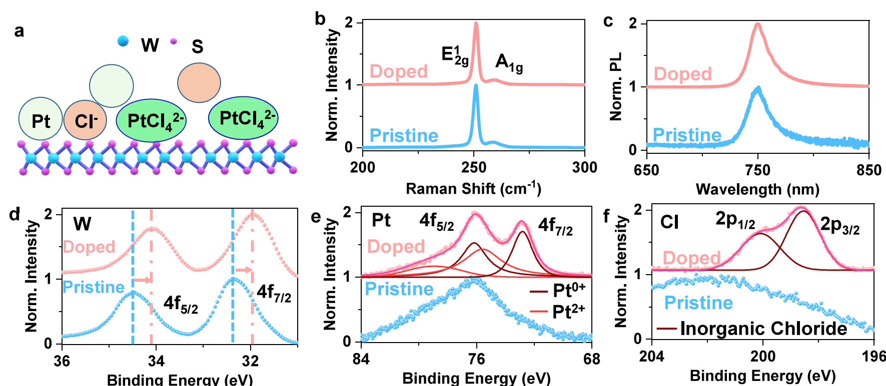


**Figure 1.** Doping characterization of the $WSe_2$–$PtCl_4$ system. (a) Schematic of the dopant molecules on a layer of $WSe_2$. (b) The Raman shift of an exfoliated bilayer $WSe_2$ flake before and after doping shows no peak shift. (c) The normalized photoluminescence spectra of a monolayer $WSe_2$ flake showing a 0.4 nm change in peak position upon doping the exfoliated flake. XPS surface analysis of $WSe_2$ before and after $PtCl_4$ doping with binding energy peaks of (d) W $4f_{7/2}$ and $4f_{5/2}$, (e) Pt $4f_{7/2}$ and $4f_{5/2}$, and (f) Cl $2p_{3/2}$ and $2p_{1/2}$.

kΩ·μm using the Y-function method (YFM)[23] and 0.32 ± 0.24 kΩ·μm measured with the transfer length method (TLM)[24] with a doping concentration as high as up to approximately $1 \times 10^{13}$ $cm^{-2}$. For a demonstration of a functioning top-gated device with underlapping regions, a long-channel device with a thicker flake was fabricated with on-currents of over 10 μA/μm. Furthermore, top-gated devices of bilayer $WSe_2$ with a gate length of only 200 nm using a $ZrO_2$ gate dielectric still showed good switching behavior with a subthreshold swing of 155 mV/dec and an on–off ratio greater than $10^7$. This implies that the dopant diffused laterally less than 100 nm from each side of the source and the drain of the FET and that the doping technique can be applied to selectively dope small-sized patterns made by conventional lithography methods to fabricate *p*-type devices with high performance. This scheme is highly desirable for underlapped top-gate devices since the regions adjacent to the source and the drain can only be influenced by fringing electric fields from the top gate. Overlapped top-gate devices are unemployed for high-performing devices, since they create a highly unfavorable parasitic coupling capacitance between the contacts and the top gate.

Figure 1a depicts a schematic of the charge transfer dopants that remain on top of a $WSe_2$ flake upon doping by treating the flake with a solution of $PtCl_4$ dissolved in hydrochloric acid (HCl). Figure S1 depicts a schematic energy band diagram of the bilayer $WSe_2$ along with the largest reduction potential ($E_0$) of the electron withdrawal process of the dopant,[25] $Pt^{2+} + 2e^- \rightarrow Pt^{0+}$, in reference to the vacuum energy level ($E_{vac}$). The valence band maximum[26] ($E_v$) of the bilayer $WSe_2$ is positioned above $E_0$, showing that the dopants can oxidize $WSe_2$ and hence increase its hole concentration. The Raman spectrum of a bilayer flake in Figure 1b shows no shift in the peak position before and after doping, which implies that the crystal structure of $WSe_2$ remains relatively intact without change. To further corroborate this, we performed photoluminescence measurement on a monolayer flake of $WSe_2$ where the normalized spectrum in Figure 1c shows a change of less than 0.4 nm in the peak wavelength, again confirming that the crystallinity of the flakes remains unaffected after doping. Although we cannot exclude the possibility of a thin layer of platinum forming over the surface of $WSe_2$, the formation of a conductive layer on the $WSe_2$ surface should alter the PL spectra due to different light–matter interaction conditions.[27] Thus, our negligible spectral shift in PL shows that the formation of an ultrathin metal layer on the surface of $WSe_2$ is unlikely. The topographic information is presented in Figure S2, where the atomic force microscopy images are presented before and after the doping of a $WSe_2$ flake. The surface roughness ($R_q$) of the flake increases only slightly from 0.58 nm to 0.60 nm before and after doping, indicating only a small formation of platinum is necessary to dope the flake.

We confirmed through X-ray photoelectron spectroscopy (XPS) that $PtCl_4$ exposure to $WSe_2$ can lower its Fermi level and hence facilitate *p*-type doping. Figure 1d shows the W 4f peaks of the XPS data, where the doped $WSe_2$ sample displays a 0.40 eV decrease in the binding energies of the peak positions. Specifically, W $4f_{5/2}$ shifts from 34.50 to 34.10 eV, and W $4f_{7/2}$ shifts from 32.35 to 31.95 eV upon doping. Downshift of a similar size in the binding energies of the peak positions is also visible in the Se 3d peaks in Figure S3 again, confirming *p*-type doping. The XPS peaks of Pt and Cl in Figure 1e and f also become visible upon doping, indicating that they were introduced after doping. The peaks of Pt suggest that they exist as $Pt^{0+}$ or $Pt^{2+}$, with most of the Pt in the form of $Pt^{0+}$, while the peaks of chlorine display that the chlorines exist without carbon bonds as in inorganic compounds. This implies that the dopant, which initially exists as $PtCl_4^{2-}$ ions in the solution, mainly appears as $Cl^-$ and $Pt^{0+}$ upon donating holes to $WSe_2$ on its surface, which confirms the previously discussed reduction process of Pt.

To observe the electronic properties of the doped $WSe_2$ FETs, back-gated FETs with the structure in Figure 2a with highly doped channels were fabricated with bilayer $WSe_2$ flakes. Figure 2b depicts the mechanism by which the carrier injection efficiency increases from thinning down the SB width by highly doping the channel. Figure 2c shows the different transfer characteristics of the different bilayer devices depending on how long the $PtCl_4$ solution was applied on the surface before drying the solution using nitrogen gas with the pristine state of the device with 60 s doping time shown as reference. Figure S4a and b show the transfer characteristics of the pristine devices with three and seven layers of pristine and doped $WSe_2$ with a 60 s doping time. The pristine devices show either slight *p*-type or ambipolar behavior, but upon doping, they all show very low gate dependence with current levels rising slightly on the negative gate bias. This indicates that the channel is heavily *p*-doped where the on-current of the


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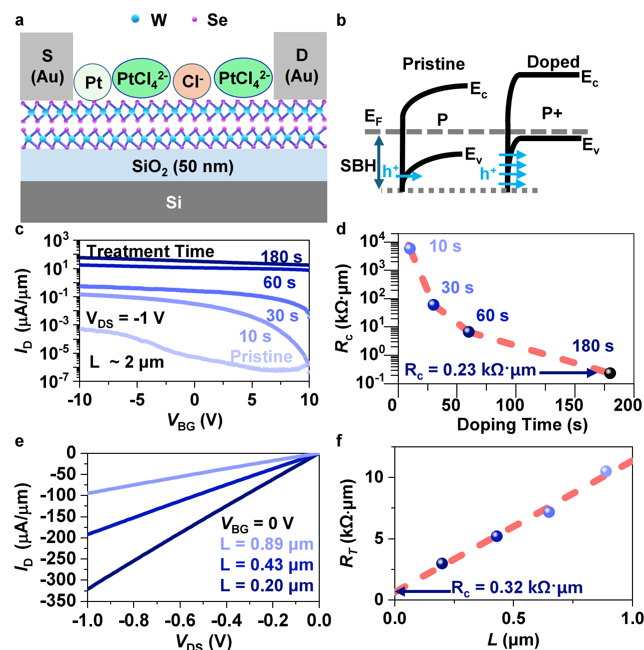


**Figure 2.** Channel-doped devices' characteristics. (a) Schematic of a channel-doped device with dopants. (b) Energy band diagram showing hole injection from the metal contact to the semiconductor channel. Despite the SB height remaining the same, the width of the SB decreases, promoting higher carrier injection via tunneling. (c) Drain current dependence on the back-gate bias shown by different doping treatment time from the pristine state to 10, 30, 60, and 180 s in contact with the doping solution before blowing away with nitrogen gas. (d) Extracted contact resistance from the curves in (c) using the YFM method. (e) Drain current dependence on the drain bias with zero back-gate bias on a TLM structure. (f) Extraction of the contact resistance using the TLM method.

two- and three-layered devices grew by more than a factor of $10^4$ for each case.

The current levels increase with higher doping treatment times, which implies a decrease in the contact resistance. This fact is highlighted in Figure 2d, where the contact resistance values of the devices were extracted from the transfer characteristics using the YFM as shown in Figure S5. The doping concentration of the bilayer devices is found to be approximately $7 \times 10^{12}$ cm$^{-2}$ after 60 s and $9 \times 10^{12}$ cm$^{-2}$ after 180 s of doping treatment. The three-layered and the seven-layered device in Figure S4 show $6 \times 10^{12}$ cm$^{-2}$ and $8 \times 10^{12}$ cm$^{-2}$, respectively, showing a similar doping level to the bilayer device with 60 s doping treatment. The 2D sheet doping concentration is calculated using the formula $p_{2D} = C_{ox}\Delta V_{th}/q$ where $C_{ox}$ is the oxide capacitance, $\Delta V_{th}$ is the shift in the threshold voltage, and $q$ is the elementary charge.[28] The result reflects a conventional behavior where the contact resistance diminishes as the doping concentration in the channel material is elevated,[29] with the lowest contact resistance from a single contact being as low as $R_c = 0.23 \pm 0.07$ kΩ·$\mu$m.

To check the validity of the contact resistance extraction, a TLM structure was fabricated on a bilayer flake using e-beam lithography to pattern submicrometer channel-length devices. The TLM device was placed in a doping treatment of 180 s, the same amount of time as the device with a contact resistance of 0.23 kΩ·$\mu$m. The output characteristics at zero gate bias are shown in Figure 2e with the current levels being 100 $\mu$A/$\mu$m or above at $V_{DS} = -1$ V even at zero gate bias for the shortest channel lengths. Moreover, the curves show a very linear dependence on the drain bias, implying that the carrier injection is more efficient in the contacts due to strong doping. The calculation of the contact resistance is shown in Figure 2f with the value of $R_c = 0.32 \pm 0.24$ kΩ·$\mu$m, which is close to the previously calculated value using YFM, hence reconfirming that our doping method induces very low contact resistance due to SB width thinning. TLM measurements for different carrier concentrations by controlling the back-gate bias are shown in Figure S6, which also yielded similar values for the contact resistance.

To explore the possibility of selectively doping only the intended regions of the channel using $PtCl_4$, we fabricated top-gated FETs with the structure shown in Figure 3a. The transfer

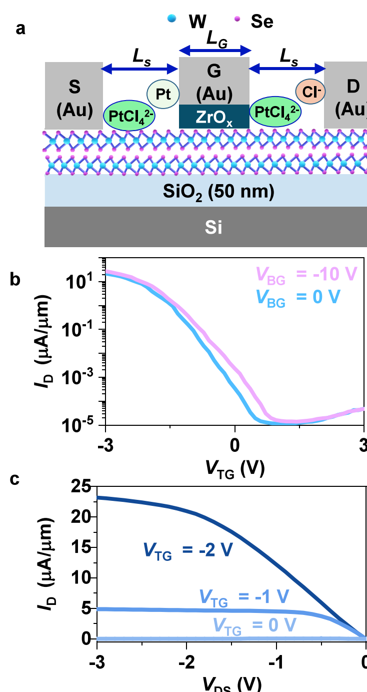


**Figure 3.** Pattern-doped devices with top gates. (a) Schematic of a top-gate device with dopants on the spacers. (b) Drain current dependence on the top-gate bias with respect to different back-gate biases after doping at $V_{DS} = -3$ V. The device has a top-gate length of $L_G$ = 2.4 $\mu$m and a spacer length $L_S$ = 0.9 $\mu$m. (c) Drain current dependence on the drain bias of the top-gate device after doping with different top-gate biases at $V_{BG}$ = 0 V of the same device in (b).

characteristics of a long-channeled top-gated device using a flake thicker than 5 nm are shown in Figure 3b. The spacer-doped devices show an on-current higher than 10 $\mu$A/$\mu$m with a subthreshold swing of approximately 300 mV/dec for both $V_{BG}$ = 0 V and $V_{BG}$ = −10 V with on−off ratios greater than $10^6$. This highlights that the level of doping greatly improved the charge injection efficiency from the contacts to the channel, with good gate control where the switching ability of the device was retained, unlike the channel-doped devices. Figure 3c shows the output characteristics of the long-channeled top-gate devices, which show linear behavior with respect to $V_{DS}$ when $V_{TG}$ is less than zero, representing the on-state of the FET, thus reconfirming that by merely doping the contact regions one can fabricate devices with higher on-currents due to the reduced SB width.


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Figure S7 shows the transfer characteristics of a device with only a 200 nm gate length, which still retains the ability to switch. This reveals that the dopants diffused less than 100 nm from each side of the spacer since if the dopant diffusion lengths were longer than the top-gate length, the transfer characteristics would be similar to the channel-doped devices in Figure 2b. This indicates that $PtCl_4$ diffuses far less than other chlorine-based dopants such as gold(III) chloride ($AuCl_3$),[7] in which the dopants traveled lengths up to $\mu$m scales. Moreover, the device displays a decent subthreshold swing of 155 mV/dec and an on−off ratio greater than $10^7$, all highlighting fine device properties with highly doped contact regions.

The dopants are also observed to be stable without any encapsulation in air at room temperature for an extended amount of time. After being placed in air for 86 days, there was only a minor shift in the transfer characteristics of a channel-doped bilayer device, as shown in Figure 4a. Also, the device

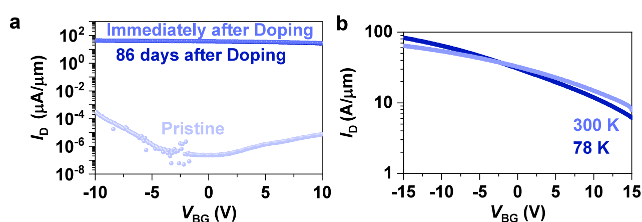


**Figure 4.** Measurements regarding the stability of the devices. (a) Drain current dependence on the back-gate bias of a channel-doped device. The channel-doped device remains almost identically doped after 86 days upon doping. (b) Drain current dependence on the back-gate bias of a channel-doped device measured at 300 and 78 K in a vacuum.

operates with slightly higher on-currents at a cryogenic temperature of 78 K at a pressure less than $10^{-5}$ Torr in Figure 4b while the degenerate level of doping is retained. The charge transfer doping is still observed in liquid nitrogen temperatures, highlighting the stability of our doping method. These measurements indicate that our doping scheme is very stable in air or vacuum environments, making it applicable to different fabrication processes and that the dopant freeze-out is nonexistent at such cryogenic temperatures.

We fabricated a channel-doped FET with the structure shown in Figure S8a to test the thermal stability of our doping scheme. The bilayer $WSe_2$ device with a channel length of 2 $\mu$m was capped with a 20 nm thick $ZrO_2$ deposited using ALD at a low temperature of 90 °C after 60 s of doping treatment with our $PtCl_4$ solution to prevent outward dopant diffusion during the annealing process. Figure S8b shows the device performance before and after ALD as well as after each rapid thermal annealing (RTA) step in a nitrogen environment. The ramp time for each annealing was set as 1 min for each temperature, and the soak time at the target temperature was held to be 0 s to represent spike annealing, a commonly used practice in CMOS processing.[30] The device behaves similarly before and after the ALD capping, also implying the stability of the dopants at temperatures near 90 °C as the ALD took approximately 16 h to complete. Moreover, the device still remains degenerately doped after 300 and 400 °C spike annealing, showing that the outward dopant diffusion can be suppressed by a simple oxide capping using ALD.

To test the dopant diffusion in lateral directions, a top-gate device with the shape shown in Figure S9a was fabricated using a $WSe_2$ flake, whose thickness is approximately 5 nm. A top gate with a 200 nm width was fabricated using 30 nm thick $ZrO_2$ to create a mask to prevent doping beneath the gate area. A 20 nm thick $ZrO_2$ capping layer was deposited as the final step after a 60 s $PtCl_4$ doping treatment to prevent outward dopant diffusion. Spike annealing was then conducted using the RTA setup in a nitrogen environment to check the thermal stability of the dopants with a 1 min ramp time for each temperature. The integrity of the top-gate dielectric, which was deposited with ALD at a low temperature, could have been compromised during the spike annealing steps. Hence, we investigated the back-gate dependence of the device before and after the spike annealing steps to solely observe any degradation in device performance by dopant diffusion after spike annealing. Figure S9b shows a representative device that is measured after $ZrO_2$ capping with the same device dimensions and flake thicknesses with the device spike annealed at 300 and 500 °C. Upon 300 °C spike annealing, the device still shows switching behaviors with similar device performance prior to annealing. Spike annealing at 500 °C also showed similar on-currents to the other two cases while also displaying a switching behavior. We believe that the stability of the dopants even at these temperatures shows that our method is highly promising in terms of their compatibility with various CMOS processing steps.[31]

In conclusion, we observed promising electronic transport properties of $WSe_2$ FETs when they were degenerately doped by using $PtCl_4$. With the doping concentrations approximately at $1 \times 10^{13}$ $cm^{-2}$, the FET shows the $R_c$ at its lowest value of 0.23 kΩ·$\mu$m, which was verified again by the extraction of $R_c$ = 0.32 kΩ·$\mu$m from TLM device measurements. The long-channel top-gated devices display switching behaviors with on-current levels of over 10 $\mu$A/$\mu$m. Moreover, the switching behavior of the top-gated FETs with underlapped regions doped with $PtCl_4$ shows that the dopant diffusion beneath the top gates is not evident even with devices with gate lengths of 200 nm while still retaining good electronic transport characteristics. The degenerately doped devices still retained a high level of doping even when being exposed to air for nearly three months and when they were held in cryogenic temperatures with vacuum. These aspects show that high-performing *p*-type $WSe_2$ FETs are realizable by doping the channel degenerately to reduce the contact resistance using a simple doping technique with high stability.

## METHODS

**Device Fabrication.** $WSe_2$ flakes were first exfoliated onto a $SiO_2$/p++Si substrate using tape and a polydimethoxysilane stamp. The substrate was then placed in a 55 °C acetone bath for 1 h to remove the residue from the tape and the stamp. Au (30 nm) contacts were used as source/drain, which were patterned by optical lithography for all devices greater than a 1 $\mu$m channel length and e-beam lithography for submicrometer channel length devices. The lift-off process after the electron beam evaporation of Au was done as the final step in placing the contacts.

The top-gated devices shown in Figure 3 and Figure S7 were fabricated with two-step lithography, where the first-step lithography patterns the source/drain contacts as previously addressed, while the second-step lithography patterns the top-gate and the oxide layer. Au (30 nm) contacts were used as


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source/drain, and Ti/Au (3 nm/30 nm) were used for the metal gate layer for the top-gate stack. The long channel device used e-beam-evaporated $ZrO_x$ (30 nm) as the gate dielectric, while the device with a 200 nm gate length used atomic layer deposition for 18 nm $ZrO_2$ as the gate dielectric.

**Doping.** Doping of the mechanically exfoliated $WSe_2$ flakes was carried out by casting a 1 wt % $PtCl_4$ solution in HCl on the flakes for each doping time and blowing it off with nitrogen gas. Subsequent annealing of the flakes was done at 130 °C on a hot plate for 3 min in ambient conditions inside a fume hood to dry the remaining solution and facilitate the charge transfer doping process due to ions such as $Pt^{2+}$ and $PtCl_4^{2-}$.

**Optical Characterization.** Raman spectroscopies were acquired by using a Horiba LabRAM HR Raman confocal imaging system. $WSe_2$ flakes were exfoliated onto a $SiO_2$/Si substrate and illuminated by a focused 532 nm laser beam. Radiation from the illuminated spot was collected and passed through a grating, separating into a spectrum, before being dispersed onto a CCD detector.

Photoluminescence (PL) measurements were gathered by using a micro-PL setup. The samples were excited with a 532 nm line source, and emission was measured with a silicon CCD (Andor Newton) connected to a spectrograph (Andor Shamrock 500i).

**X-ray Photoelectron Spectroscopy.** The chemical composition of $WSe_2$ and doped $WSe_2$ films (W 4f, Pt 4f, Se 3d, and Cl 2p) was obtained by XPS using a Kratos Axis Ultra DLD system at a takeoff angle of 0° relative to the surface normal. An Al K$\alpha$ source ($h\nu$ = 1486.6 eV) was used with a pass energy of 20 eV for the narrow scan of core levels and valence band spectra with a step size of 0.05 and 0.025 eV, respectively. The spectral fitting was conducted using Casa XPS analysis software.

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.4c02948.

Energy band diagram of the $WSe_2$−$PtCl_4$ system, AFM images of doped $WSe_2$ flake, XPS data of Se, transfer characteristics of channel-doped three- and seven-layered $WSe_2$ transistors, YFM calculations, TLM data with different back-gate biasing conditions, top-gate device transfer characteristics with 200 nm gate length, and thermal stability test data for a channel-doped and spacer-doped devices (PDF)

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### Author Contributions

I.K., N.H., and A.J. conceived the idea for the project and designed the experiments. I.K. fabricated the devices and carried out the doping process of the devices. R.R. and S.W. performed imaging of the devices. H.K. and J.G. performed optical characterization of the materials. R.P. and J.A. performed XPS measurements. I.K., N.H., and A.J. analyzed the data. I.K. and A.J. wrote the manuscript. All authors discussed the results and commented on the manuscript.

### Notes

The authors declare no competing financial interest.

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