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Fully Printed, High Performance Carbon Nanotube Thin-Film Transistors on Flexible Substrates

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Supporting Information

ABSTRACT: Fully printed transistors are a key component of ubiquitous flexible electronics. In this work, the advantages of an inverse gravure printing technique and the solution processing of semiconductor-enriched single-walled carbon nanotubes (SWNTs) are combined to fabricate fully printed thin-film transistors on mechanically flexible substrates. The fully printed transistors are configured in a top-gate device geometry and utilize silver metal electrodes and an inorganic/ organic high- κ (~17) gate dielectric. The devices exhibit excellent performance for a fully printed process, with mobility



and on/off current ratio of up to ~9 cm²/(V s) and 10⁵, respectively. Extreme bendability is observed, without measurable change in the electrical performance down to a small radius of curvature of 1 mm. Given the high performance of the transistors, our high-throughput printing process serves as an enabling nanomanufacturing scheme for a wide range of large-area electronic applications based on carbon nanotube networks.

KEYWORDS: Flexible electronics, thin-film transistors, semiconducting nanotube networks, printable electronics

C ingle-walled carbon nanotubes (SWNTs) have been widely explored as a high performance channel material for thinfilm transistors (TFTs) with high carrier mobility, low operating voltage, and solution-based processing.¹⁻⁶ In addition, SWNT networks exhibit excellent mechanical flexibility owing to their inherently small diameters. As a result, demonstration of various flexible components including integrated circuits, displays, and sensors using SWNT TFTs has been shown.^{1,5,7,8} In order to enable the use of flexible electronics for large-surface applications, printing has been proposed as a viable solution.⁹⁻¹⁴ Many advances have been made toward creating printable SWNT TFTs. The most important performance metrics for printed transistors are the carrier mobility, operation power, and device-to-device uniformity. Fully printed nanotube TFTs for applications such as radio-frequency identification, D flip-flop, and full adder have been successfully demonstrated using a combination of roll-to-roll and inverse gravure printing.¹⁵ However, the carrier mobility ($<0.1 \text{ cm}^2/(\text{V s})$) and operation voltage (>20 V) of such devices have been limited by the nature of the printed layers and the use of mixtures of metallic and semiconducting nanotubes as the active channel layer. Furthermore, these previously reported devices based on gravure printing exhibit high sensitivity to the surroundings¹⁶ due to the use of a bottom-gate device design and the lack of encapsulation, resulting in the direct exposure of nanotubes to the ambient. To improve the electrical performance, partially printed devices requiring some photolithography processes have been previously demonstrated based on semiconductor-enriched nanotubes.¹⁷ Furthermore, fully printed SWNT TFTs using ion-gel gate dielectrics have also been demonstrated to lower power dissipation.^{18,19} However, the use of ion-gel dielectrics limits the transistor speed and reliability as compared to conventional gate insulators. Despite the tremendous progress in the field, a practical processing platform for fully printed and high-performance nanotube TFTs has not yet been realized.

In this study, we demonstrate fully printed, top-gated TFTs based on 99% semiconductor-enriched nanotubes by using a scalable inverse gravure printing process with high overlay printing registration accuracy of $\pm 10 \ \mu$ m. The process scheme involves multistep printing of silver source (S), drain (D), and gate (G) metal electrodes and inorganic/organic high- κ gate dielectric on a poly(ethylene terephthalate) (PET) substrate. The resulting devices exhibit hole mobility up to ~9 cm²/(V s),

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Figure 1. Fully printed SWNT TFTs on mechanically flexible PET substrates. (a) Schematic diagram showing the printing process scheme. (b) Representative SEM image of a SWNT network deposited on a PET substrate. (c) Image of the inverse gravure printer used in this work. (d, e) Optical micrograph of a single TFT and optical image of a fully printed 20×20 device array on a PET substrate, respectively.

while having a low maximum processing temperature of 150 °C. This mobility value is the highest for a fully printed, flexible nanotube TFT and among the highest for all low-temperature solution processed devices.

Figure 1a shows the main steps for fabricating fully printed SWNT TFTs on a PET substrate (thickness of ~100 μ m; area of ~ 6 in. \times 10 in.). The substrate was first cleaned and surface modified with oxygen plasma (120 W) for 2 min. Then the surface was functionalized using poly(L-lysine) solution (0.1% w/v in water; Sigma-Aldrich) for 5 min by immersion and rinsed with deionized (DI) water to enhance subsequent SWNT adhesion.^{7,8,20} The active channel material was deposited by immersion in purified 99% semiconductorenriched SWNT solution (NanoIntegris, Inc.) for 2 h. It was then followed by a thorough rinse with DI water and dried with a nitrogen gun, resulting in uniform assembly of SWNT random network over the entire surface of the substrate. The scanning electron microscope (SEM) image in Figure 1b shows the high density (~60 SWNTs/ μ m²) of the nanotube network obtained on a PET substrate.

Using a custom-built inverse gravure printer (Figure 1c), the source and drain electrodes, gate dielectric, and gate electrode were printed in the respective order using three different plate masks. The gravure plates are chrome-plated flat copper sheets etched with regularly spaced cells (see Supporting Information, Figure S1) that together form the print patterns. The printer has a dual camera system monitoring the alignment markers on the PET substrate and the gravure plate to make fine adjustments to the stage position and rotation before each print to ensure proper alignment between layers. Inks were dropped onto the plates using pipettes and were spread evenly onto the gravure cells in the plates by using doctoring blades, with the excess pushed beyond the print contact area. The barrel, with the PET substrate attached, was then lowered to contact the gravure plate with $\sim 100-300$ N of force. Releasing the barrel rotation clutch, the stage gained control of the barrel through static friction. As the stage moves across a print length of 128 mm, the barrel rotates along with that motion, transferring the ink pattern from the gravure plate onto the PET substrate. After each layer was printed, the sample was baked in an oven at 150 °C for 1 min to evaporate the solvents and cure the inks.

The source and drain electrodes were printed from the first gravure plate using a silver nanoparticle ink (PG-007AA; Paru Corporation, Korea). The insulator was then printed using a hybrid ink consisting of high- κ barium titanate nanoparticles and poly(methyl methacrylate) (PD-100; Paru Corporation, Korea). The dielectric constant of the printed insulator film is \sim 17. The sample was then exposed to oxygen plasma (120 W) for 2 min to etch away excess SWNTs on the substrate, using the printed insulator layer as a hard mask. In the future, it is desirable to develop a more cost-effective fabrication process to conserve nanotube usage by selectively printing nanotube ink only in the active channel regions. The gate line was finally printed using the same silver nanoparticle ink. It should be noted that ink dilutions, ink doctoring speeds, and printing pressures and speeds were the main parameters adjusted for the optimization of each print layer. The details of the process for each layer are summarized in the Supporting Information. Our gravure plates were designed to print a 20×20 array of TFTs, each with a channel length, L, of ~85 μ m and width, W, of ~1250 μ m. Figures 1d and 1e show optical images of a fully fabricated SWNT TFT and the entire array, respectively. Optical images of the substrate after the printing of each layer are shown in Figure S2.



Figure 2. Electrical properties of a representative fully printed TFT. (a) Transfer characteristics of a TFT measured at $V_{DS} = -5$ and -1 V. (b) Output characteristics measured with V_{GS} from -10 to 2 V in 2 V steps. (c) Field-effect hole mobility extracted as a function of the gate voltage.



Figure 3. Statistical variation studies in the electrical properties of the fully printed TFT arrays. (a) Transfer characteristics of 66 SWNT TFTs measured at $V_{DS} = -5$ V. (b–f) Histograms of V_{th} , I_{ON}/I_{OFF} , unit-width normalized I_{ON} , unit-width normalized transconductance, and field-effect mobility, respectively.

The electrical properties of a fully printed SWNT TFT measured at room temperature and ambient air are presented in Figure 2. The as-fabricated devices are p-type as evident from the transfer characteristics (Figure 2a). The device exhibits a peak ON-current density (I_{ON}/W) of ~29 μ A/mm and peak transconductance (g_m/W) of ~3.35 μ S/mm as normalized by the channel width at $V_{DS} = -5$ V. ON to OFF current ratio (I_{ON}/I_{OFF}) is 10⁴ at $V_{DS} = -5$ V for the applied gate voltage range of -10 to 10 V. Notably, the hysteresis²¹ is minimal due to the use of a top-gate device geometry as shown in Figure S3. Output characteristics are shown in Figure 2b. Clear current saturation at high drain voltages due to pinch-off is evident. At low fields, the I-V characteristics are linear, suggesting minimal

contact resistance (i.e., Schottky barrier resistance) as compared to the channel resistance.

From the transconductance, field-effect device mobility can be extracted. The gate oxide capacitance per unit area (C_{ox}) was directly measured from parallel plate test structures on the substrate with an average value of 10.8 nF/cm². The field-effect device mobility is then extracted using the following equation: $\mu_{device} = (L/V_DC_{ox}W)(dI_d/dV_g) = (L/V_DC_{ox})(g_m/W)$. The lowfield mobility extracted at $V_{DS} = -1$ V is plotted in Figure 2c as a function of the gate voltage, and it peaks at ~8 cm²/(V s) for this device. It is worth noting that the parallel-plate capacitance value used is an overestimation of the actual gate capacitance value for the SWNT network devices since the entire substrate is not covered by nanotubes.⁷ Therefore, the extracted mobility

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Figure 4. Mechanical flexibility of the fully printed TFTs. (a) Optical image of a printed TFT under electrical measurement while bent. (b) Transfer characteristics measured at $V_{\text{DS}} = -5$ V for three different bending conditions of relaxed and bent at 4 and 1 mm radii of curvature. (c) $\Delta G/G_0$ as a function of bending radius of curvature (relaxed state is infinite curvature radius).



Figure 5. Time and operation stability of the fully printed TFTs. (a) Transfer characteristics of a device measured at $V_{DS} = -5$ V after fabrication and after 60 days of exposure to air. (b) Transfer characteristics measured at $V_{DS} = -5$ V after 1, 10, 100, and 1000 measurement cycles. (c–e) V_{th} I_{ON}/I_{OFF} , and peak field-effect device mobility as a function of measurement cycles, respectively.

value represents a lower bound. The mobility value of our printed TFTs is among the highest for solution processed TFTs processed at room temperature. Yet, the mobility of a single SWNT is >4000 cm²/(V s).⁶ This is expected given that for SWNT random networks the charge transport is limited by the nanotube—nanotube junctions rather than transport across individual tubes. In the future, further optimization of nanotube density, and thereby junction density, should result in improved device mobility.

Next we focus on the uniformity of the fabricated devices. The functional device yield is ~66% with the rest of the devices being nonfunctional due to short due to ink smearing for the S/ D pattern formation and/or gate leakage through pinholes in the insulator. The yield is respectable given that the printing process was not performed in a cleanroom environment with humidity control, and the printer was not placed on a vibration isolated table and/or floor. Figure 3a shows the transfer characteristics of 66 TFTs on a PET substrate measured at $V_{\rm DS}$

= -5 V. Figure 3b-e shows the histograms of the statistical variations in threshold voltage ($V_{\rm th}$), $I_{\rm ON}/I_{\rm OFF}$, $I_{\rm ON}/W$, $g_{\rm m}/W$, and field-effect device mobility, respectively. V_{th} was calculated by locating the max g_m point of each transfer characteristic curve and extrapolating a line tangent to the curve at that point to find the zero crossing voltage. The $V_{\rm th}$, $I_{\rm ON}/I_{\rm OFF}$, $I_{\rm ON}/W$, and $g_{\rm m}/W$ were measured at $V_{\rm DS}$ = -5 V, and the low-field mobility was extracted as described above at $V_{\rm DS}$ = -1 V. The best performances measured, from different devices, are $I_{\rm ON}/I_{\rm OFF}$ of 5.7×10^5 , $I_{\rm ON}/W$ of 32.2 μ A/mm, $g_{\rm m}/W$ of 5.69 μ S/mm, and field-effect device mobility of 9.13 cm²/(V s). The $V_{\rm th}$ lies in the negative range, making the devices enhancement mode p-FETs, which is desirable from a circuit design point of view. The average of $\log(I_{ON}/I_{OFF})$, I_{ON}/W , g_m/W , mobility, and V_{th} are 4.55 ± 0.87 , $19.5 \pm 9.68 \ \mu\text{A/mm}$, $2.47 \pm 1.10 \ \mu\text{S/mm}$, $4.27 \pm$ 1.62 cm²/(V s), and -2.29 ± 1.15 V, respectively. The device uniformity is good given that the entire processing was performed outside of a cleanroom environment. In the future,

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the yield and uniformity may be further enhanced by process optimization (e.g., optimization of the inks and printing parameters), the use of a cleanroom facility, and using high purity level solvents.

Mechanical flexibility of the printed TFTs was also characterized. Because of the inherently small diameter of SWNTs (1-2 nm), the random network-based devices are expected to exhibit excellent mechanical flexibility as long as the metal and dielectric layers are also kept thin and/or flexible. Here, the thicknesses of the printed source and drain, gate insulator, and gate electrodes are ~2.5, 1.5, and 1.25 μ m, respectively, as measured by a profilometer. Although the printed metal and insulator layers are relatively thick, the polymer binders contained in their respective inks aid the mechanical flexibility of the printed layers, allowing the device performance to remain stable even when bent to the extreme. Figure 4a shows an optical image of a device being electrically measured as the substrate is bent along the channel length. Transfer characteristics measured at $V_{\rm DS} = -5$ V of a device without (i.e., flat) and with bending down to 1 mm radius of curvature are shown in Figure 4b. The results show that the TFTs can be operated without noticeable degradation in electrical performance when severely bent. This observation is further highlighted in Figure 4c where the normalized change in conductance, $\Delta G/G_0$, where ΔG is the change in conductance as a function of bending and G_0 is the conductance at the relaxed state, is shown in Figure 4c. This shows that our fully printed SWNT TFTs are well suitable to be used to conform to curved surfaces.

Finally, the stability of the printed nanotube TFTs as a function of time and operation cycle is examined. An advantage of the top-gate device geometry used in this work is the direct encapsulation of the SWNT network by the gate stack rather than their exposure to the ambient. A device was measured immediately after fabrication and again after 60 days of exposure to ambient air to examine the stability over time. As shown in Figure 5a, a shift in $V_{\rm th}$ of ~1 V was observed with no other serious degradation in device performance. While this stability is good for a printed device, it may be further improved in the future by using a proper encapsulant for packaging purposes to fully isolate the devices from the environment. The stability over 1000 electrical measurement cycles was also tested and is shown in Figure 5b-e. The transfer characteristics $V_{\rm th}$, $I_{\rm ON}/I_{\rm OFF}$, and field-effect device mobility all remain nearly unchanged after 1000 measurement cycles. The results suggest that the devices presented here exhibit good stability over usage and time and are ideal for reliable large-area electronics.

In conclusion, we have demonstrated a fully printed TFT process that incorporates the use of 99% semiconductorenriched nanotubes as the active channel material along with a printed high- κ gate dielectric. The top-gated devices exhibit excellent mobility (up to ~9 cm²/(V s)), operation stability, and uniformity for a fully printed process scheme. In the future, the printed TFT arrays can be readily configured as the activematrix back-plane for a number of applications, including largearea sensor networks (e.g., electronic skin) and mechanically flexible displays. Notably, the inverse gravure printing process used here is potentially adaptable into a roll-to-roll gravure printing setup for even higher throughput and larger area device processing. In the future, further scaling of the channel length down to sub-10 μ m may be feasible through optimization of the ink formulation and printing process parameters. This work presents an important advance toward the practical use of nanotube networks for large-area electronics.

ASSOCIATED CONTENT

Supporting Information

Cell structure of gravure mask plates; detailed print parameters for each layer; optical images of the substrate after each printed layer; hysteresis measurements of fully printed TFTs. This material is available free of charge via the Internet at http:// pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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Supporting Information

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Cell structure of gravure mask plates

The cells in the gravure plates are rounded squares with sides of $\sim 115 \mu m$ in length and are $\sim 15 \mu m$ deep. They together form the patterns for the various layer masks. The optical microscope images of the patterns for each layer (for a single TFT) are shown in Figure S1.



Figure S1. Optical micrographs of the gravure mask patterns. (a) Source/drain (S/D) contacts, (b) gate insulator, and (c) gate metal line (middle finger) along with the S/D bonding pads.

Detailed print parameters for each layer

The source and drain layer was printed using the as-received silver nanoparticle ink (PG-007AA; Paru Corporation Korea) without further dilution. The ink was spread across the gravure mask in both directions by doctoring blades. The barrel was lowered with ~ 150 N of force, and the final print was completed with the stage moving at ~ 50 mm/s.

The gate insulator layer was printed using barium titanate nanoparticle ink (PD-100; Paru Corporation Korea) diluted with dietylene glycol butyl ether at a weight ratio of 4:1. The ink was spread across the gravure mask in both directions by doctoring blades. The barrel was lowered with ~ 250 N of force, and the final print was completed with the stage moving at 20 mm/s.

The gate layer was printed using silver nanoparticle ink (PG-007AA; Paru Corporation Korea) diluted with etylene glycol at a weight ratio of 10:1. The ink was spread across the gravure mask in one direction by the doctoring blade. The barrel was lowered with \sim 300 N of force, and the final print was completed with the stage moving at 35 mm/s.

The stage moves at 100 mm/s for all steps when doctoring the ink.

Optical micrographs after each printed layer



Figure S2. Optical micrographs of a TFT after each printing step. (a) Source and drain contacts, (b) gate insulator, (c) removal of excess SWNTs using O₂ plasma, (d) gate fingers and source/drain contact pads.

Hysteresis measurements in the transfer characteristics of fully-printed SWNT TFTs



Figure S3. Double-sweep measurements of the transfer characteristics. Transfer characteristics of a TFT measured at $V_{DS} = -5$ V (red) and -1 V (black), with V_{GS} sweeping from -10 to 10 V and back to show the hysteresis. Only minimal hysteresis is observed.