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Self-Aligned, Extremely High Frequency III−V Metal-Oxide-Semiconductor Field-Effect Transistors on Rigid and Flexible Substrates

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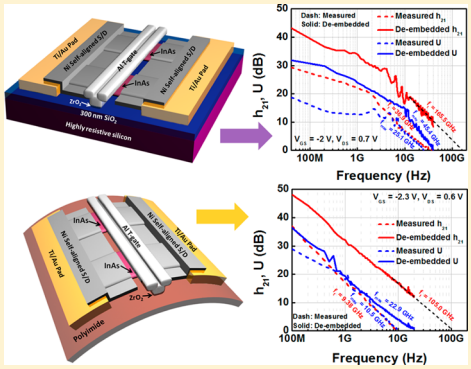
Supporting Information

ABSTRACT: This paper reports the radio frequency (RF) performance of InAs nanomembrane transistors on both mechanically rigid and flexible substrates. We have employed a self-aligned device architecture by using a T-shaped gate structure to fabricate high performance InAs metal-oxide-semiconductor field-effect transistors (MOSFETs) with channel lengths down to 75 nm. RF measurements reveal that the InAs devices made on a silicon substrate exhibit a cutoff frequency (f_t) of ∼165 GHz, which is one of the best results achieved in III−V MOSFETs on silicon. Similarly, the devices fabricated on a bendable polyimide substrate provide a f_t of ∼105 GHz, representing the best performance achieved for transistors fabricated directly on mechanically flexible substrates. The results demonstrate the potential of III−V-on-insulator platform for extremely high-frequency (EHF) electronics on both conventional silicon and flexible substrates.



KEYWORDS: *III−V-on-insulator, XOI, two-dimensional membranes, radio frequency transistors, flexible electronics*

The growing demand on larger bandwidth for wireless communications has stimulated the quest for transistors that can be operated at fastest possible frequencies. Besides the conventional silicon metal-oxide-semiconductor field-effect transistors (MOSFETs),[1] various types of nanomaterial systems including carbon nanotubes,[2−7] graphene,[8−11] and III−V nanowires[12−14] have been heavily explored for radio frequency (RF) applications. However, none of these material platforms have yet offered transistors that can surpass the performance achieved in III−V high electron mobility transistors (HEMTs).[15−20] The record-high cutoff frequency (f_t) for InAs-based HEMTs has already reached 644 GHz for 30 nm long devices on InP substrates.[17] Despite the tremendous success in III−V HEMT research, the platform still has a few inherent limitations. First of all, sophisticated epitaxial growth is needed to grow multiple layers with desired chemical compositions in order to form the quantum well structures. Second, due to the use of epitaxial processes, the selection of substrate is limited to expensive III−V bulk substrates such as InP or GaAs, or in some cases, silicon with thick buffer layers. Third, such HEMT devices are not compatible with flexible electronics, which has attracted significant amount of interest recently.

In light of the above-described limitations faced by III−V HEMTs, we have previously reported a III−V-on-insulator, or "XOI" approach,[21] which enables the transfer of ultrathin, two-dimensional III−V membranes to virtually any type of handling substrate using a facile contact printing process.[22,23] The use of the ultrathin III−V membranes allows optimal gate control and offers transistors with minimal short channel effects, which is especially important for a small bandgap semiconductor such as InAs.[24] Using this XOI platform, we have already demonstrated high-performance InAs[24] and InAsSb[25] n-MOSFETs and InGaSb-based[26] p-MOSFETs on silicon support substrates. In addition, the XOI platform enables easy fabrication of transistors on mechanically flexible substrates. Previously, the best reported cutoff frequencies for the flexible transistors made with various types of material platforms including carbon nanotube,[27] graphene,[28] silicon,[29,30] and III−V nanowires[31,32] typically lie in the range of a few hundred megahertz to sub-10 gigahertz. The work by Rogers et al. has demonstrated the potential of using GaAs membranes for high-performance flexible RF electronics.[23] However, the reported cutoff frequency of 2 GHz is only modest due to the relatively long

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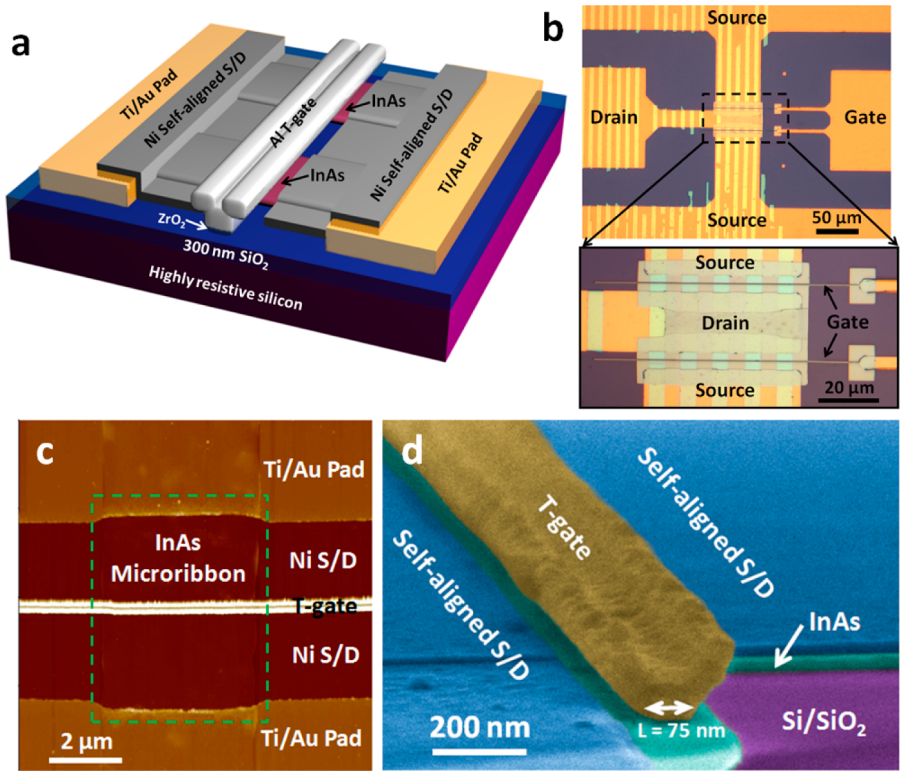

Figure 1. Self-aligned fabrication of InAs XOI MOSFETs on silicon substrates. (a) Schematic of a self-aligned InAs XOI MOSFET with an aluminum/ZrO_2 T-shaped gate stack, and self-aligned nickel S/D extensions. (b) Optical microscope images of a self-aligned XOI RF transistor. (c) AFM and (d) cross-sectional SEM images (false color) of the device.

channel length used without self-aligned source/drain contact electrodes in respect to the gate.

In this paper, we study the RF characteristics of transistors fabricated using InAs XOI platform. Transistors with T-shaped gate electrodes are fabricated in order to obtain source/drain (S/D) contacts self-aligned to the gate electrode to allow minimal parasitic capacitances and resistances.[33] It is well-known that the cutoff frequency (f_t) and maximum oscillation frequency (f_{max}), which are two most important figures of merit for RF transistors, can be predicted using the following relations[34]

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (1)$$

$$f_{max} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd} + g_d(R_g + R_s)}} \approx \sqrt{\frac{f_t}{8\pi R_g C_{gd}}} \quad (2)$$

where g_m is the transconductance, C_{gs} and C_{gd} are the gate/source and gate/drain capacitances, respectively, R_g and R_s are the gate and source series resistances, respectively, and g_d is the output conductance. The reduced parasitic capacitances and resistances provided by the self-aligned T-gate design would thereby lead to enhanced RF performance. Meanwhile, the use of InAs channel with a high saturation velocity of electrons (1.3×10^7 cm/s for bulk)[35] combined with short gate lengths (i.e., sub-100 nm) lead to high g_m, which is optimal for high frequency operation.

RF measurements of InAs XOI MOSFETs with self-aligned T-gate architecture reveal that the devices made on a silicon substrate exhibit a f_t of ~165.5 GHz, which is one of the best results achieved in III–V MOSFETs on a Si substrate. The performance is truly impressive considering the simple fabrication process used on a conventional Si handling wafer, as opposed to the sophisticated multiepitaxial-layer structures of the III–V HEMTs. Similarly, the devices fabricated on flexible substrate provide a f_t of 105 GHz. The result is more than 10 times better than the fastest flexible devices reported in the literature made with graphene (f_t = 8.7 GHz),[28] another widely studied two-dimensional (2D) material for RF applications. This work demonstrates the successful operation of flexible III–V MOSFETs at extremely high frequency (EHF) regime (30 to 300 GHz) for the first time. Although impressive performance has been previously demonstrated by bonding HEMT devices fabricated on conventional epitaxial substrate to flexible substrate,[36] our work represents the best performance achieved for transistors fabricated directly on mechanically flexible substrates. Our results indicate the RF device potential of XOI platform and provide a viable approach for future flexible electronics when ultrahigh performance transistors are needed for large bandwidth wireless communication applications.

The schematic of a self-aligned InAs XOI MOSFET is shown in Figure 1a. For DC measurements, the transistors are fabricated on a heavily doped (ρ < 0.005 Ω·cm) silicon wafer to allow back-gate biasing in addition to the T-gate, while for RF measurements, a highly resistive silicon wafer (ρ = 10 kΩ·cm) with 300 nm thick SiO_2 was used to ensure minimum parasitic capacitances from the substrate. InAs microribbons with a width and spacing of ~5 μm and a nominal thickness of ~15 nm is transferred onto a Si wafer using a contact printing method as described in our previous publications.[21] According to our previous study, a field-effect mobility of around 2300 $cm^2\ V^{-1}\ s^{-1}$ can be achieved in such 15 nm thick InAs

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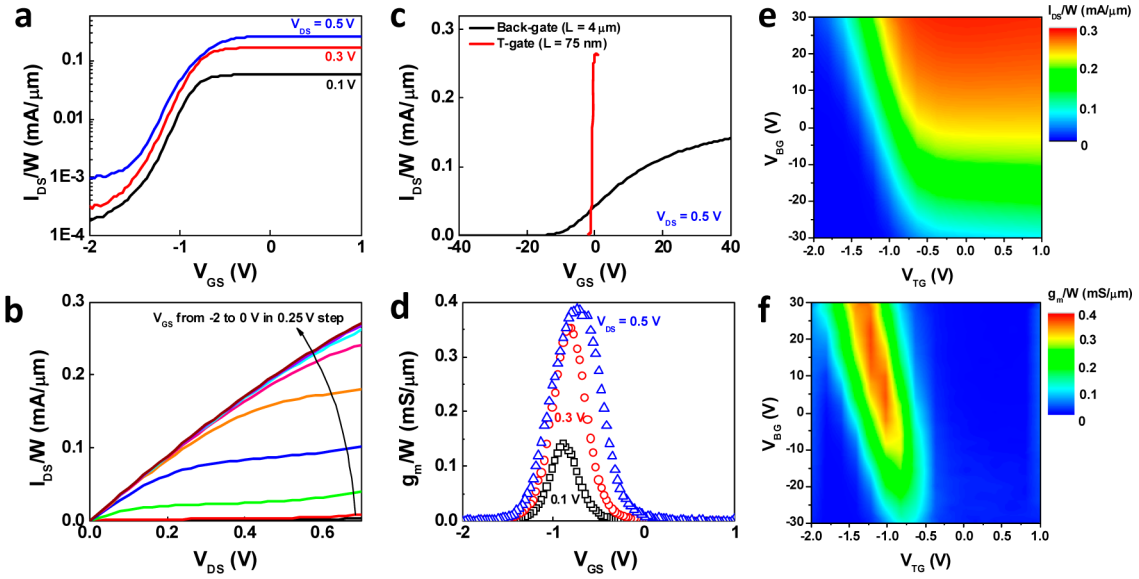

Figure 2. DC characteristics of the self-aligned InAs XOI MOSFET fabricated on Si/SiO_2 substrate. (a) $I_{DS}-V_{GS}$ characteristics of a self-aligned InAs MOSFET (L = 75 nm, W = 50 μm). (b) $I_{DS}-V_{DS}$ characteristics of the same device measured at various V_{GS} from −2 to 0 V. (c) $I_{DS}-V_{GS}$ characteristics of the device measured with back-gate (black trace) and self-aligned top gate (red trace) at V_{DS} = 0.5 V. (d) g_m-V_{GS} characteristics of the same device in (a). (e,f) Contour plots showing I_{DS}/W (e) and g_m/W (f) as a function of the top gate (V_{TG}) and back gate (V_{BG}) voltages.

nanomembranes.[21] Subsequently, Ti/Au probing pads are first patterned using photolithography and T-shaped Al/ZrO_2 gate stacks are defined using electron-beam (e-beam) lithography, atomic layer deposition of ZrO_2 (thickness, 10 nm) at 130 °C, evaporation of Al (thickness, 110 nm), and a lift-off process. As a final step, directional deposition of Ni (20 nm) on the T-gate forms the self-aligned S/D contacts and concludes the device fabrication. More details about the device fabrication process can be found in the Supporting Information (Figure S1).

The optical microscope images of a completed InAs RF transistor on a Si substrate is shown in Figure 1b, where the device is configured into the ground−signal−ground (GSG) coplanar waveguide structure to allow microwave measurements. As shown in the zoom-in optical microscope image, the device consists of a pair of MOSFETs with a channel width of 50 μm each. Each 50 μm wide MOSFET contains five uniformly spaced ribbons with an effective channel width of ~25 μm. The corresponding atomic force microscopy (AFM) and cross-sectional scanning electron microscopy (SEM) images showing the active region of the MOSFETs are exhibited in Figure 1c,d, respectively. From the SEM image, one can find that the S/D electrodes are self-aligned to the T-shaped gate. The T-gate has a base-length of ~75 nm and a tip-length of ~244 nm. The length of the ungated channel regions, corresponding approximately to the difference between tip- and base-lengths of the gate is ~85 nm for both source and drain contacts.

We first characterized the DC performance of the self-aligned InAs XOI MOSFETs on silicon substrates, and the results are summarized in Figure 2. The transfer ($I_{DS}-V_{GS}$) and output ($I_{DS}-V_{DS}$) characteristics of a representative device are presented in Figure 2a,b, respectively. The data is normalized to the total width of the InAs microribbons, which is 25 μm for this particular device. From the $I_{DS}-V_{GS}$ curves, one can find that the on-state current density (I_{on}/W) of the device measured at V_{DS} = 0.5 V and V_{GS} = 1 V is ~0.26 mA/μm, average current on/off ratio (I_{on}/I_{off}) is ~500, and the subthreshold slope (SS) is 310 mV/dec Note that the SS is higher than the values reported in our previous reports,[21,24] because the forming gas (5% H_2 in N_2) anneal process at 170 °C, known to improve the SS significantly,[24] is not compatible with the gate-first fabrication process used in this work. Specifically, diffusion of the metal atoms into the dielectric was observed at elevated temperatures. In the future, the use of high-temperature metals, such as TiN and TaN need to be explored to enable a forming gas anneal to further improve the $InAs/ZrO_2$ interface.

From the $I_{DS}-V_{DS}$ characteristics presented in Figure 2b, one can roughly estimate the carrier saturation velocity (ν_{sat}) in InAs membranes using the current equation below for classical MOSFETs with velocity saturation[34]

$$I_{Dsat} = W(V_{GS} - V_{th})C_{ox}\nu_{sat}$$

where I_{Dsat} is the saturation current, V_{th} is the linear extrapolated threshold voltage, and C_{ox} is the parallel plate capacitance for 10 nm ZrO_2 ($\varepsilon \sim 13$). The ν_{sat} is estimated to be ~0.77×10^7 cm/s for an applied electric field of 28.7 kV/cm, which is close to the value reported in the literature.[35] Furthermore, Figure 2c compares the $I_{DS}-V_{GS}$ characteristics measured with the back-gate (black trace) and self-aligned top gate (red trace) at V_{DS} = 0.5 V. From the figure, it is obvious that with the use of high-κ ZrO_2 dielectric (ε = 13, effective oxide thickness EOT = 3 nm), the top-gate is significantly stronger than the back-gate (EOT = 300 nm), which requires −40 to 40 V to achieve similar amount of gate modulation.

Figure 2d shows the transconductance (g_m-V_{GS}) curves derived from the $I_{DS}-V_{GS}$ characteristics. The maximum g_m is measured to be 0.39 mS/μm when V_{GS} and V_{DS} are at −0.8 and 0.5 V, respectively. Although this value is already respectable, it is lower than the best value reported in our previous publication by a factor of ~4×.[24] This is likely to be limited by the source/drain contact resistance and/or series resistance of the ungated regions arising from the tip to base length ratio of the T-gate. According to the SEM image in Figure 1d, the underlapped region is around 85 nm for both the source and drain sides, and the corresponding series plus contact resistance

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(R_S, R_D) is estimated to be around 900 Ω·μm (Supporting Information Figure S2).

By applying back-gate bias through the substrate, the contribution from the ungated region to the S/D series resistance is examined. Figure 2e,f shows the contour plots of I_{DS}/W (Figure 2e) and g_m/W (Figure 2f) as a function of the top gate (V_{TG}) and back gate (V_{BG}) voltages for the self-aligned InAs XOI MOSFET. The results indicate that as the V_{BG} changes from 0 to 30 V, I_{on}/W only increases slightly from 0.26 to 0.3 mA/μm, and the maximum g_m remains almost constant. This indicates that the ungated regions do not contribute significantly to the series resistance. Therefore, the S/D contact resistance should be the limiting factor for the overall device performance. Annealing of the devices in N_2 at 300 °C prior to the formation of the gate stack was previously found to drastically reduce the contact resistance values[24,37] as also shown in the Supporting Information (Figure S3). However, contact thermal annealing is not compatible for the gate-first process scheme studied in this work. Annealing at 300 °C causes the Ni atoms of the gate metal to diffuse into the gate dielectric, resulting in low I_{on}/I_{off}. As shown in the Supporting Information (Figure S2), after subtracting the measured contact resistance (from transmission line method), the intrinsic transconductance (g_{mi}) is extracted to be ~3 mS/μm at V_{DS} = 0.5 V, which is consistent with our previously reported value.[24] In the future, gate stacks with higher thermal budgets need to be developed to enable contacting annealing of Ni S/D electrodes, and thereby, further reducing the contact resistances. Moreover, according to Figure S3 shown in the Supporting Information, the contact resistance increases as the thickness of InAs membrane gets smaller. Therefore, for the future ultimately scaled transistors with thinner InAs channel, n-doping of InAs near the metal contacts need to be explored to further reduce the contact resistance.

The RF performance of a self-aligned InAs XOI RF transistor (dual channel with L = 75 nm and W = 50 μm) on a highly resistive silicon substrate is characterized using a vector network analyzer (Anritsu 37397C). For the measurements, the source contacts are grounded, and the DC biases are supplied to the gate and drain terminals through the bias-T. The gate is biased at V_{GS} = −2 V and the drain is biased at V_{DS} = 0.7 V, as this is the bias point that gives the maximum g_m determined from the DC measurements. Note that this device has slightly different threshold voltage (V_{th}) compared to the device presented in Figure 2 due to the difference of substrate work function and/or process variations. The measured S-parameters from 40 MHz to 40 GHz are plotted in Figure 3a. From the S-parameters, the as-measured current gain (h_{21}) and Mason's unilateral gain (U) are extracted and plotted as a function of frequency (Figure 3b). The as-measured f_t and f_{max}, which are defined as the frequencies that h_{21} and U drop to 0 dB, are found to be 36.9 and 25.1 GHz, respectively.

The as-measured f_t and f_{max} of the transistors are largely affected by the parasitic pad capacitances and inductances. In particular, considering the small size of the transistor channel in comparison with the GSG pads incorporated for probing measurements, the parasitics could drastically degrade the corresponding AC performance. Such parasitics can be easily subtracted by performing an on-chip open/short de-embedding (Supporting Information S4) and the de-embedded h_{21} and U of the device can be deduced, which are plotted as the solid traces in Figure 3b. From the figure, the de-embedded f_t and f_{max} are found to be 165.5 and 45.4 GHz, respectively. The

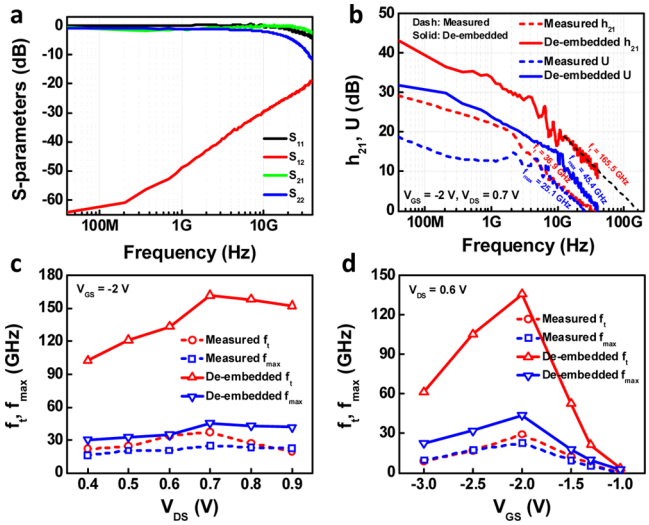

Figure 3. RF characteristics of self-aligned InAs XOI MOSFETs on Si. (a) Measured S-parameters for a self-aligned InAs XOI RF transistor (dual channel with L = 75 nm, W = 50 μm) from 40 MHz to 40 GHz. The transistor is biased at V_{GS} = −2 V and V_{DS} = 0.7 V for maximum performance. (b) As-measured (dash) and de-embedded (solid) current gain (h_{21}) and Mason's unilateral gain (U) derived from the S-parameters from 40 MHz to 40 GHz. The de-embedded current gain cutoff frequency is 165.5 GHz. (c,d) As-measured (dash) and de-embedded (solid) cutoff frequencies as a function of V_{DS} (c) and V_{GS} (d).

observed f_t = 165.5 GHz for a 75 nm long transistor represents the best frequency response currently achieved in III−V-based MOSFETs on silicon substrates. Furthermore, considering the fact that f_t is proportional to g_m, the ultimate performance (i.e., intrinsic f_t) of our self-aligned XOI RF transistor is projected to be ~1.27 THz when removing the effect of contact resistance. This projection is obtained by replacing g_m with the extracted g_{mi} of 3 mS/μm from the DC measurements in the f_t equation.

We also note that f_{max} is lower than f_t for our devices, which can be attributed to the loss from the parasitic gate resistance. As shown in the Supporting Information (Figure S5), we have established a small-signal equivalent circuit model to extract the device parameters from the measured S-parameters and the values are summarized in Table 1. R_g is extracted to be 180 Ω, which could limit the f_{max} performance according to eq 2. In the future, optimized multifinger layout design can be employed to minimize the gate resistance and further improve f_{max} of the transistors. Additionally, the intrinsic gain of our InAs XOI RF transistor is $g_m R_{ds}$ = 9.24, which is high for such a small channel length.

The drain bias and gate bias dependency of the cutoff frequencies are studied and illustrated in Figure 3c,d, respectively. As the V_{DS} increases, the f_t and f_{max} peaks at 0.7 V, and then starts to decrease slightly (Figure 3c), which is likely resulted from the heating of the InAs membranes. Under various gate biases from −3 to −1 V, the f_t and f_{max} also vary and peak at V_{GS} = −2 V (Figure 3d). The variations of f_t and f_{max} follow the variation of g_m since they are directly proportional.

The XOI platform is also compatible with mechanically flexible substrates.[22,23] As a demonstration, we report self-aligned InAs XOI MOSFETs fabricated on a bendable polyimide (PI) substrate. The fabrication process involves the spin coating and curing of polyimide (HD MicroSystems, Inc.

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Table 1. Extracted Device Parameters for the InAs XOI RF Transistor Presented in Figure 3

g_m	R_s	R_d	R_g	R_{ds}	R_{NQS}	C_{gs}	C_{gd}	C_{ds}
14 mS	17.8 Ω	17.8 Ω	180 Ω	660 Ω	14.3 Ω	8.5 fF	4.8 fF	22.9 fF

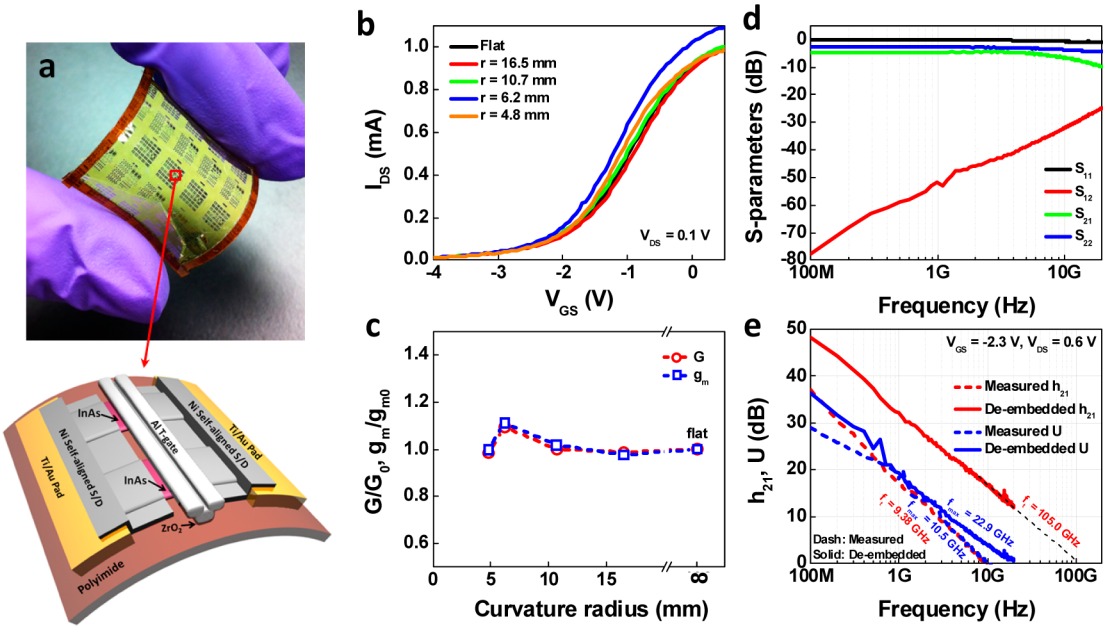

Figure 4. RF characteristics of self-aligned InAs XOI MOSFETs on mechanically flexible substrates. (a) Photograph of self-aligned flexible InAs XOI MOSFETs fabricated on a polyimide substrate. Inset: schematic of the device. (b) $I_{DS}-V_{GS}$ characteristics of a flexible device measured under various curvature radii at V_{DS} = 0.1 V. The average I_{on}/I_{off} ratio is ∼100 and the average I_{on}/W is ∼0.04 mA/μm at V_{DS} = 0.1 V. (c) Normalized on-state conductance (G/G_0) and maximum transconductance (g_m/g_{m0}) as a function of curvature radius. (d) Measured *S*-parameters for a device (dual channel with L = 75 nm, W = 50 μm) from 100 MHz to 20 GHz. The transistor is biased at V_{GS} = −2.3 V and V_{DS} = 0.6 V for maximum performance. (e) As-measured (dash) and de-embedded (solid) h_{21} and U derived from the *S*-parameters from 100 MHz to 20 GHz. The de-embedded current gain cutoff frequency is 105 GHz.

PI-2525) onto a silicon handling wafer, resulting in a film thickness of ∼12 μm. Subsequently T-gate MOSFETs are fabricated using the process scheme described above, followed by deposition of a parylene passivation layer (thickness, 500 nm). Finally, the PI substrate is detached from the handling wafer after the fabrication is completed.[12,38] It is important to point out that parylene passivation layer is used in order to encapsulate the devices to avoid the delamination of the InAs membranes from the substrate or the shortage between the gate and source/drain during the peel-off process.

An optical photograph of a PI substrate with self-aligned InAs RF MOSFETs is shown in Figure 4a. The device schematic is also shown. The devices show excellent mechanical robustness with minimal performance change under various curvature radii down to 4.8 mm (Figure 4b). The normalized on-state conductance (G/G_0) and maximum transconductance (g_m/g_{m0}) as a function of curvature radius are shown in Figure 4c, where g_{m0} and G_0 are the transconductance and on-state conductance in the relaxed state. The results indicate that the performance change is within 11% under all bending conditions tested. Furthermore, RF characterizations (Figure 4d,e) from 100 MHz to 20 GHz show that the flexible InAs MOSFET has an impressive de-embedded f_t of 105 GHz.

For practical mixed-signal integrated circuits, most of the modules such as digital signal processing (DSP), analog-to-digital converter (ADC), digital-to-analog converter (DAC), and IF-band amplifiers are typically operating at moderate frequencies (a few hundred MHz to low GHz). While power amplifiers (PA) and RF front-end such as low-noise amplifier (LNA) and mixer may require a few transistors that can be operated at faster speeds (a few GHz to tens of GHz). In the future, one can envision flexible electronic systems based on a few InAs XOI MOSFETs on a small-area that are heterogeneously integrated with low-cost-material-based transistors on large-area substrates. This represents a high-performance yet cost-effective approach. Furthermore, our XOI platform is also universal to all types of III−V material systems. Therefore, despite the relatively low breakdown field and power handling capability of InAs due to its small bandgap, it is possible to heterogeneously integrate multiple III−V materials on the same substrate for different applications. For instance, it would be attractive to have an integrated system with InAs XOI transistors in the high-speed RF front-end such as low-noise amplifiers and mixers, and GaN[39] XOI transistors in components such as the power amplifiers.

In summary, RF performance of InAs XOI MOSFETs is explored through the use of self-aligned device geometry. Compared with graphene, which is another 2D material that has been widely studied for RF applications, the ultrathin III−V membranes used in this study exhibit comparable frequency response on Si substrate and in the meantime offer higher I_{on}/I_{off}. Although for RF applications, the requirement on I_{on}/I_{off} is more relaxed as compared to digital applications, low I_{on}/I_{off} still limits the possible applications such as high efficiency power amplifiers. Our well-established XOI platform, coupled with the self-aligned device design, could provide a viable and simple approach to enable heterogeneous integration of high-speed III−V transistors with silicon CMOS. It could also serve

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as a foundation for ultrahigh speed flexible electronics for large bandwidth wireless communication applications.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Details about the self-aligned XOI MOSFET fabrication process (S1); contact resistance and intrinsic transconductance g_{mi} (S2); effect of contact anneal (S3); on-chip open/short de-embedding for intrinsic RF performance (S4); and small signal RF modeling to extract the device parameters from the measured *S*-parameters (S5). This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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Self-Aligned, Extremely High Frequency III-V Metal-Oxide-Semiconductor Field-Effect Transistors on Rigid and Flexible Substrates

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Supporting Information

S1. Details about the self-aligned XOI MOSFET fabrication process

The fabrication process for the self-aligned XOI MOSFET is illustrated in Figure S1. The GaSb source wafer with 15-nm-thick InAs and 60-nm-thick $Al_{0.2}Ga_{0.8}Sb$ sacrificial layer grown by molecular beam epitaxy (MBE) is patterned and etched into microribbons using previously reported process conditions.[1] The AlGaSb layer is then selectively wet etched using NH_4OH solution to achieve freestanding InAs active layers, which are subsequently transferred onto the target substrate using a PDMS slab. On top of the transferred InAs microribbons, Ti/Au (5/35 nm) probing pads are first patterned using photolithography and lift-off processes. T-shaped gate is then patterned using electron beam (e-beam) lithography with a bilayer e-beam resist of Poly(methyl methacrylate) (PMMA) and copolymer P(MMA-MAA), which has higher exposure sensitivity than PMMA. The gate stack is subsequently formed using a lift-off process with 10 nm of high-κ ZrO_2 dielectric deposited by low-temperature (130 ˚C) atomic layer deposition (ALD) and 110 nm of Al deposited using e-beam evaporation. As a final step, an opening window is patterned across the channel region using e-beam lithography and 20 nm Ni is deposited to allow the formation of self-aligned S/D contacts due to the shadow effect from the T-shaped gate.

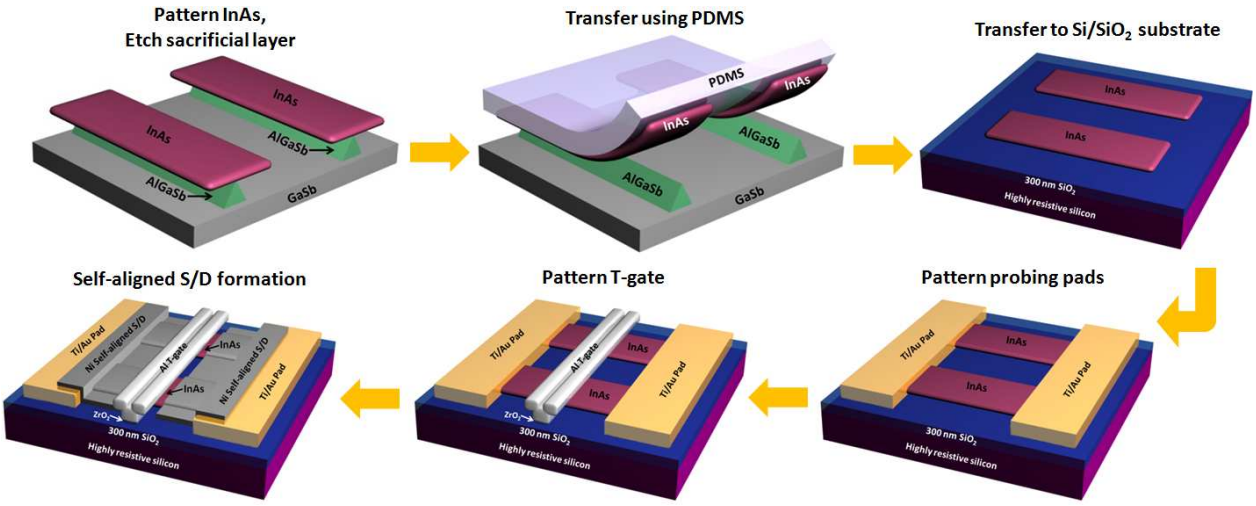

Figure S1. Schematic illustration of the self-aligned XOI MOSFET fabrication process.

S2. Contact resistance and intrinsic transconductance g_{mi}

I_{DS}-V_{GS} curves saturate at V_{GS} larger than -0.5 V, which is resulted from the source/drain series resistance. The total output resistance (R_{SD}) is calculated to be ~1.8 kΩ·μm for all V_{DS} biases (gray dashed lines in Figure S2a). The series resistance works like a source degeneration resistor and reduces g_m of the transistor. By excluding the effect of the source/drain series resistance, we can deduce the intrinsic transconductance (g_{mi}) of the transistor using the relation $g_{mi} = g_m/(1-g_mR_S-g_dR_{SD})$. In this relation, g_m values are taken from Figure 2d, R_S = 900 Ω·μm is one half of R_{SD}, and g_d is the output conductance (Figure S2b and c), which is obtained by taking derivative of the output (I_{DS}-V_{DS}) characteristics shown in Figure 2b. Using the above values, g_{mi} under various V_{GS} biases are extracted as shown in Figure S2d. The maximum g_{mi} at V_{DS} = 0.5 V is ~3 mS/μm, which is much higher than the extrinsic value of 0.39 mS/μm. This indicates the potential of further improvement of our device performance by reducing the contact resistances. If a device transconductance close to g_{mi} is experimentally achieved, the self-aligned XOI MOSFETs can potentially be operated at above-terahertz regime.

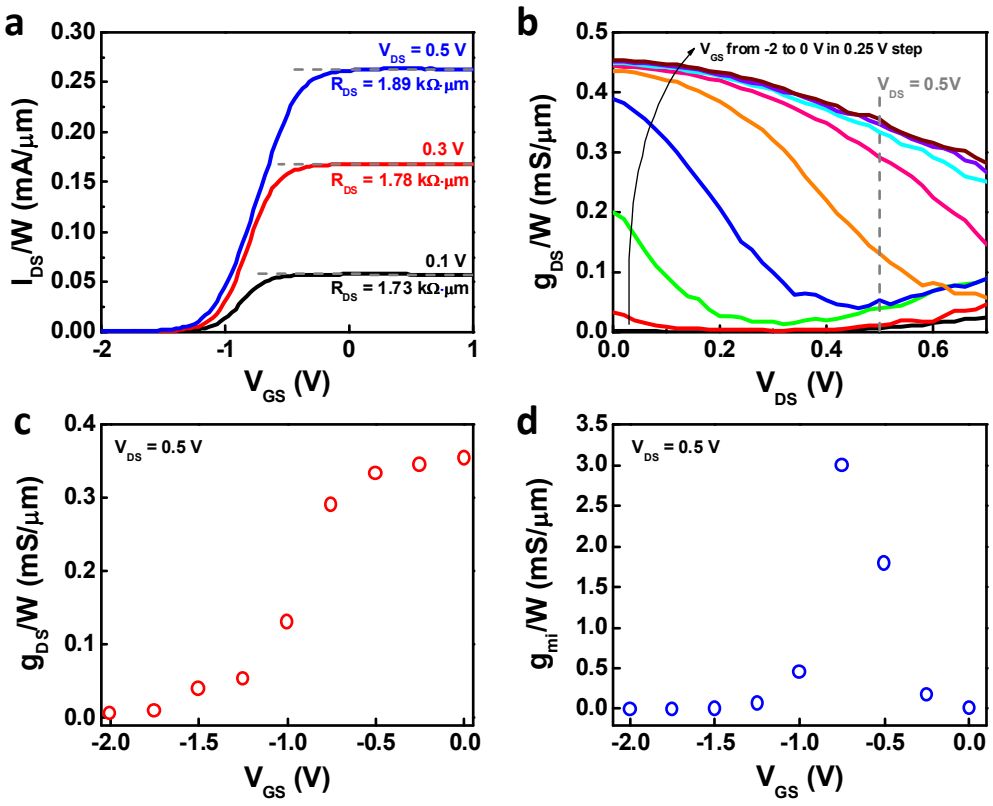

Figure S2. (a) I_{DS}–V_{GS} characteristics of a self-aligned InAs XOI MOSFET showing the near-saturation of the current at V_{GS} > -0.5V. (b) Output conductance g_{DS} as a functional of V_{DS}. (c) g_{DS} as a function of V_{GS} evaluated at V_{DS} = 0.5 V. (d) Intrinsic transconductance g_{mi} as a function of V_{GS} evaluated at V_{DS} = 0.5 V.

S3. Effect of contact anneal

We have studied the contact resistance of Ni-InAs junction as a function of InAs thickness using transmission line method (TLM)[2], with and without thermal annealing at 300 ºC for 1 min. The devices explored in this work have gate-first structure as opposed to S/D-first. As a result, Ni S/D contact annealing cannot be performed due to the gate stack degradation. In the future, gate/gate dielectric materials with higher thermal budget can be selected and the annealing process can be further optimized to reduce the contact resistance of the self-aligned T-gate transistors in order to further improve the experimental g_m.

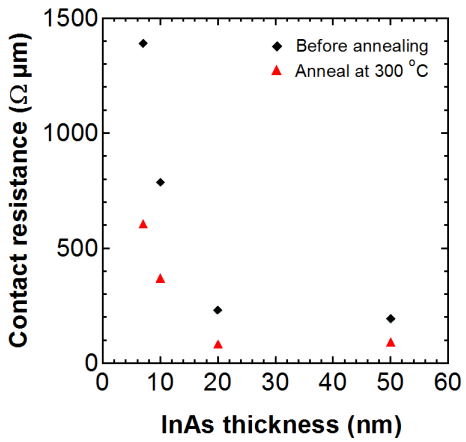

Figure S3. Contact resistance as a function of InAs thickness before and after annealing in N_2 environment at 300 ˚C.

S4. On-chip open/short de-embedding

We have performed an open/short de-embedding in order to remove the parasitic capacitances and inductances of the probing pads. The de-embedding is done by on-chip probing measurements, where the open/short structures are fabricated together with the device-under-test (DUT), and with exactly the same dimensions. The optical microscope images for the short and open structures are shown in Figure S4b and c, respectively. The as-measured S-parameters of the device, open, and short are converted to Y-parameters, and the intrinsic Y-parameters of the DUT are deduced using the following equation

$$Y_{DUT\_Intrinsic} = ((Y_{DUT} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1}$$

The intrinsic S-parameters are then in turn converted back from the intrinsic Y-parameters, which are used to deduce the de-embedded h_{21} and U of the transistor.

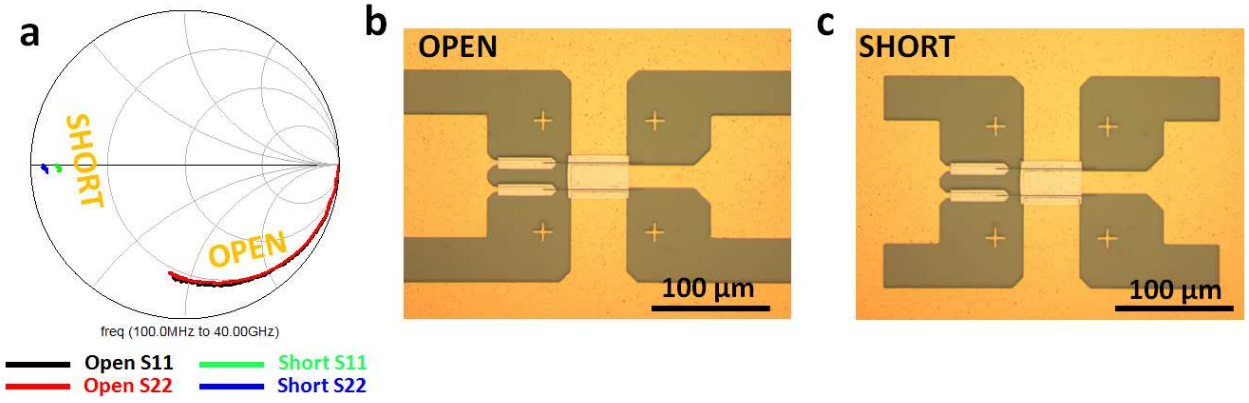

Figure S4. Open/short de-embedding. (a) As-measured S_{11} and S_{22} of the open and short structures. (b,c) Optical microscope images of the on-chip open (b) and short (c) structures used for the de-embedding.

S5. Small signal RF modeling to extract the device parameters from the measured *S*-parameters

In order to provide insight into the device performance over the measured frequency range, a π-model is established to create a small-signal equivalent circuit for the InAs XOI RF transistor as shown in Figure S5. To extract the component values in the model, the measured *S*-parameters are converted to *Y*-parameters first and the following equations are used to extract each component value:

$$y_{in} = y_{11}+y_{12}$$

$$y_{out} = y_{22}+y_{12}$$

$$g_m = -Re(y_{21})$$

$$C_{gd} = -Im(y_{12})/2\pi f$$

$$C_{in} = Im(y_{in})/2\pi f$$

$$R_{in} = 1/Re(y_{in})$$

$$C_{gs} = C_{in}/(1+1/Q_{in}^2)$$

$$R_g = R_{in}/(1+Q_{in}^2)$$

$$Q_{in} = Im(y_{in})/Re(y_{in})$$

$$C_{ds} = Im(y_{out})/2\pi f$$

$$R_{ds} = 1/Re(y_{out})$$

$$R_{NQS} = 1/5g_m$$

R_s and R_d are extracted from the DC I_{DS}–V_{GS} characteristics and R_{NQS} models the quasi-static behavior of the transistor due to distributed channel resistance. The extracted component values are summarized in Table 1 of the paper.

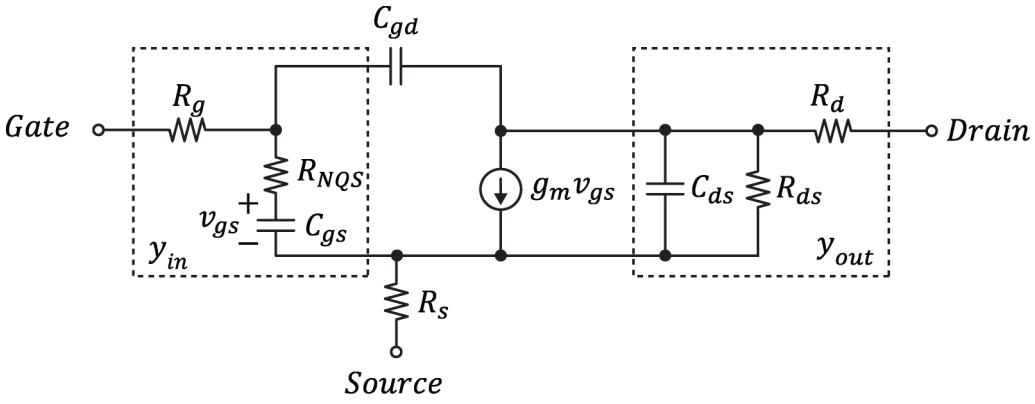

Figure S5. Small-signal equivalent circuit model for the InAs XOI RF transistor.

The RF measurement results show that f_{max} is lower than f_T considerably, which is primarily due to high loss from the gate resistance. The gate resistance to the first order can be estimated based on the dimension of the T-gate geometry and the conductivity of the material. In this specific design, the gate finger is 80 μm with a foot length, tip length, and gate height equal 75, 244, and 110 nm, respectively. If a bulk conductivity of 28.2 nΩ·m is used for aluminium, the calculated gate resistance is around 128.6 Ω, which is close to the extracted gate resistance from the *S*-parameter measurements as shown in Table 1. It is important to note that f_{max} can be significantly improved in the future if a multi-finger layout is employed.

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