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III–V Complementary Metal–Oxide–Semiconductor Electronics on Silicon Substrates

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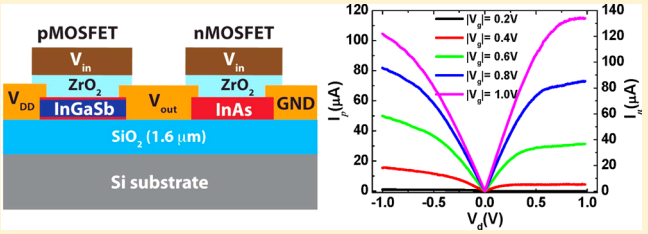
ABSTRACT: One of the major challenges in further advancement of III–V electronics is to integrate high mobility complementary transistors on the same substrate. The difficulty is due to the large lattice mismatch of the optimal *p*- and *n*-type III–V semiconductors. In this work, we employ a two-step epitaxial layer transfer process for the heterogeneous assembly of ultrathin membranes of III–V compound semiconductors on Si/SiO_2 substrates. In this III–V-on-insulator (XOI) concept, ultrathin-body InAs (thickness, 13 nm) and InGaSb (thickness, 7 nm) layers are used for enhancement-mode *n*- and *p*- MOSFETs, respectively. The peak effective mobilities of the complementary devices are ~1190 and ~370 $cm^2/(V\ s)$ for electrons and holes, respectively, both of which are higher than the state-of-the-art Si MOSFETs. We demonstrate the first proof-of-concept III–V CMOS logic operation by fabricating NOT and NAND gates, highlighting the utility of the XOI platform.



KEYWORDS: *III–V CMOS, InAs, InGaSb, two-dimensional semiconductors, logic gate*

Silicon-based metal–oxide–semiconductor field-effect transistors (MOSFET) have been the workhorse for the remarkable expansion of integrated circuits (ICs) industry since its first introduction.[1] This phenomenal growth has been mainly due to successful size scaling, which has brought significant performance improvement of electronic devices, resulting in enormous economic benefits.[2] The scaling trend has been continued up to date[3] and recently the 22 nm-node technology has been reported. With continued device scaling, however, dissipated power density has started to limit the performance of ICs.[4] Reducing the operating voltage of transistors is required for further device miniaturization.[5] In this regard, the use of high mobility channel materials, such as III–V semiconductors may provide a solution.

For the realization of high performance complementary MOS (CMOS) circuits, it is necessary to adopt high mobility *p*- and *n*-channel materials. Arsenic-based III–V compound semiconductors, such as InAs,[6−9] InGaAs,[10−13] and GaAs[14,15] exhibit excellent electron mobility as compared to silicon. On the other hand, relatively high hole mobilities have been reported using Sb-based semiconductors, including strained InSb,[16] InGaSb,[17,18] and epitaxially transferred InAs/InGaSb/InAs-on-insulator material systems.[19] Although high mobility *n*- and *p*-type III–V MOSFETs have been separately demonstrated, integrating them on the same substrate to realize CMOS circuits has not been achieved in part due to the large lattice mismatches of the explored materials. Of particular interest is to obtain III–V CMOS circuits on Si handing wafers due to the well-established process technology, and superb mechanical and thermal properties of Si. Here, we report the first heterogeneous integration of high mobility *p*- and *n*-type III–V compound semiconductors on Si using a two-step epitaxial layer transfer process. The approach results in nanoscale thickness membranes of III–V semiconductors with user-defined composition and dimensions on Si/SiO_2 substrates. In resemblance to the conventional Si-on-insulator (SOI) technology, the resulting III–V-on-insulator substrates are referred as XOI.[20] We demonstrate proof-of-concept CMOS logic gate operations, employing InAs XOI for *n*-MOSFETs and InAs/InGaSb/InAs hetero-XOI for *p*-MOSFETs.

The fabrication process schematic for XOI CMOS is depicted in Figure 1a. Here, a two-step layer transfer technique[21] was employed. First, InAs (thickness, 8 nm) and InAs/$In_{0.3}Ga_{0.7}Sb$/InAs stack layers (thickness, 2.5/7/2.5 nm) are grown separately on two different GaSb substrates with $Al_{0.2}Ga_{0.8}Sb$ (thickness, 60 nm) as the sacrificial layer by molecular beam epitaxy (MBE). The active layers are then pattern etched into nanoribbons (NRs) using previously reported process conditions.[9,19] The NRs are then released from the original source substrates by selective etching of AlGaSb in NH_4OH solution. The nearly freestanding NR active layers are then transferred onto Si/SiO_2

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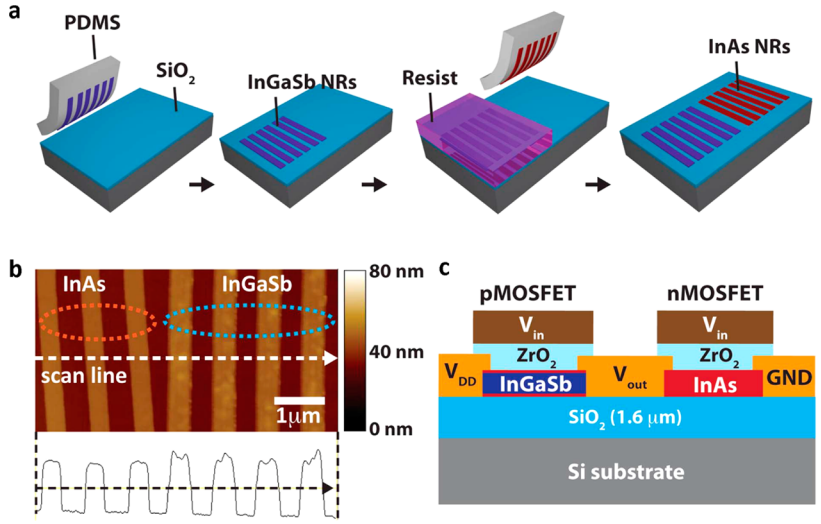

Figure 1. III–V XOI CMOS. (a) Process schematic for the heterogeneous integration of InAs and InAs/InGaSb/InSb XOI on a Si/SiO_2 substrate. (b) Atomic force micrograph of transferred InAs and InAs/InGaSb/InAs NRs, located adjacently. (c) Schematic representation of a top-gated CMOS inverter with InAs (n-type) and InGaSb (p-type) active layers, having 10 nm of ZrO_2 as the top-gate dielectric.

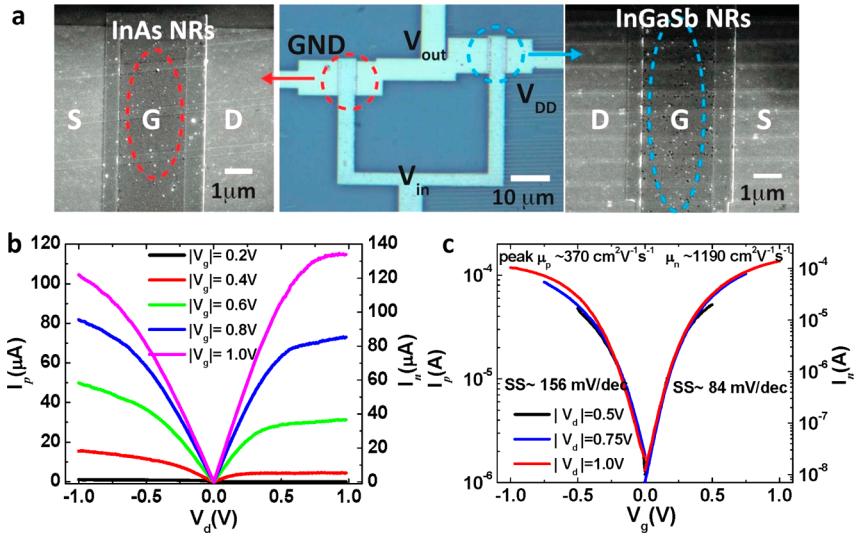

Figure 2. Performance of *p*- and *n*-type XOI MOSFETs. (a) Optical image (center) of a fabricated III–V CMOS inverter and the corresponding SEM images of each channel region (left: InAs; right: InAs/InGaSb/InAs). (b) Output and (c) transfer characteristics of *p*- (left axis) and *n*- (right axis) MOSFETs.

(1.6 μm thick, thermally grown) substrates with a PDMS slab. The InAs/InGaSb/InAs stack layer was transferred first, and covered by photoresist (PR) with proximate regions patterned by photolithography for the subsequent InAs NR transfer. Next, the PR is removed in acetone, leaving behind InAs and InAs/InGaSb/InAs NRs only at the predefined locations. Figure 1b shows the atomic force micrograph (AFM) of the transferred NR arrays scanned near the region where the two different channel materials are adjacently located. Figure 1c shows the device schematic of the top-gated XOI transistors, configured as a CMOS inventor. For device processing, the source/drain (S/D) electrodes were first defined by electron-beam (e-beam) lithography, followed by Ni evaporation (thickness, 30 nm) and lift-off. Atomic layer deposition of ZrO_2 gate dielectric (thickness, 10 nm), e-beam lithographic patterning of the gate electrodes, Ni gate deposition (thickness, 30 nm) and lift-off complete the device fabrication.

It should be noted that as indicated in our previous report, the role of InAs cladding layer on InGaSb body is 3-fold.[19] First, it protects the highly reactive InGaSb layer which can be severely oxidized in ambient air. Second, it provides dopant-free, low-resistance contacts by forming type-III band alignment at the InGaSb/InAs heterojunction underneath the metal contacts. Finally, it compresses the InGaSb channel biaxially and hence enhances the hole mobility. This heterostructure presents an important advance for realizing high performance III–V *p*-FETs on Si substrates.[19]

Figure 2a shows the optical and scanning electron microscope (SEMs) images of a CMOS inverter fabricated on a Si/SiO_2 substrate. Here, the circuit is composed of an InAs *n*-MOSFET and an InAs/InGaSb/InAs *p*-MOSFET. The *n*-MOSFET is composed of 3 NRs, with each NR having a width and channel length of ~340 nm and 2.85 μm, respectively. The p-MOSFET has 9 NRs with a NR width and channel length of ~200 nm and ~2.6 μm, respectively.

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Thus, the effective channel widths are ~1 μm and ~1.8 μm for the *n*- and *p*-MOSFETs, respectively. We note that different numbers of NRs (i.e., different channel widths) were chosen to achieve near symmetric pull-up and pull-down in the CMOS inverter, given the known difference in the mobility of InAs[22] and InGaSb XOI FETs.[19] Figures 2b and 2c show the I_d–V_d and I_d–V_g curves for both *n*- and *p*-MOSFETs. The output characteristics in Figure 2b clearly show closely matched current levels between the two transistors. Next, using the I_d–V_g data in Figure 2c, the effective carrier mobility of both devices were extracted based on the relation, $\mu_{eff} = L_g[WR_{ch}C_{ox}(V_g - V_{TH} - 0.5V_d)]^{-1}$, where L_g is the channel length, W is the total channel width, R_{ch} is the channel resistance, C_{ox} is the gate-to-channel capacitance, V_{TH} is the threshold voltage, and drain voltage, $|V_d|$ is biased at 50 mV. The V_{TH} values at $|V_d|$ = 50 mV are −0.09 V and 0.25 V for *p*- and *n*-MOSFETs, respectively as obtained by linear extrapolation of $I_d - V_g$ data. Approximately, 3-fold higher peak mobility, $\mu_{eff,n}$ ~1190 cm^2/V·s, was obtained in the InAs (thickness, 8 nm) *n*-MOSFET as compared to InAs(2.5 nm)/InGaSb(7 nm)/InAs(2.5 nm) *p*-MOSFET with peak hole mobility of $\mu_{eff,p}$ ~370 cm^2/V·s. Although hole mobility up to ~800 cm^2/V·s can be achieved in the thicker body InGaSb (15 nm) XOI FETs,[19] here, we employed thinner body InGaSb layers to obtain enhancement-mode FETs with $V_{TH} < 0$. The subthreshold swing (SS) values at $|V_{ds}|$ = 0.5 V, defined as SS = $-[d(\log I_d)/dV_g]^{-1}$, are ~156 mV/dec and ~84 mV/dec for *p*- and *n*-MOSFETs, respectively. The modest SS value for the *p*-MOSFET is attributed to higher density of interface states (at InAs/InGaSb and InAs/ZrO_2) in addition to reduced gate coupling to the InGaSb body due to InAs capping layer.[19] The I_{ON}/I_{OFF} ratio for *p*- (*n*-) MOSFET is ~10^2 (10^3) when the devices are biased between V_g = 0 and ±0.5 V, which is increased to ~10^4 (10^5) when they are biased between V_g = −0.5 and +0.5 V, measured at $|V_d|$ = 0.5 V. We note that the gate leakage currents were below 10 pA for all the devices.

Next, CMOS inverter performance was investigated using the fabricated device shown in Figure 2a. Figure 3a shows the

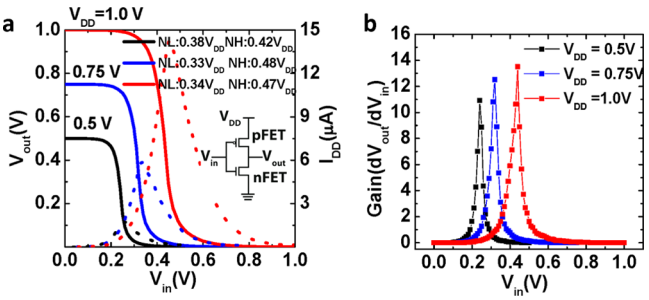

Figure 3. III–V CMOS inverter. (a) Transfer characteristics of a CMOS inverter, measured at different supply voltages (V_{DD}). Inset shows the circuit diagram for the fabricated inverter. (b) Inverter gain (dV_{out}/dV_{in}) dependence on the input voltage.

inverter voltage transfer characteristics and switching current I_{DD} for different supply voltage, V_{DD} = 0.5, 0.75 and 1.0 V. The inset in Figure 3a demonstrates the circuit diagram for the CMOS inverter, which is composed of one *p*- and one *n*-MOSFET, connected in series. At low input voltage (V_{in}) (logic "0"), the output voltage (V_{out}) is pulled-up to V_{DD} (logic "1"). The noise margins of NH = 0.38 V_{DD} and NL = 0.42V_{DD} were obtained at V_{DD} = 0.5 V, where NH and NL are the high- and low-state noise margin, respectively. Figure 3b shows the gain characteristics ($\Delta V_{out}/\Delta V_{in}$) of the CMOS inverter. A gain of >11 is obtained at V_{DD} = 0.5 V, which gradually improves with V_{DD}.

To further demonstrate the logic operation of III–V complementary MOSFETs, we fabricated a NAND logic gate. The NAND-gate logic was realized by connecting two InAs *n*-MOSFETs in series and two InAs/InGaSb/InAs *p*-MOSFETs in parallel (Figure 4a). During the measurement, a constant

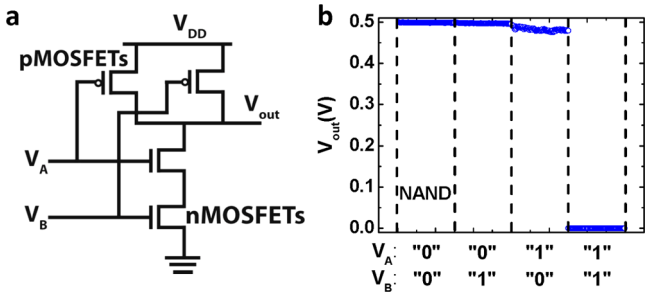

Figure 4. III–V CMOS NAND logic gate. (a) Circuit schematic of a CMOS NAND gate. The circuit is designed by connecting two p-MOSFETs in parallel and two n-MOSFETs in series. (b) Output voltage V_{out} for four different combinations of input states "0 0", "0 1", "1 0", and "1 1". The output is in the "low-state" only if the inputs are "1 1". Note: Input voltages of +0.5 and −0.5 V are treated as logic "1" and "0", respectively. The supply voltage (V_{DD}) for the circuit is 0.5 V.

V_{DD}= 0.5 V was applied with two input voltages of V_A and V_B = ± 0.5 V. Here, the logic "0" ("1") input corresponds to −0.5 V (+0.5 V). The result from the NAND gate operation is shown in Figure 4b. Namely, when either one or both of the *p*-MOSFETs are in the "low" state, the V_{out} is $V_{DD} \approx$ 0.5 V, corresponding to logic "1". Only when both of *n*-MOSFETs are in the logic "1", the output becomes logic "0" ($V_{out} \approx$ GND). This representative result highlights that more complicated logic circuits can be realized using the similar approaches.

While in this work, both *n*- and *p*- channel materials were assembled on the same device layer, in the future, three-dimensional assembly of III–V XOI materials need to be explored in order to present a more practical pathway for achieving a high density of device fabrication and processing on the same chip.[23−25] In this proposed approach, an insulator layer is deposited after each III–V layer transfer.

In conclusion, we have successfully demonstrated the first III–V CMOS circuits on Si handling wafers using a two-step epitaxial layer transfer technique. The *n*- and *p*- channel materials were specifically chosen to deliver the highest carrier mobilities. As a proof-of-concept, CMOS NOT and NAND logic gates are demonstrated. The work here demonstrates an important advance in the field of III–V electronics, and shows the versatility of the layer transfer technique for obtaining heterogeneous III–V electronics on conventional Si substrates.

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Notes

The authors declare no competing financial interest.

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