

Monolithic Integration of Carbon Nanotube Devices with Silicon MOS Technology

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Received November 1, 2003; Revised Manuscript Received November 18, 2003

ABSTRACT

An integrated circuit combining single-walled carbon nanotube (SWNT) devices with n-channel metal oxide semiconductor (NMOS) field effect transistors was fabricated. SWNTs were grown, using chemical vapor deposition, from catalyst islands located on an NMOS decoder circuit. Massive arrays of nanotube devices, each addressed individually using the NMOS circuit, were rapidly characterized. The successful monolithic integration of nanotube devices and MOS transistors creates many possibilities, including electronically addressable nanotube chemical sensor arrays.

Carbon nanotubes (CNTs) have attracted much attention for their unique properties in recent years. CNTs are found to have very large Young's modulus¹ and structurally dependent electronic properties.² Depending on their chirality, CNTs can be either semiconducting or metallic. Numerous demonstrations of field-effect transistors (FETs) based on semiconducting CNTs have been reported.^{3–6} Metallic CNTs, on the other hand, are capable of supporting a very large current density,⁷ on the order of 1×10^9 A/cm². Furthermore, inverter circuits made entirely of complementary CNT-FETs have been reported and show a gain larger than unity.^{8,9} These results indicate that CNT is a promising electronic material.

Owing to the maturity of silicon technology, as well as the unique chemical and mechanical properties of CNTs, we can anticipate the emergence of a hybrid technology that makes use of the advantages of both materials. One example would be a CNT-based memory with a read-out circuitry based on silicon MOSFETs.¹⁰

Chemical vapor deposition (CVD) initiated from pre-patterned catalyst islands has been shown to produce CNTs that contain very few defects,¹¹ and whose location is well controlled.¹² By changing the growth environment and the catalyst size and chemistry, one can selectively grow single-walled nanotubes (SWNTs) and control their diameter.¹³

Given that semiconducting CNTs have shown promise as an electronic material, it is desirable to optimize the CNT

growth process for this application. The optimization usually requires making electrical measurements on many devices. This is a tedious task, since data collection from a large number of devices is required to establish significant statistics. To accelerate the optimization process, we wish to have a tool that can rapidly determine the electrical characteristics of a large number of CNTs.

To accomplish the task of rapid measurement, and to demonstrate, for the first time, a process that integrates CNTs with silicon MOS technology, we designed and fabricated a random access nanotube test chip (henceforth referred to as the RANT chip) that integrates nanotubes grown using chemical vapor deposition with an n-channel metal oxide semiconductor (NMOS) circuitry fabricated in a standard silicon integrated circuit process. The RANT chip is a simple switching network consisting of NMOS transistors, through which approximately two thousand three-terminal CNT devices, obtained through growth from equally many catalyst sites, can be electrically accessed on an individual basis by using only 22 binary inputs. Ideally, one nanotube is grown at each site, and two thousand nanotube devices can be characterized, yielding a large sample size that enables statistical analysis of a growth process.

To individually access every one of the two thousand growth sites using only 22 inputs, we employ an addressing circuit consisting of an 11-level binary tree of NMOS transistors.¹⁴ Figure 1a shows the circuit schematic. To select a site numbered by S , we proceed as follows. S is written in an 11-bit binary number, and the value of the n th bit

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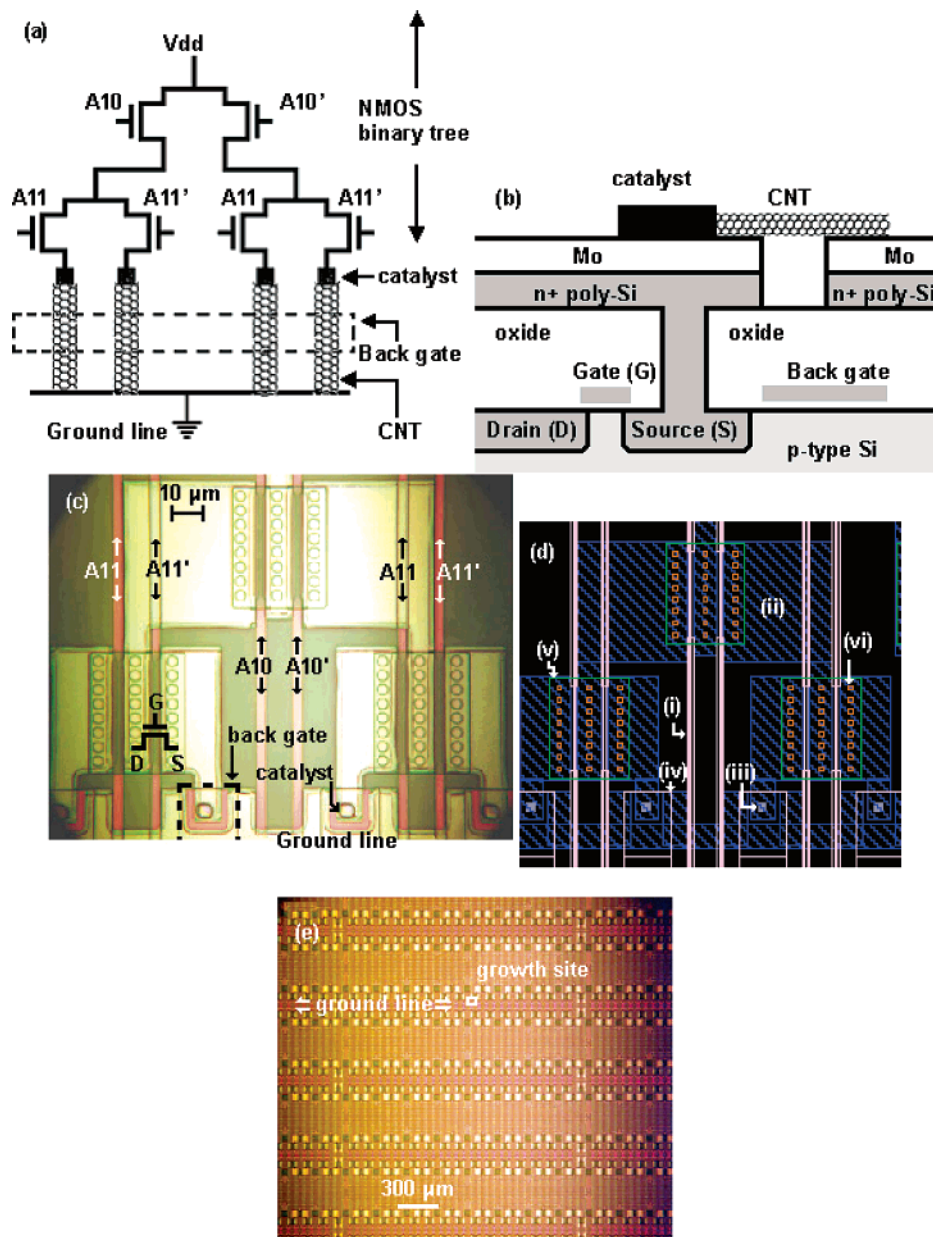


Figure 1. (a) Circuit schematic of the nanotube decoder. Nanotubes are grown on catalyst islands located at the bottom level of an 11-level binary tree of NMOS transistors (only two levels are drawn for clarity). To address the CNT at the extreme left, A10 and A11 are set to 5 V to turn on the NMOS transistors in series with the CNT, while A10' and A11' are set to 0 V to turn off the other paths. The back gate is used to modulate the conductance of the CNTs. (b) Schematic of the cross-section of the decoder chip near the catalyst island. (c) Optical micrograph of part of the circuit, which corresponds closely to the schematic in (a). The catalyst island is located on the source (S) of an NMOS transistor (identified by the overlaid device symbol). CNTs grown from the catalyst island cross the U-shaped gap to make contact to the ground line, seen at the bottom of the figure. Shown by the dashed line is the perimeter of the back gate lying under the catalyst island and the U-shaped gap. (d) layout of the circuit: (i) polysilicon gate of NMOS transistors; (ii) hatched area, Mo/Poly-Si stack; (iii) catalyst; (iv) polysilicon back gate; (v) NMOS active area; (vi) metal to source/drain contact. (e) Expanded view of the circuit. The white box encloses one growth site. About 500 sites are shown in the figure.

determines which NMOS transistors in the n th level should be turned on. A n th bit values of “1” or “0” turn on the NMOS transistors branching to the left or right, respectively. Thus, only two inputs are necessary for each level, one controlling the transistors branching to the left and one for those to the right, and these two inputs are logical complements of each other. The 11-level binary tree addresses therefore a total of 2^{11} or 2048 growth sites. For an NMOS binary tree of arbitrary number of levels, the number of accessible sites depends exponentially on the number of

inputs:

$$\text{No. accessible sites} = 2^{(\text{no. inputs}/2)} \quad (1)$$

The conductance of a CNT can be modulated by a polysilicon back gate buried under a 500 nm-thick oxide layer. Thus a semiconducting CNT can be distinguished from a metallic one by measuring its conductance as a function of the back gate bias. To simplify the fabrication process, only n-channel MOS transistors are employed, instead of complementary

MOS (CMOS) transistors. A CMOS circuit would have required only 11 rather than 22 inputs. Consider the circuit in Figure 1a: the transistors controlled by A10' and A11' can be replaced by p-channel MOS transistors (PMOS) and their gates tied to A10 and A11. A logical 1 (+5 V) applied at A10 will simultaneously turn on the NMOS branching to the left, but turn off the PMOS branching to the right. As a result, only one input is required for each level in the binary tree.

The current flowing through a CNT device must go through a chain of 11 NMOS transistors connected in series. When a supply voltage V_{dd} equal to the NMOS gate voltage is applied, it drops by about one transistor threshold voltage after the first transistor in the chain. Since the current through the chain is very small compared to the saturation current of the transistor ($\sim 100 \mu\text{A}$), subsequent NMOS transistors operate in the triode region and the voltage drop across them is small. Using the transistor parameters of our process (electron mobility: $1000 \text{ cm}^2/\text{Vs}$, gate oxide thickness: 10 nm), we estimate a drop of 0.512 V across the first transistor and 5 mV across the second, when the following bias conditions are assumed: current $I = 1 \mu\text{A}$, $V_{dd} = 5 \text{ V}$, gate voltage = 5 V. The voltage drop of the entire chain is approximately 1V, and most of the supply voltage is delivered to the CNT device.

Measurements on the RANT chip are performed using an automated measurement system consisting of the Hewlett-Packard 4062B semiconductor parametric test system and the Electroglas 2001X automatic wafer probing system.

The RANT chip is fabricated using a two-part process. In the first, the NMOS circuit is made using UC Berkeley Microlab's $1 \mu\text{m}$ baseline process.¹⁵ Every transistor is $40 \mu\text{m}$ wide with a $1 \mu\text{m}$ gate length, and a threshold voltage of 0.5 V. The NMOS transistors are then interconnected using a stack of phosphorus-doped n+ polysilicon (thickness: 3000 \AA) and molybdenum (thickness: 1000 \AA). In the second part of the process, CNTs are grown on the NMOS circuit via chemical vapor deposition. Catalysts prepared as in ref 16 are deposited at desired locations on the circuit using lift-off.¹⁷ CNTs are then grown in a 1 in. CVD furnace at $875 \text{ }^\circ\text{C}$ for 4 min under the flow of 1000 standard cubic centimeter per minute (sccm) of CH_4 , 500 sccm of H_2 , and 10 sccm of C_2H_4 .⁹ SWNTs grown under this condition have diameters of 2 to 4 nm. The cross-section of the final structure is depicted in Figure 1b. Magnified and expanded views of the completed circuit and the catalyst islands are shown in Figure 1c and Figure 1e, respectively. Measurement of control samples shows that the circuit remains fully functional after the lift-off and the thermal cycle (without the growth of nanotubes). The successful growth of nanotubes on the NMOS circuit is shown in Figure 2. CNTs bridge the gap separating a NMOS transistor from the ground line, completing the electrical path from V_{dd} to the ground line.

The successful interconnection of CNT transistors to the NMOS circuit is confirmed via electrical measurement. Figure 3 shows the effect of back gate bias V_g on the conductance of a CNT device addressed by the NMOS circuitry. The observed ambipolar behavior is a characteristic

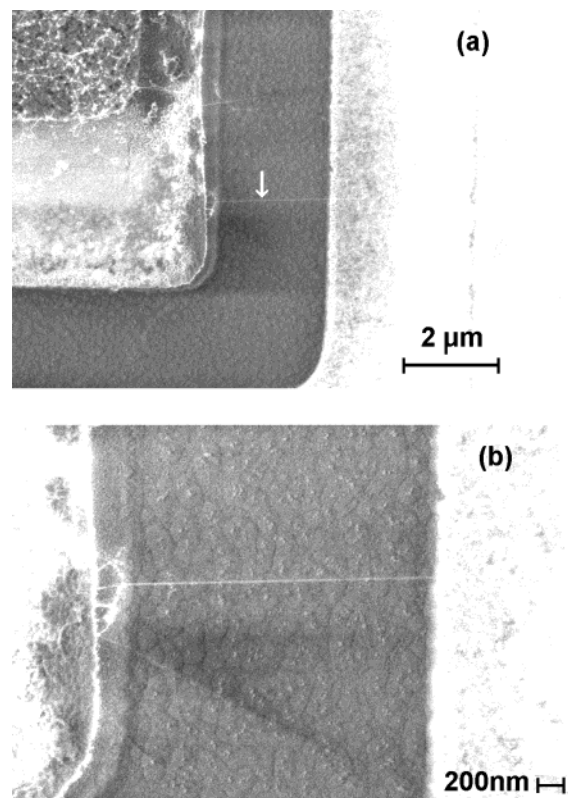


Figure 2. (a) Scanning electron microscope image of a CNT (indicated by white arrow) bridging the gap, completing the decoder circuit. The catalyst island is located at the left side of the gap and the ground line at the right side. (b) Magnified view of the CNT in (a).

of a close to mid-gap Schottky barrier FET.¹⁸ Due to the lack of Fermi level pinning in CNT-FETs, the work function of the metal contacts is found to play an essential role in determining the contact properties, and hence the transport characteristics of the devices. As a result, a spectrum of devices ranging from ohmically contacted p-FETs to n-FETs has been demonstrated for various nanotube diameters by integrating high or low work function S/D metal contacts, respectively. We note that while previously fabricated devices with Mo contacts on SiO_2 ($\sim 500 \text{ nm}$)/Si substrates have shown p-FET characteristics, the devices demonstrated in this letter are quite ambipolar. The results suggest that the work function of the contacts in this study may be lower than the previously studied devices. This may be attributed to the formation of Mo silicide or the diffusion of P atoms from the underlying poly-Si film into the Mo electrodes, resulting in a different contact composition. In future work, alternative metal contacts (such as Pd)⁵ can be integrated into the circuit in order to obtain higher performance CNT-FETs.

Electrical measurements reveal that there are CNT devices with weak gate dependence, in addition to the semiconducting devices. The back gate dependence of such a device is shown in Figure 3b. It is possible that both metallic and semiconducting CNTs are present at this particular site (number 7) and that conduction is dominated by the metallic CNT(s) at low gate biases, while the semiconducting CNT(s) contribute only at large negative gate biases.

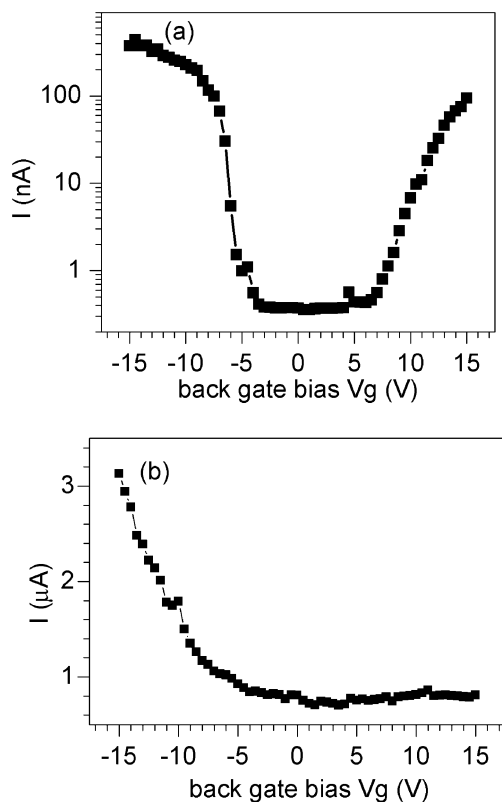


Figure 3. (a) Ambipolar $I-V_g$ characteristic as measured using the decoder chip, at growth site 125. Biasing conditions: $V_{dd} = 5$ V, NMOS gate = 5 V. (b) CNT device exhibiting weak dependence on back gate bias (site 7), as measured using the decoder chip. Biasing conditions: $V_{dd} = 5$ V, NMOS gate = 5 V.

A statistical plot of the ratio of the “on” current I_{on} (at back gate = -15 V) to the “off” current I_{off} (back gate = 0 V) is shown in Figure 4. Only about 1% of the sites show significant back gate dependence, but about 10% show an I_{on}/I_{off} ratio larger than two. It is possible that many CNTs do not cross the gap to make contact to the ground line, as idealized in Figure 1a and 1b. These open sites have an I_{on}/I_{off} ratio on the order of unity, as only instrumental noise (~ 100 pA) is measured and the on and off currents are equally small. In the present proof-of-concept work, the MOS fabrication and CVD nanotube growth steps were not optimized. Higher percentage of devices with FET characteristics may be obtained by optimization of the growth parameters. The next generation of CNT-MOS integrated circuits will be much more advanced based on the experience acquired here.

A tool for rapidly characterizing thousands of carbon nanotube devices has been fabricated. Implemented in the NMOS technology, it is the first instance of monolithic integration of CNT with MOS technology. In addition to providing a tool for accelerating the optimization of CNT growth, this work demonstrates a process that allows the massive integration of CNT devices within a MOS circuit. Applications that require the advantages from each technology may now be realized. An immediate application is the development of massive nanotube chemical sensor arrays¹⁹ in which each sensor can be addressed electrically through a MOS circuit. The process developed in this work can be

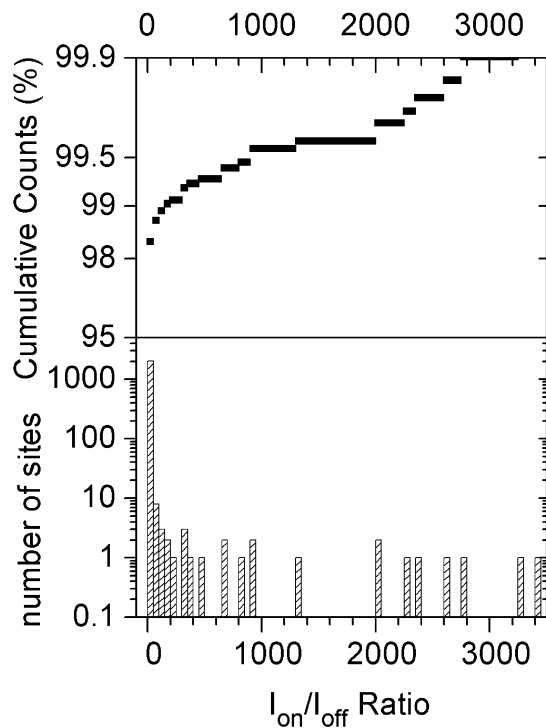


Figure 4. Statistics of electrical measurements on 2048 growth sites. About 1% of the sites show large ($I_{on}/I_{off} > 100$) dependence on back gate bias. I_{on} and I_{off} are the currents at back gate biases of -15 V and 0 V, respectively. Bin size for histogram: 50.

readily adapted to the integration of other nanoelectronic devices with MOS technology, providing a similar tool for optimization as well as opening up the possibility of other novel applications.

Acknowledgment. The authors thank Dr. Yang-Kyu Choi and the UC Berkeley Microlab staff for help on the process development and measurement scheme. This work is funded by MARCO MSD Focus center and DARPA/MTO. A. J. acknowledges an SRC Peter Verhofstadt Graduate Fellowship.

References

- (1) Treacy, M. M. J.; Ebbesen, T. W.; Gibson, J. M. *Nature* **1996**, *381*, 678.
- (2) *Carbon nanotubes: synthesis, structure, properties, and applications*; Dresselhaus, M. S., Dresselhaus, G., Avouris, Ph., Eds.; Springer: Berlin, 2001.
- (3) Dai, H.; Kong, J.; Zhou, C.; Franklin, N.; Tomblor, T.; Cassell, A.; Fan, S.; Chapline, M. *J. Phys. Chem. B* **1999**, *103*, 11246.
- (4) Avouris, Ph. *Chem. Phys.* **2002**, *281*, 429.
- (5) Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. *Nature* **2003**, *424*, 654.
- (6) Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. *Nature Mater.* **2002**, *1*, 241.
- (7) McEuen P.; Fuhrer, M. S.; Park H. *IEEE Trans. Nanotechnol.* **2002**, *1*, 78.
- (8) Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, Ph. *Nano Lett.* **2001**, *1*, 453.
- (9) Javey, A.; Wang, Q.; Ural, A.; Li, Y.; Dai, H. *Nano Lett.* **2002**, *2*, 929.
- (10) Luyken, R. J.; Hofmann, F. *Nanotechnology* **2003**, *14*, 273.
- (11) Kong, J.; Yenilmez, E.; Tomblor, T. W.; Kim, W.; Dai, H.; Laughlin, R. B.; Liu, L.; Jayanthi, C. S.; Wu, S. Y. *Phys. Rev. Lett.* **2001**, *87*, 106801-1.
- (12) Kong, J.; Soh, H. T.; Cassell, A. M.; Quate, C. F.; Dai, H. *Nature* **1998**, *395*, 878.

- (13) Kong, J.; Cassell, A. M.; Dai, H. *Chem. Phys. Lett.* **1998**, 292, 567.
- (14) Baker, R. J.; Li, H. W.; Boyce, D. E. *CMOS Circuit Design, Layout, and Simulation*; IEEE Press: New York, 1998.
- (15) *CMOS Baseline Process in the UC Berkeley Microfabrication Laboratory*, URL <http://www-microlab.eecs.berkeley.edu/baseline/index.html>.
- (16) Cassell, A. M.; Raymakers, J. A.; Kong, J.; Dai, H. *J. Phys. Chem. B* **1999**, 103, 6484.
- (17) Franklin, N. R.; Wang, Q.; Tomblor, T. W.; Javey, A.; Shim, M.; Dai, H. *Appl. Phys. Lett.* **2002**, 81, 913.
- (18) Martel, R.; Derycke, V.; Lavoie, C.; Appenzeller, J.; Chan, K. K.; Tersoff, J.; Avouris, Ph. *Phys. Rev. Lett.* **2001**, 87, 256805-1.
- (19) Qi, P.; Vermesh, O.; Grecu, M.; Javey, A.; Wang, Q.; Dai, H.; Peng, S.; Cho, K. J. *Nano Lett.* **2003**, 3, 347.

NL0349707