NANO LETTERS

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Vol. 0, No. 0
A−F

Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors

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Received November 29, 2002

ABSTRACT

Carbon nanotube field-effect transistors commonly comprise nanotubes lying on SiO_2 surfaces exposed to the ambient environment. It is shown here that the transistors exhibit hysteresis in their electrical characteristics because of charge trapping by water molecules around the nanotubes, including SiO_2 surface-bound water proximal to the nanotubes. Hysteresis persists for the transistors in vacuum since the SiO_2-bound water does not completely desorb in vacuum at room temperature, a known phenomenon in SiO_2 surface chemistry. Heating under dry conditions significantly removes water and reduces hysteresis in the transistors. Nearly hysteresis-free transistors are obtainable by passivating the devices with polymers that hydrogen bond with silanol groups on SiO_2 (e.g., with poly(methyl methacrylate) (PMMA)). However, nanotube humidity sensors could be explored with suitable water-sensitive coatings. The results may have implications to field-effect transistors made from other chemically derived materials.

The interaction between single-walled carbon nanotubes (SWNTs) and molecular species in the environment can significantly affect the electrical properties of nanotube devices.[1] This effect can be exploited for nanoscale chemical sensors,[2,3] but is not desired for nanotube-based field-effect transistors (FETs)[4−13] potentially applied to future electronics. Passivation of these transistors should be developed to impart stable electrical characteristics against environmental changes.

Hysteresis due to various charge traps in a FET must be eliminated for most applications or must be controlled for specific memory devices. Recently, several groups reported SWNT FETs fabricated on SiO_2/Si substrates (device structure similar to that in Figure 1a) exhibiting hysteresis in current versus gate-voltage (Si as back-gate) characteristics and attributed the hysteresis to charge traps in bulk SiO_2, oxygen-related defect trap sites near nanotubes, or traps at the SiO_2/Si interface.[11,12,14] No dependence of the hysteresis on chemical environments was observed (e.g., in ambient air versus in vacuum). Here, we show that the foremost significant cause of hysteresis in passivation-free nanotube FETs is the water molecule, especially SiO_2 surface-bound water that cannot be fully removed by pumping in vacuum. We also report that a simple polymer coating can be used as passivation to afford nearly hysteresis-free nanotube transistors.

The nanotube FETs used in this work were obtained by the chemical vapor deposition (CVD) synthesis[15] of individual semiconducting SWNTs to bridge preformed molybdenum source (S) and drain (D) electrodes (Figure 1b)[16] or

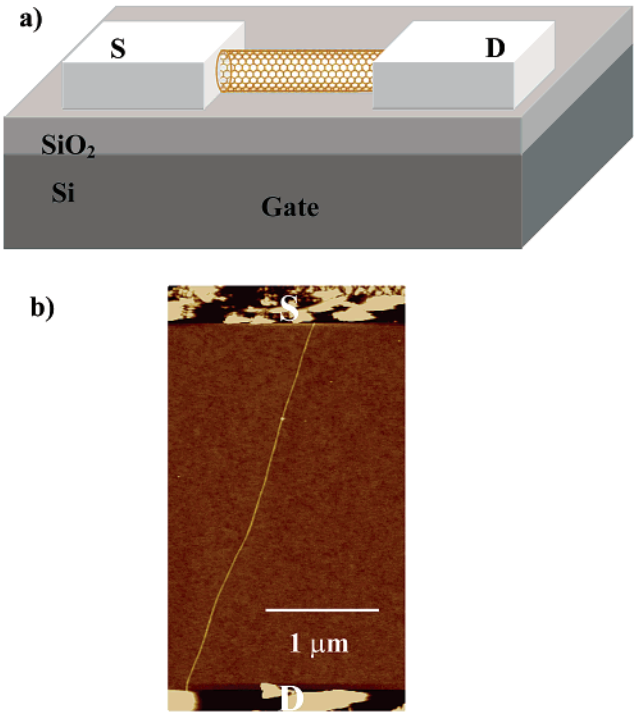

Figure 1. (a) Schematic structure of a back-gated SWNT FET. (b) Atomic force microscopy image of a device with a single nanotube (lying on SiO_2) bridging source (S) and drain (D) electrodes.

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10.1021/nl0259232 CCC: $25.00
Published on Web 00/00/0000

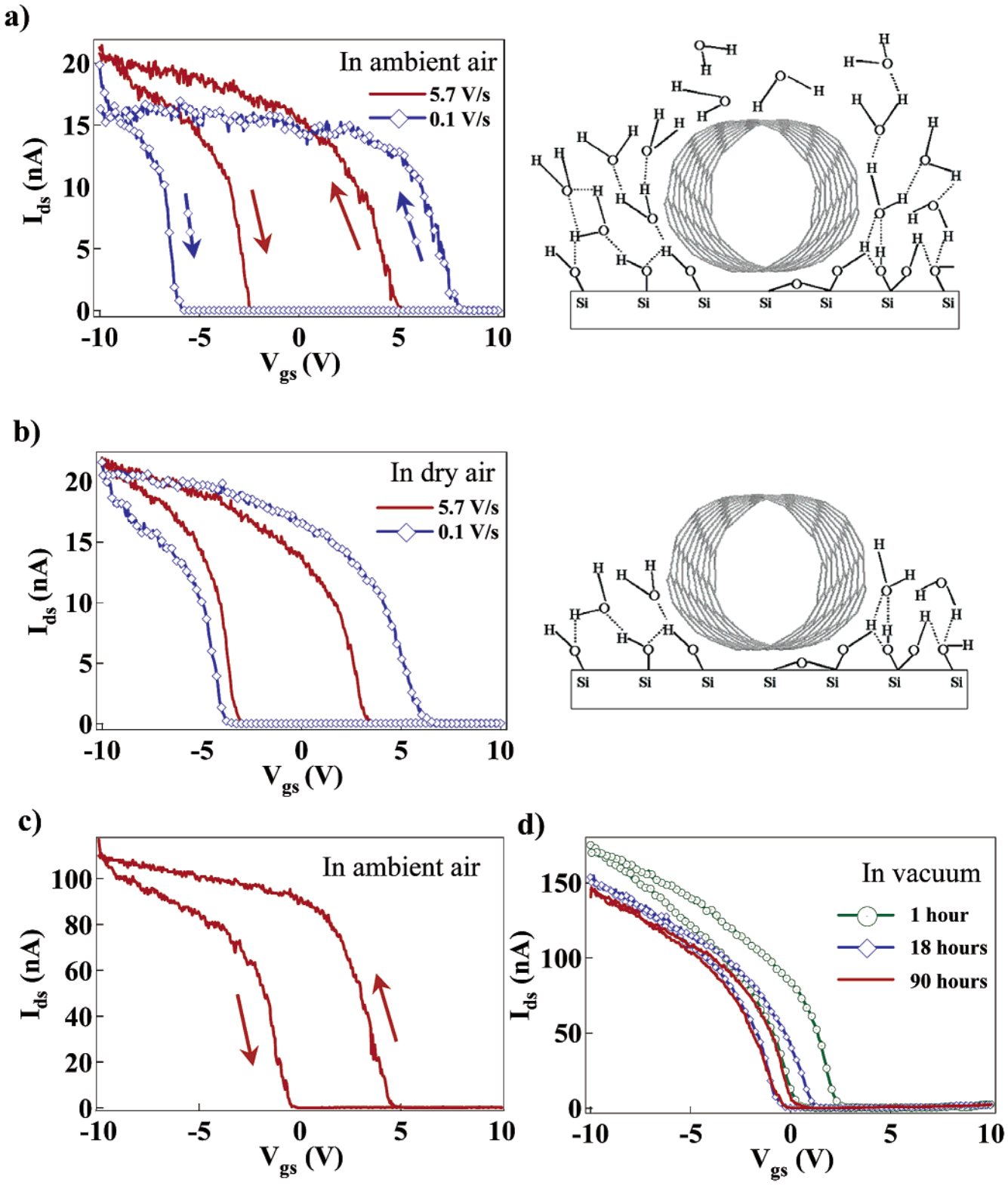

Figure 2. (a) $I_{ds}-V_{gs}$ curves recorded for a SWNT FET under two V_{gs} sweep rates (as indicated) in ambient air. Bias voltage $V_{ds} = 10$ mV. The schematic drawing at the right depicts water molecules hydrogen bonding to the surface Si−OH groups and physisorbed on a nanotube. (b) Data recorded for the same device as in (a) after placing the device in dry air for 0.5 h. The schematic drawing at the right shows surface Si−OH-bound water molecules. (c) $I_{ds}-V_{gs}$ data for a second SWNT FET in ambient air. Gate-sweep rate = 5.7 V/s. Bias voltage $V_{ds} = 10$ mV. (d) Data recorded after the same device as in (c) was pumped in vacuum for various periods of time.

by placing Ti/Au S−D electrodes on top of SWNTs after growth.[17] The substrates consisted of 500-nm-thick thermally grown SiO_2 on p-type doped Si wafers (used for back-gate, Figure 1a). The 500-nm oxide was grown by a wet oxidation process for Si wafers at 1000 °C ($H_2/O_2 = 150/1000$ in the oxidation chamber).

As shown in Figure 2a, for SWNT FETs exposed to the ambient environment, hysteresis was observed in the current

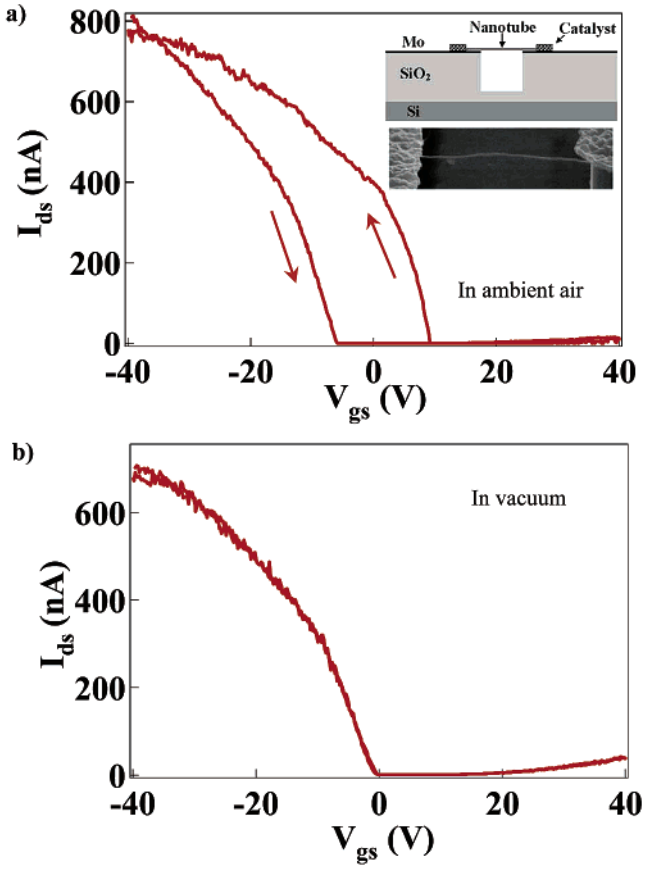

Figure 3. (a) $I_{ds}-V_{gs}$ curves recorded for a suspended SWNT FET exposed to ambient air. Bias voltage $V_{ds} = 10$ mV. V_{gs} sweep rate $= 0.1$ V/s. The inset shows a scanning electron microscopy image and a schematic structure of the device. (b) Diminished hysteresis recorded with the same device immediately after placing it in vacuum.

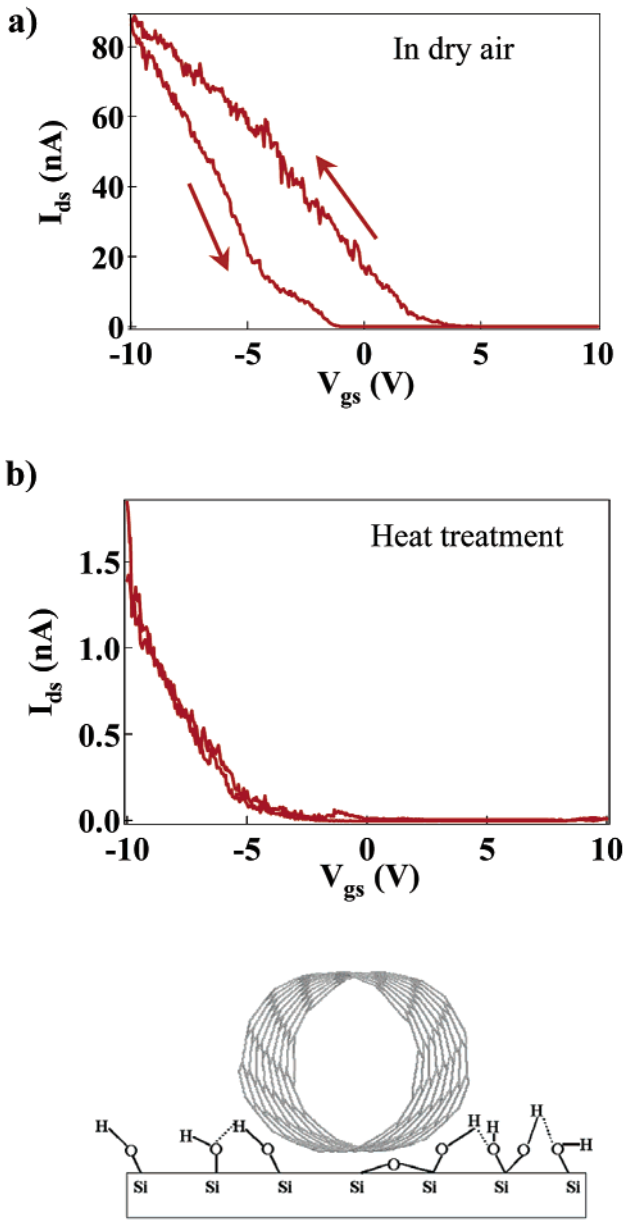

Figure 4. (a) $I_{ds}-V_{gs}$ data for an SWNT FET (on SiO_2) in dry air. $V_{ds} = 10$ mV. (b) Significantly reduced hysteresis recorded for the device after heating to 200 °C in H_2 for 4.5 h, cooled to room temperature, and exposed to dry air for 5 h. The schematic drawing depicts the removal of surface-bound water after the thermal treatment.

(I_{ds}) versus gate voltage (V_{gs}) characteristics (recorded under constant S/D bias V_{ds}) when V_{gs} was swept from -10 V to $+10$ V and back to -10 V. That is, when sweeping V_{gs} back from $+10$ V to -10 V, we observed a shift in the recorded $I_{ds}-V_{gs}$ toward the positive V_{gs} side. The width of the hysteresis in V_{gs} exhibited a significant dependence on the sweeping rate of the gate voltage, dV_{gs}/dt. The difference in the threshold voltage values due to hysteresis increased from 7.5 V for $dV_{gs}/dt = 5.7$ V/s to 14 V for $dV_{gs}/dt = 0.1$ V/s (Figure 2a). A significant dependence of the hysteresis on the V_{gs} scan range was also observed, with larger-range V_{gs} scans producing larger hysteresis (data not shown). These results suggest that the hysteresis is caused by slow charge traps that discharge on a time scale longer than several seconds.

Through a series of control experiments, we find that the hysteresis of SWNT FETs does depend on chemical environments. However, the dependence can be missed since it can take a relatively long time for appreciable effects to take place. Upon changing the environment for the nanotube FET in Figure 2a from ambient to dry air, we observed noticeable decreases in hysteresis (Figure 2b versus Figure 2a). In vacuum (10^{-7} Torr), hysteresis in nanotube FETs slowly decreased over time but did not completely vanish. This can be seen in the data recorded in air and vacuum (Figure 2c and Figure 2d, repectively) for a device. Hysteresis persisted even after the device was pumped in vacuum for ~4 days (Figure 2d). In another control experiment, we investigated SWNT FETs comprising fully suspended SWNTs over the back gate by ~2 μm.[16] Under ambient conditions, hysteresis was observed in $I_{ds}-V_{gs}$ for a V_{gs} sweep range of [-40 V, 40 V] (Figure 3a. Note: the gate has a low efficiency due to the 2-μm air gap). For this type of device, the hysteresis quickly reduced to near zero after it was placed in vacuum (Figure 3b).

The results above have been reproduced with multiple devices (>3 for each data set in the Figures) and suggest that charge trapping by water is an important cause of the

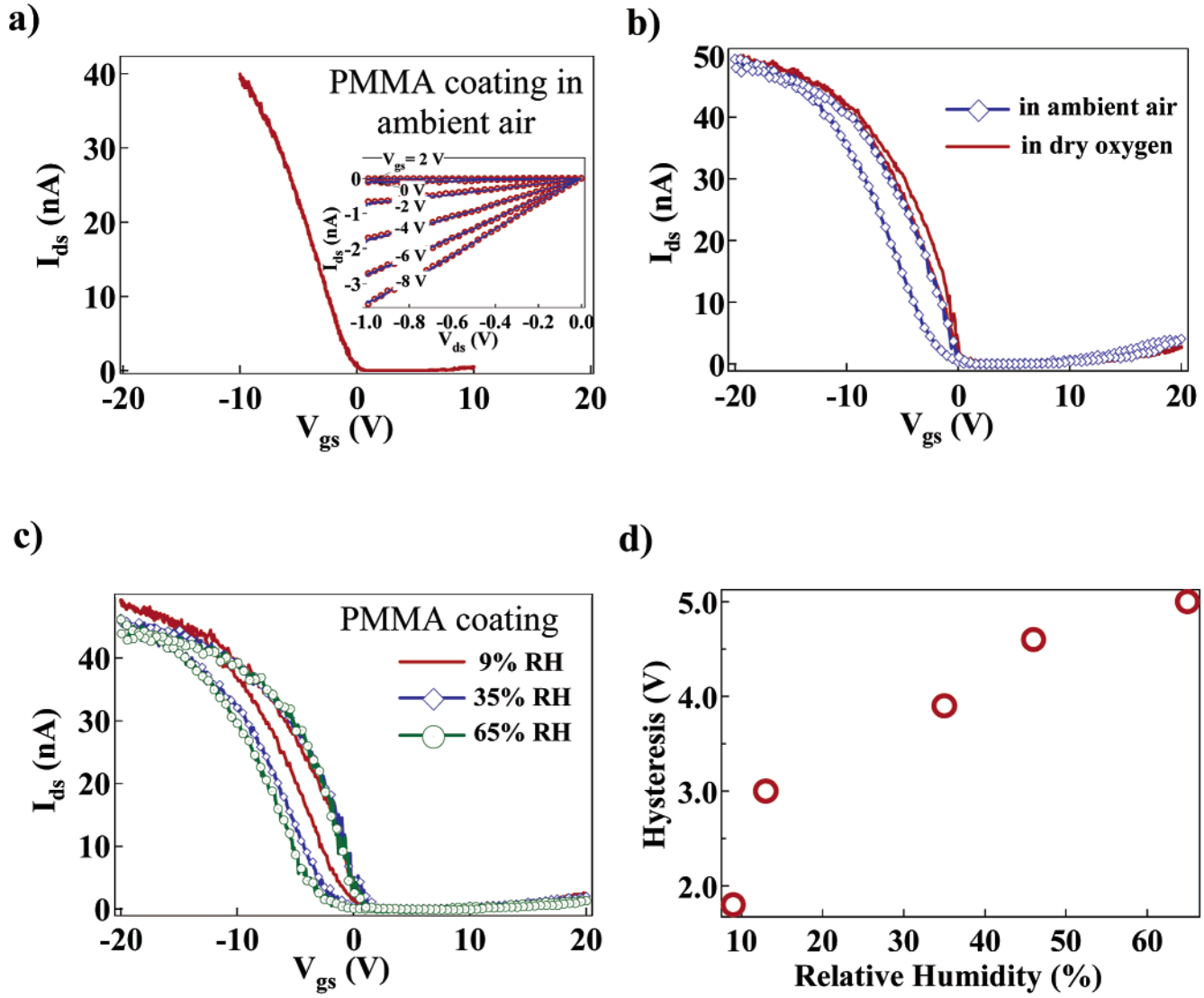

Figure 5. (a) PMMA-coated SWNT FET shows near-zero hysteresis in ambient air after baking at 150 °C. V_{ds} = 10 mV. The inset shows $I_{ds}-V_{ds}$ data for several V_{gs}. Solid lines and symbols (red circles) are two data sets recorded during increasing and decreasing V_{gs}, respectively. The two data sets overlap very well, meaning the $I_{ds}-V_{ds}$ curves depend only on V_{gs}, not on the history of V_{gs} in the [−10 V, 10 V] range. (b) Same device exhibits an ∼2.5 V hysteresis in V_{gs} under a larger V_{gs} sweep range of [−20 V, 20 V] under ambient conditions. The hysteresis significantly decreases in dry oxygen. (c) Evolution of $I_{ds}-V_{gs}$ curves for the device under varying humidity. (d) Hysteresis in V_{gs} vs humidity data. The hysteresis was measured at the $I_{ds} \approx$ 25-nA level.

hysteresis in SWNT FETs exposed to the ambient environment. We suggest that two types of water charge traps exist. Type I involves water molecules weakly adsorbed on the nanotube surface, and these molecules can be easily removed by pumping in vacuum, as in the case of suspended-tube devices. Type II involves SiO_2 surface-bound water in close proximity to the nanotubes. The thermally grown SiO_2 substrates on which SWNT FETs are fabricated have surface chemistry that is similar to that of silica.[18−20] When stored in ambient air, the thermally grown SiO_2 surface consists of Si−OH silanol groups and is hydrated by a network of water molecules that are hydrogen bonded to the silanols.[18−20] A multilayer of surface-bound water could exist in ambient air (relative humidity 40−50%) because of hydrogen bonding among water molecules. Similar to the effect of heating in vacuum, the CVD nanotube growth condition at 900 °C may dehydrate the surface and condense the silanols to form Si−O−Si siloxanes. However, when exposed to and stored in ambient air, the surface siloxanes on the substrate react with water and gradually revert to Si−OH, after which the substrate becomes rehydrated.[18−20] It is well known that a monolayer or submonolayer of hydrogen-bonded water remains on SiO_2 and cannot be removed by pumping in vacuum over extended periods of time at room temperature.[18−20] This is responsible for the residual hysteresis observed in the nanotube FETs after prolonged vacuum treatment.

It is also known that water bound to silanols on SiO_2 can be removed by heating in dry environments to ≥200 °C.[18−20] This is consistent with our result that hysteresis in SWNT FETs (tube-on-SiO_2 devices) is nearly eliminated or at least drastically reduced after heating to 200 °C in H_2 for 4.5 h, cooling to room temperature, and then exposing to dry air (Figure 4). A large amount of hysteresis returns immediately

upon exposure of the devices to ambient air (data not shown). All of the hysteresis phenomena correlate with the H_2O-SiO_2 surface chemistry very well. This correlation, plus the fact that water is known to act as slow charge traps (removable by annealing in dry conditions) in conventional metal oxide−semiconductor (MOS) devices,[21−23] leads to the conclusion that surface water is largely responsible for the hysteresis in the nanotube FETs.

We can roughly estimate the amount of charge trapping by water molecules on the basis of gate capacitances in SWNT devices. For SWNTs on $h = 500$-nm-thick SiO_2, the unit-length back-gate capacitance is[24] $C_{gs} = 2\pi\epsilon\epsilon_0/[\cosh^{-1}(h/r)] \approx 2\pi\epsilon\epsilon_0/\ln(2h/r) = 0.0322$ aF/nm (or 0.322 pF/cm), where the SiO_2 dielectric constant is $\epsilon \approx 4$ and $r \approx 1$ nm is the typical tube radius. In a dry environment, the threshold voltages (V_T) for forward and backward V_{gs} scans are −3 V and +3.5 V, respectively, as a result of hysteresis (Figure 2b). The number of charges trapped per unit length is $Q \approx C_{gs}|V_T| = 1.3\ |e|$/nm ($e$ = elemental charge). This corresponds to charging by $\sim 0.005|e|$ per carbon atom for a typical 2-nm tube. According to the SiO_2 surface-chemistry literature,[25] the density of silanol-bound surface water (type II, monolayer) on SiO_2 is $\sim 10/nm^2$, corresponding to a line density of 20/nm within a ∼2 nm width around the nanotube. This suggests charging by roughly $0.1|e|$ for each H_2O molecule in the vicinity of the nanotube. The estimates here should be taken as specific to the V_{gs} sweep range ([−10 V, 10 V]) and sweep rate for the current devices.

For SWNT FETs to become useful components for practical electronics applications, passivation should be devised to eliminate the undesired hysteresis. We find that as a first step, coating nanotube devices with PMMA can afford nearly hysteresis-free FETs. This is done simply by spin casting (at 4000 revolutions per min for 30 s) a 9% PMMA (molecular weight 950K) chlorobenzene solution onto the as-made SWNT transistors, followed by baking the devices on a hot plate at 150 °C for ∼24 h (all steps carried out in ambient air, PMMA thickness ≈ 1.7 μm). Figure 5a shows that under a V_{gs} scan range of [−10 V, 10 V] and a scan rate of ∼1 V/s, a PMMA-coated device exhibits near-zero hysteresis in the ambient atmosphere (results reproduced with >10 devices). We attribute the passivation to two factors. First, the ester groups of PMMA can hydrogen bond with silanol groups on SiO_2.[26] Baking at 150 °C combined with the polymer−SiO_2 interaction can significantly remove the silanol-bound water. Second, PMMA is hydrophobic and can keep water in the environment from permeating the PMMA and adsorbing on the nanotube in a significant manner. Nevertheless, in ambient air, over a larger V_{gs} sweep range of [−20 V, 20 V] and a scan rate of 1 V/s, an ∼2.5 V hysteresis in V_{gs} is still observed for the PMMA-coated devices (Figure 5b). The same device placed in dry oxygen (under identical gate-sweep conditions) exhibits a clear reduction in hysteresis (Figure 5b). When investigating hysteresis versus humidity for the device (humidity adjusted by mixing dry air and wet air in various ratios before flowing into a test chamber in which the device resides), we clearly observe increased hysteresis at higher humidity (Figure 5c and d). This is likely due to a higher concentration of permeated H_2O molecules in the PMMA layer.

For modern Si electronics, much is known about the causes and elimination of hysteresis in metal oxide semiconductor (MOS) FETs. The common types of charge traps include[27] (i) SiO_2/Si interface trapped charges due to the interruption of the periodic Si lattice structure (these charges can rapidly exchange with Si); (ii) fixed immobile oxide charges near the SiO_2/Si interface; (iii) mobile ionic charges due to alkaline ion (e.g., Na^+) contaminants that can be manipulated by bias-temperature aging; and (iv) oxide-trapped space charge associated with defects in SiO_2. Charge traps due to water have been reported for MOSFETs without encapsulation/passivation.[22] Slow states due to water charge traps have also been observed in MOS capacitances and tunnel diodes with hydrated SiO_2 gate insulators.[21,23] These water-related slow charge traps are all removable by thermal annealing in dry atmospheres.[21−23] For nanotube FETs, previous work attributed hysteresis to charge traps related to SiO_2/Si.[11,12,14] We have shown here that water molecules are in fact by far the most significant charge traps for the nanotube FET structures commonly used. These traps are charged and discharged slowly, with the discharge mechanism likely being ionic conduction through water. We do not rule out the existence of SiO_2/Si-related charge traps in the nanotube FETs. However, they are not the main causes of hysteresis over the gate-voltage ranges under which nanotube transistors typically operate.

The current work reveals that simple surface chemistry manifests itself strongly and can dictate the properties and potential applications of nanoscale devices. The finding of hysteretic charge trapping in surface water is of fundamental importance not only to nanotube transistors but also to devices constructed on surfaces for other chemically derived nanomaterials. Truly robust passivation of these devices must be developed for practically useful electronics. However, an orthogonal direction is to control the surface chemistry and devise specific coatings for these devices aimed at nanoscale detectors including humidity sensors.

Acknowledgment. We acknowledge Professor D. Antoniadis for insight on hysteresis in silicon electronics and Professor C. Chidsey for insight on SiO_2 surface chemistry. This work was supported by the MARCO MSD Focus Center, DARPA/MTO, SRC/AMD, and the Packard, Sloan and Drefus Foundations.

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NL0259232