High-κ dielectrics for advanced carbon-nanotube transistors and logic gates

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The integration of materials having a high dielectric constant (high-κ) into carbon-nanotube transistors promises to push the performance limit for molecular electronics. Here, high-κ (~25) zirconium oxide thin-films (~8 nm) are formed on top of individual single-walled carbon nanotubes by atomic-layer deposition and used as gate dielectrics for nanotube field-effect transistors. The p-type transistors exhibit subthreshold swings of S ~ 70 mV per decade, approaching the room-temperature theoretical limit for field-effect transistors. Key transistor performance parameters, transconductance and carrier mobility reach 6,000 S m^{-1} (12 μS per tube) and 3,000 cm^2 V^{-1} s^{-1} respectively. N-type field-effect transistors obtained by annealing the devices in hydrogen exhibit S ~ 90 mV per decade. High voltage gains of up to 60 are obtained for complementary nanotube-based inverters. The atomic-layer deposition process affords gate insulators with high capacitance while being chemically benign to nanotubes, a key to the integration of advanced dielectrics into molecular electronics.

High-κ dielectrics have been actively pursued to replace SiO_2 as gate insulators for silicon devices[1]. The relatively low κ of SiO_2 (at 3.9) limits its use in transistors as gate lengths scale down to tens of nanometres. High-κ gate insulators afford high capacitance without relying on ultra-small film thickness, thus allowing for efficient charge injection into transistor channels and meanwhile reducing direct-tunnelling leakage currents. This has motivated intense research in the synthesis and device integration of high-κ films—κ ~ 20–30, for example, in zirconium oxide (ZrO_2) and hafnium oxide (HfO_2)[2,3]—an area that is at one of the forefronts of materials science and semiconductor electronics[4].

Molecular electronics is an emerging area with a goal of using molecular materials as core device components. An advantage is that molecular structures are small in size, surpassing structures attainable by top-down lithography, and could therefore be essential to miniaturization. Yet, a wide-open question is whether molecular materials could bring about higher device performance than conventional electronic materials, especially for the most basic and widely used device units, field-effect transistors (FETs). The intrinsic electrical properties of molecular materials combined with advanced gate dielectrics may open a new route to advanced miniature field-effect devices.

Single-walled carbon nanotubes (SWNTs) are wires with molecular-scale diameters (~1 nm), and individual semiconducting SWNTs have been actively explored to construct nanotube FETs[5]. One of the promises of SWNTs for transistors is the high carrier mobility[6–10], because electrical transport in high-quality nanotubes can be ballistic[11–13]. In terms of gating of nanotubes, the most widely used gate structure has been macroscopic, doped Si substrates as back-gates and thermally grown SiO_2 as gate dielectrics[6,14,15]. Several new gate structures have been developed for nanotubes, including bottom aluminium gates with subnanometre-thick native Al_2O_3 dielectrics[16], top-gates with SiO_2 dielectrics ~15–20 nm thick[17], bottom tungsten gates with SiO_2 dielectrics[18] and electrochemical gates with an aqueous electrolyte solution as dielectrics[8]. These works have produced progressively improving nanotube transistor characteristics. For instance, the

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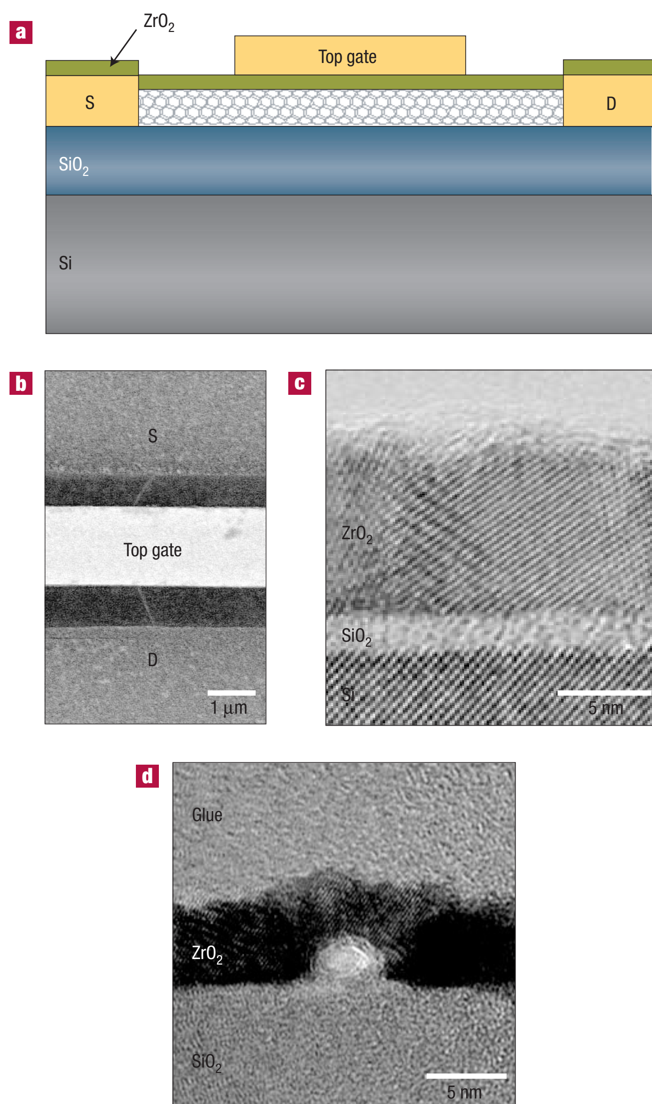

Figure 1 Integrating high-κ dielectrics into molecular transistors. a, Sideview of a SWNT-FET with ALD-ZrO_2 as the gate dielectrics (source S, and drain, D electrodes). The nominal thickness of ZrO_2 used for our FETs is 8 nm. The thickness of thermally grown SiO_2 on the Si substrate is 500 nm. **b**, Scanning electron microscopy (SEM) image of a ZrO_2/SWNT-FET viewed from the top. An individual SWNT can be seen with the ZrO_2 film on top. The gated length of the nanotube ~2 µm. **c**, Cross-section transmission electron microscopy (TEM) image of an 8 nm ZrO_2 deposited by atomic layer deposition on ~1.4 nm thermally grown SiO_2. **d**, TEM image of the cross-section of a SWNT on SiO_2 with conformal coating of 4-nm-thick ZrO_2. The circular region at the ZrO_2-SiO_2 interface is the cross-section of a nanotube that exhibits light contrast in the TEM.

subthreshold swing (S), a parameter key to the scaling of FETs has reached S ~ 130 mV per decade for top-gated nanotubes[17], and S ~ 80 mV per decade for solution-gated SWNTs[8].

Here, we report the integration of thin films (~8 nm) of ZrO_2 high-κ dielectrics (κ ~ 25) into SWNT-FETs. The atomic-layer deposition (ALD) process[3,19] used for ZrO_2 is benign to nanotubes, that is, it does not destroy their electrical properties. The high capacitance of ZrO_2 dielectrics affords subthreshold swings of S ~ 60–80 mV per decade for p-type ZrO_2/SWNT-FETs and S ~ 90–100 mV per decade for n-type FETs. The transconductance of these transistors reach ~6,000 S m^{-1} (normalized by the width of nanotubes), exceeding that achieved for silicon devices. High carrier mobilities in the ZrO_2/SWNT-FETs of the order of ~3,000 cm^2 V^{-1} s^{-1} are observed. Further, complementary inverters exhibiting voltage gains of up to 60 (the highest reported to date for nanotube-based logic gates) are obtained.

The devices used in this work were composed of individual semiconducting SWNTs synthesized by chemical vapour deposition (CVD)[20], bridging metal source (S) and drain (D) electrodes (of spacing ~3 µm) on SiO_2/Si substrates. A ZrO_2 dielectric layer with nominal thickness of 8 nm was formed by ALD[3,19] on top of an array of SWNT-FETs[9] (with a common Si back-gate), followed by patterning local top-gates (2 µm wide) located between the S and D electrodes for each of the transistors (Fig. 1a,b and Methods). The quality of ZrO_2 films was investigated by transmission electron microscopy (TEM). Cross-sectional TEM revealed excellent crystallinity of ZrO_2 film on SiO_2 substrate (Fig. 1c) and coverage of ZrO_2 on the SWNTs (Fig. 1d).

We have carried out systematic electrical transport measurements of more than 30 ZrO_2/SWNT-FETs obtained from different batches of chips that experienced independent nanotube growth, fabrication and ZrO_2 ALD processes. Figure 2a shows the typical current (I_{ds}) versus gate voltage (V_{gs}) characteristics for an as-made (p-type) SWNT transistor when back-gated through a 500-nm-thick SiO_2 layer (circles), and when top-gated through a ZrO_2 dielectric layer (solid line). A drastic difference is the subthreshold swing S, defined as $S = \ln(10)[dV_{gs}/d(\ln I_{ds})]$ (ref. 21). With back-gate and a SiO_2 dielectric 500 nm thick, the device exhibits a subthreshold swing of S ~ 1–2 V per decade. With top-gate and a ZrO_2 dielectric 8 nm thick, S ~ 70 mV per decade; up to five orders of magnitude change in current is observed for a top-gate voltage change of ~0.4 V (Fig. 2b). Subthreshold swings for all of our p-type ZrO_2/SWNT-FETs are reproducibly measured in the S = 70–100 mV per decade range for various bias voltages V_{ds} = –0.01 to –1 V (Fig. 2b). Importantly, the tunnelling leak current through the ~8-nm-thick ZrO_2 dielectric layer is negligible in the range of gate voltages of ≤ 3 V (Fig. 2d).

The subthreshold swing is a key parameter to transistor miniaturization. A small S is desired for low threshold voltage and low-power operation for FETs scaled down to small sizes[22]. Within the model for metal oxide semiconductor FETs (MOSFETs)[21], S is determined by $S = \ln(10)[dV_{gs}/d(\ln I_{ds})] = (k_B T/e)\ln(10)(1+\alpha)$, where T is temperature, k_B is Boltzmann's constant, e is the elementary charge and α depends on capacitances in the device and is ~0 when the gate capacitance is much higher than other capacitances. The lowest theoretical limit for S is therefore $S = (k_B T/e)\ln(10) \approx 60$ mV per decade at room temperature[21]. Intense effort has been made to reach this limit for Si-based devices, and new types of transistor schemes have been sought to overcome this barrier. In this regard, the S of 70 mV per decade reached by our ZrO_2/SWNT-FETs are significant.

Figure 2c shows typical current versus source–drain bias voltage curves (I_{ds}–V_{ds}) under various gate voltages V_{gs} in steps of 0.1 V for the ZrO_2/SWNT transistors. The shapes of the I_{ds}–V_{ds} curves closely resemble those of conventional p-MOSFETs, exhibiting linear triode regions at low V_{ds}, and saturation regions at higher V_{ds}. The MOSFET square law model[21] seems to fit the I_{ds}–V_{ds} characteristics of our devices very well[23]. In the saturation regions of the I_{ds}–V_{ds} curves, we deduce a transconductance of $g_m = dI_{ds}/dV_{gs}|_{V_{ds} = -1.2\,V}$ = 12 µS. Normalized by the width of the nanotube d ~ 2 nm, a transconductance of 6,000 S m^{-1} is obtained. A fair comparison between our nanotube FETs and Si-based devices turns out to be non-trivial due to the quasi-one-dimensional nature of SWNTs. The apparent diameter-normalized transconductance for our device is about 10 times higher than that in p-type crystalline Si. However, this normalization requires justification. As pointed out by theory, the effective device width for a nanotube transistor should be about twice the nanotube diameter $2d$ ~ 4 nm, that is the effective gate-width because the charge distribution on the gate plane spreads over a larger width than the tube diameter[24].

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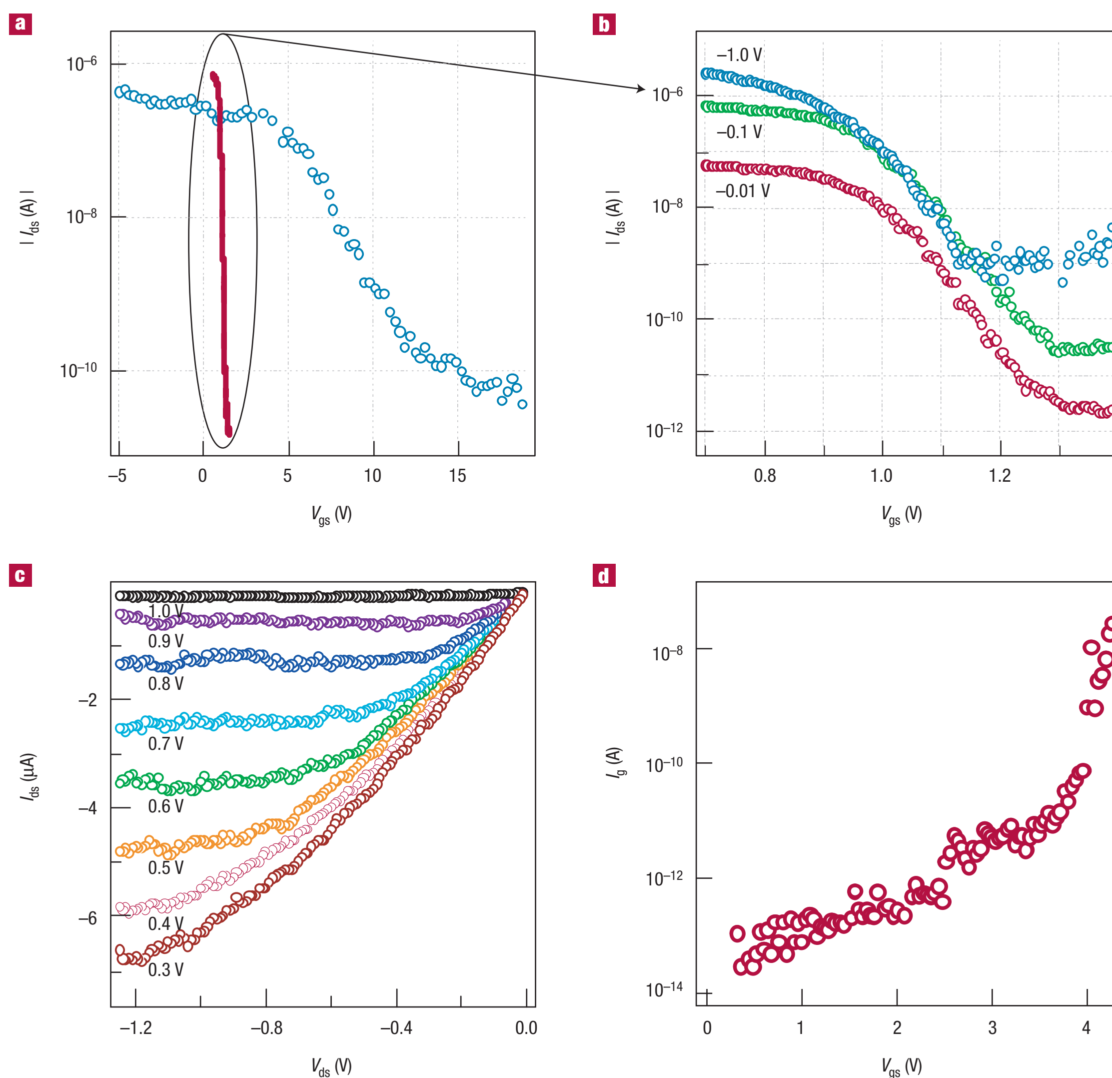

Figure 2 Characteristics of a p-type SWNT-FET with high-κ gate insulator. a, I_{ds}–V_{gs} curves recorded under V_{ds} = −100 mV with bottom Si/SiO_2 gate (circles) and top-gate/ZrO_2 (solid curve) respectively. The bottom-gate was grounded during top-gate operation of our transistors throughout this work. **b**, I_{ds}–V_{gs} curves recorded with top-gate/ZrO_2 at bias voltages of V_{ds} = −10 mV, −0.1 V and −1 V, respectively. **c**, I_{ds}–V_{ds} curves of the FET recorded for various top-gate voltages at 0.1 V steps. **d**, Gate leak current versus top-gate voltage. The leak current is negligible (at the pA level) until V_{gs} > 3 V.

This has important consequences when packing parallel nanotubes for transistors[24,25]. Taking the effective width of our devices to be ~2*d*, we derive a transconductance of 3,000 S m^{-1}, which is still well above that achieved in the state-of-the-art Si MOSFETs (~800 S m^{-1} for the Intel 60 nm transistor[26,27]). This is a significant result because high transconductance is critical to the performance of transistors and voltage gains of transistor-based devices including amplifiers and logic gates.

To further analyse the performance parameters for the ZrO_2/SWNT-FETs, we first consider the gate capacitance. For a quasi-one-dimensional SWNT channel, the electrostatic gate-coupling capacitance has a logarithmic dependence on the thickness of the dielectric layer[28], $C_{g_ZrO2} = 2\pi\varepsilon\varepsilon_0 L/[\cosh^{-1}(h/r)] \approx 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$ where the ZrO_2 dielectric constant ε ~25 and thickness h = 8 nm. For a nanotube with gated length of L ~ 2 μm and radius r ~ 1 nm, the electrostatic capacitance C_{g_ZrO2} = 1.1 fF (unit length capacitance 5 pF cm^{-1}). This capacitance is slightly higher than the quantum capacitance of the 2 μm gated nanotube C_{g_Q} = 0.8 fF (unit length quantum capacitance 4 pF cm^{-1})[8,24]. The total gate capacitance is then $C_{gs} = (C_{g_ZrO2}C_{g_Q})/(C_{g_ZrO2} + C_{g_Q})$ = 0.46 fF. We borrow the standard transistor model to analyse the carrier mobilities in our devices. In the low-bias linear-triode regions of the I_{ds}–V_{ds} curves, the hole mobility μ_h can be deduced from[21] $g_{ds} = I_{ds}/V_{ds} = 2K(V_{gs}-V_T)$, where g_{ds} is the zero bias conductance, K is the conductivity parameter given by $K = \mu_h C_{gs}/2L^2$, and V_T = 1 V is the threshold gate voltage for the device. Alternatively, we derive the carrier mobility from the saturation regions of the I_{ds}–V_{ds} curve by $I_{ds} = K(V_{gs}-V_T)^2$. Both methods yield μ_h ~ 3,000 cm^2 V^{-1} s^{-1}, which is about 8 times higher than that in p-type bulk crystalline Si (~450 cm^2 V^{-1} s^{-1}). Further, in an actual Si MOSFET, the hole-mobility is about half of that of bulk Si due to surface roughness scattering.

We note that our device differs from previous nanotube transistors in that the top gate covers a ~2-μm-long segment of the SWNT instead of the full length between the S and D electrodes. Despite this difference, the apparent transistor performance parameters can be compared

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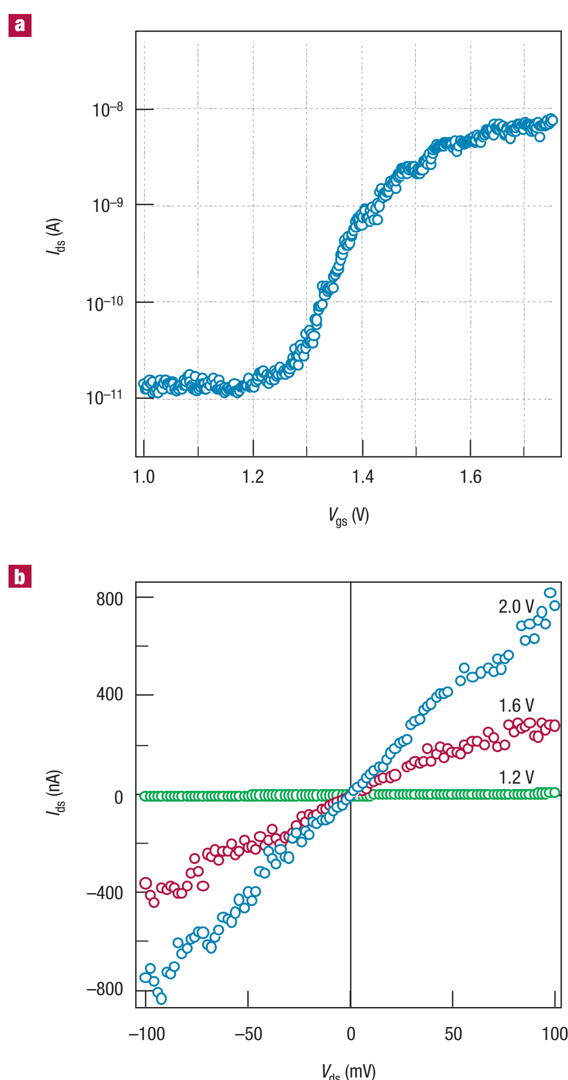

Figure 3 Characteristics of an n-type SWNT-FET with high-κ gate insulator. a, I_{ds}–V_{gs} curve for a device recorded under a V_{ds} = 10 mV bias. **b**, I_{ds}–V_{ds} curves for the device at various top-gate voltages. Note that the top-gate can act like a side-gate to the ungated sections (see the SEM image of the device structure in Fig. 1b) for n-gating of these sections, but not with high efficiency. The n-type devices obtained by annealing in hydrogen recover to p-type after exposure to air for about one day. This indicates that the 8-nm-thick ZrO_2 does not completely block oxygen (without the ZrO_2 coating, our back-gated devices recover to p-type in ~1 h).

because they are extracted from transport data in similar manners as for earlier devices. The subthreshold swing for our ZrO_2/SWNT-FETs is S ~ 70 mV per decade, superior to devices with bottom gates and Al_2O_3 and SiO_2 dielectrics (S ~ 180 mV per decade[16] and 400 mV per decade[18] respectively), and to those with top-gates through SiO_2 (S ~ 130 mV per decade[17]). In aqueous electrolyte solutions, the high dielectric constant of water (κ ~ 80) affords subthreshold swings of S ~ 80 mV per decade[8]. SWNT Schottky barrier FETs have been reported with HfO_2 (κ ~ 7) dielectrics and S ~ 120–130 mV per decade[29]. The diameter-normalized transconductance of 6,000 S m^{-1} for our ZrO_2/SWNT-FETs is the highest among solid-state gated-tube devices. Transconductance normalized in the same manner for top-gated SiO_2 (layer thickness 15 nm)/SWNT-FETs is ~2,300 S m^{-1} (ref. 17), and 300 S m^{-1} for bottom-gated Al_2O_3/SWNT-FETs[16]. Also, the mobility measured in our devices is among the best for SWNT-FETs gated by global back-gates and electrolytes[6–10].

It is not likely that our devices operate as Schottky barrier FETs as suggested for fully gated SWNTs[29–31]. Because our top-gate is directly on top of the gated-tube section and ~0.5 μm away from the S/D metal contacts, switching of our device should be dominated by carrier depletion along the bulk length of the nanotube, not by change of Schottky barriers at the S/D contacts. The extracted carrier mobility for our devices involves resistance within the nanotube.

The high-κ ZrO_2 gate insulator affords high gate capacitance critical to the small subthreshold swings and high transconductance. Comparatively, for SiO_2 dielectrics, to obtain an electrostatic coupling capacitance approaching the quantum capacitance of an SWNT, an ultra-thin 1–2 nm SiO_2 layer is required because the electrostatic coupling capacitance logarithmically depends on thickness. The thin SiO_2 causes substantial leakage currents, a problem well-known in conventional transistor scaling[32]. Thus far, the thinnest SiO_2 dielectric layers used for nanotube transistors are 15–20 nm, and the subthreshold swings observed are S ~ 130 mV per decade[17].

Carrier mobility is a parameter intrinsic to materials properties. It is important to note that the ZrO_2 deposited on top of SWNTs by ALD is benign and does not destroy nanotubes, and in fact does not significantly reduce the apparent carrier mobility by introducing a high density of scattering sites. Also important is that the typical ON-state resistance of the ZrO_2/SWNT-FETs is ~100–500 kΩ, similar to those that did not undergo ZrO_2 ALD[6,8]. The compatibility of ALD with nanotubes, which was not obvious at first considering the oxidative H_2O and ion species involved in ALD at 300 °C, is key to fabrication of integrated SWNT/high-κ dielectrics devices. As an aside, we found that several thin-film deposition methods are incompatible with nanotubes. Deposition of SiO_2 on nanotubes by sputtering or plasma-enhanced CVD resulted in complete loss of electrical connection in our SWNT devices.

The as-made p-type ZrO_2/SWNT-FETs are converted to n-type transistors by heating in molecular hydrogen at 400 °C for 1 h. Figure 3 shows the characteristics of a typical n-type ZrO_2/SWNT-FET obtained in this way. The n-FET has S ~ 90–100 mV per decade (Fig. 3a), with a transconductance of ~600 S m^{-1}, and electron mobility of μ_n ~ 1,000 cm^2 V^{-1} s^{-1}. These characteristics are excellent compared to previous n-type SWNT-FETs with back-gates or local-gates obtained by alkali[33,34] or functional-group charge-transfer doping[7] or heating in inert environments[34]. Nevertheless, the performance of the n-type ZrO_2/SWNT-FET is not as ideal as our p-type FETs with higher S and resistance (~1 MΩ) and lower ON/OFF ratio.

Our as-made back-gated devices appear p-type (typically in enhancement mode, where $V_T \le 0$) with no appreciable n-channel conduction under high positive back-gate voltages. It has been shown[31,35] that hole-doping of the bulk length of SWNTs by adsorbed oxygen[36,37] is insignificant. N-channel conduction is not favoured due to large band bending at the metal-tube junctions. Removal of oxygen on the S/D metal by annealing affects the metal work function and lowers the barrier for n-conduction[38]. For our devices after the ALD ZrO_2 deposition, we always observe a shift in the I_{ds}–V_{gs} curves towards the more positive V_{gs} side by ~10 V (V_T ~ 10 V with back-gate), signalling significant additional hole-doping to the SWNTs. We attribute the additional doping to the oxidative species or charge traps in ZrO_2. ALD of ZrO_2 using a $ZrCl_4$ precursor is known to leave up to 1 atom% of chloride ions (P. McIntyre, unpublished results) that could cause hole-doping or act as charge traps. This contributes to the normally ON operation for our p-ZrO_2/SWNT-FETs (depletion mode) with a relatively high top-gate threshold voltages of V_T ~ 1 V (corresponding to a p-doping fraction of f ~ 0.01 estimated from capacitance and V_T). Annealing in hydrogen removes oxygen in our devices, which could lower the barriers at the S/D contacts for n-channel transport.

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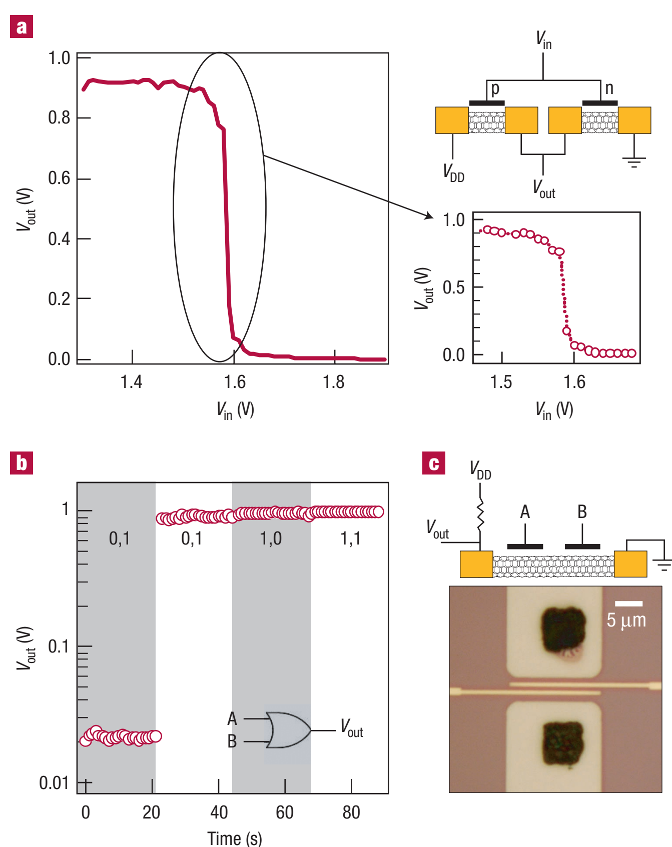

Figure 4 Logic gates built from nanotube transistors with high-κ dielectrics. **a**, Transfer characteristic for a complementary NOT logic (inverter) operated at $V_{DD} = 1$ V. The right panel shows the schematic device structure and a zoom-in of the transfer characteristics in the inversion region. Note that the operating input voltage range for the inverter is higher than that of the output. Additional amplifiers in conjunction with the ZrO_2/SWNT inverters are needed to realise high voltage gain in a real device. The high threshold voltages for the p- and n-FETs are responsible for the asymmetric transfer characteristics, and can be adjusted by controlling the bulk-length nanotube doping. Defining the threshold voltages remains an issue to be addressed in the nanotube transistor area. Nevertheless, our data here clearly suggests the potential of high-gain devices based on nanotube transistors with integrated high-κ dielectrics. **b**, An OR gate output characteristics for a nanotube with double top-gates. The right panel shows the schematic and an optical image of the device. The operating voltage is $V_{DD} = 1$ V. The inputs for the two gates, A and B, are 2 V for state 1 and 0 V for state 0.

Nevertheless, the operation of our n-ZrO_2/SWNT-FETs, with the seemingly ungated tube sections, is not yet understood. The n-FETs show relatively high threshold voltages ($V_T \sim 1.2$ V, enhancement-mode) and high ON-state resistance, possibly due to inefficient n-doping/gating of the ungated sections. One possible factor for n-gating to these sections is fringing fields originating from the top-gate (≤ 0.5 µm away) under $V_{gs} > V_T$. In any event, the partial-gating structure is not desired for n-type FETs, and can be significantly improved with fully gated structures or by direct doping of the ungated sections chemically or by resorting to the back-gate.

The ability to obtain both p- and n-type FETs is important to construct complementary electronics that are known to be superior in performance (for example, low power) on to devices consisting of unipolar p- or n-type transistors. We have constructed a NOT logic gate, that is, an inverter, by connecting a p- and n-type ZrO_2/SWNT-FET (Fig. 4a). The most noteworthy characteristics of the inverter based on the ZrO_2/SWNT-FETs is the high voltage gain (Fig. 4a). In the inversion region of the transfer characteristics, the output voltage changes by 0.6 V on an input voltage change of 10 mV, giving rise to a voltage gain of up to $\beta = \Delta V_{out}/\Delta V_{in} \sim 60$. This is the highest gain obtained with any molecular materials including SWNT and conjugated organic materials. Voltage gains reported previously for complementary SWNT inverters are ~2 and 8 for back-gated[34] and local bottom-gated devices[18], respectively. The high gain for our ZrO_2/SWNT inverters is a direct result of the high performance of the p- and n-ZrO_2/SWNT transistors, owing to the high transconductance.

Finally, we demonstrate that fabricating multiple local-gate electrodes on ZrO_2 dielectrics and SWNTs readily allows for diverse electronic functions based on individual nanotubes. An OR gate is obtained with two gate electrodes fabricated on ZrO_2 and a p-type SWNT in conjunction with a 10 MΩ resistor (Fig. 4b). The OR function occurs because the output voltage is low when both gates are at low voltages so that the nanotube channel is in the ON-state. When one or both gates are at high voltages, the nanotube channel is electrically shut off, resulting in a high output voltage defined by the input (Fig. 4b).

In summary, we have integrated ZrO_2 high-κ dielectrics into SWNT transistors. ALD, a promising technique for deposition of high-κ dielectrics in scaling silicon electronics, is benign to carbon nanotubes. The electrostatic capacitance attainable with ~10-nm-thick ZrO_2 gate insulators exceeds the quantum capacitance of SWNTs, which is difficult to obtain by scaling SiO_2 films without producing large leakage currents. P-type SWNT-FETs coated by ZrO_2 dielectrics exhibit superior performance in subthreshold swings (70 mV per decade), high transconductance (12 µS per tube, 6,000 S m^{-1}) and mobility (3,000 $cm^2 V^{-1} s^{-1}$). High-performance n-type nanotube transistors with ZrO_2 gate insulators are also obtained. Complementary NOT gates constructed with the transistors exhibit the highest-to-date voltage gains (up to 60) for nanotube transistors. Thus, the integration of advanced dielectrics into nanotube materials is promising for pushing the performance limit of molecular electronics.

METHODS

SWNT-FETs WITH TOP-GATES AND ZrO_2 GATE DIELECTRICS

The substrates used were doped Si wafers with 500-nm-thick SiO_2 layers, and the doped Si used as the usual back-gate. Following a method described elsewhere[9], we first patterned Mo (50 nm thick) S–D electrode arrays on a substrate, followed by catalyst patterning on top of the electrodes and CVD growth of SWNTs to bridge the pre-formed source and drain. After growth, atomic force microscopy was used to identify devices in the array with S/D electrodes connected by individual SWNTs. Conductance versus back-gate measurements were then used to identify individual semiconducting nanotubes[6,14,15]. A ZrO_2 film of 8 nm nominal thickness was deposited onto the sample by ALD using $ZrCl_4$ precursor and H_2O oxidizer in a high purity N_2 carrier gas[3,19]. Films were deposited in a load-locked ALD research reactor with base pressure of 10^{-8} torr and a process pressure of 0.5 torr. The ZrO_2 ALD process was performed at 300 °C with alternating pulses (1–2 s duration) of the precursor and oxidizer. Each precursor/oxidizer pulse cycle resulted in the deposition of ~0.6 Å of ZrO_2 onto SiO_2. Cross-wafer ellipsometry measurements (calibrated by cross-sectional TEM) were used to confirm the film thickness and thickness uniformity of the ZrO_2 by ALD. Standard electron-beam lithography and lift-off processes were then used to pattern top-gates (Ti/Au, 60 nm thick) on the deposited ZrO_2 film between the S–D electrodes.

CROSS-SECTIONAL TEM

TEM was performed in a Philips CM20 microscope operated at an accelerating voltage of 200 kV. Thin foil specimens of SiO_2 substrates with ALD ZrO_2 (Fig. 1c) were prepared by typical mechanical polishing steps including cutting the substrate into half, bonding of the two pieces face-to-face by glue and thinning the cross-section followed by a brief argon-ion milling to perforation. Previous studies of ALD-ZrO_2 gate dielectric layers deposited on to oxidized Si surfaces have shown that the films are polycrystalline and exhibit the tetragonal zirconia crystal structure[3]. These results are consistent with TEM images obtained from the present zirconia dielectrics. For cross-sectional TEM of ZrO_2 coated SWNTs on SiO_2 (Fig. 1d), SWNTs were first grown on the SiO_2 substrate with discrete catalytic Fe_2O_3 nanoparticles deposited on the surface[39]. The number of SWNTs in a 10 x 10 µm^2 is about 20 measured by atomic force micsoscopy. ZrO_2 was then deposited on the sample, followed by TEM specimen preparation in the same way as the SiO_2/ZrO_2 samples. Note that the catalytic nanoparticles stayed at one of the ends of each SWNT[39]. Therefore, the SiO_2 substrate was clean, containing only nanotubes on the surface. Circular structures of 1–3 nm diameter, and with an image contrast lighter than the surrounding SiO_2 and ZrO_2 layers, were frequently observed in cross-sectional TEM (Fig. 1d) imaging of the SWNT samples, and were absent with SiO_2/ZrO_2 samples without SWNTs grown on the substrate. These structures were attributed to nanotubes observed in varying degrees of oblique cross-section, with the nanometre-scale region of lightest contrast corresponding to the nanotube.

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Competing financial interests

The authors declare that they have no competing financial interests

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