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Carbon Nanotube Transistor Arrays for Multistage Complementary Logic and Ring Oscillators

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ABSTRACT

This work demonstrates multistage complementary NOR, OR, NAND, and AND logic gates and ring oscillators (frequency ~220 Hz) with arrays of p- and n-type nanotube field effect transistors (FETs). The demonstration is made possible by progress in three aspects of nanotube synthesis and integration. First, patterned growth leads to large numbers of nanotube FETs in an array, as up to 70% of individual nanotubes are semiconductors. Second, metal electrodes are successfully embedded underneath nanotubes and used as local gates. Third, complementary logic gates are made possible by converting p-type FETs in an array into n-type FETs by a local electrical manipulation and doping approach.

Nanotubes and nanowires derived by bottom-up chemical routes could be useful quasi 1D building blocks for next generations of electronic devices.[1,2] Individual semiconducting single-walled carbon nanotubes (SWNTs) have been made into field effect transistors (FETs)[1] and intratube p−n junctions.[3,4] Inverters, the simplest form of logic gates, have been demonstrated using one and two nanotube FETs in unipolar[5] and complementary[6,7] modes. Ring oscillators with oscillation frequency of 5 Hz have been made using three unipolar p-type FETs and resistors.[5]

Several issues need to be addressed in order to impart complexity and advanced functionality or performance to nanotube based electronics. The first is to obtain large numbers of nanotube FETs reliably on substrates, a challenging task since only semiconducting nanotubes are useful for FETs, and an efficient assembly strategy must be developed for nanotubes. The former requires nanotube chirality control, and the latter requires placing nanotubes in arrayed fashion at specific locations with well-defined orientations.[8] The second issue concerns integration that requires nanotube FETs to be turned on or off by independent gates instead of by commonly used back-gates that manipulate all nanotubes on a substrate. This issue has been tackled recently.[5,9] Third, since complementary circuits comprising p- and n-type FETs are superior to unipolar devices known for Si technology, it is desired to control the doping of nanotube FETs locally and obtain large numbers of p- and n-FETs on the same substrate. This has not yet been achieved with nanotubes.

This letter presents an effort to address the issues above. We grow arrays of SWNTs by chemical vapor deposition (CVD) over catalytically patterned SiO_2 chips. Up to 70% of SWNTs produced by CVD are found to be semiconductors,[10] allowing for the fabrication of large numbers of nanotube FETs on the chip. Integrated local gates for the transistor arrays are obtained by embedding W metal electrodes underneath the SiO_2 dielectric layer prior to SWNT synthesis. Nanotube FET arrays with local bottom-gates are therefore obtained. While as-made FETs are all p-type, a local electrical manipulation method is found to be capable of converting specified tube FETs into n-type in oxygen-free environments. This local doping approach leads to multiple n-FETs coexisting with p-FETs on a chip. Complementary logic gates with up to six complementary transistors and three stage ring oscillators are then realized by simply connecting the n- and p-transistors.

Device fabrication involves the synthesis of SWNT arrays by CVD of methane on substrates prepatterned[11] with catalyst and bottom-W-gate arrays. Figure 1a shows the schematic structure of a final local gate device. A heavily doped Si wafer with 500 nm thick SiO_2 is used as the starting substrate. The gap region between the source and drain electrodes for each device is defined by photolithography and etched down by 50 nm followed by deposition of 50 nm W in the etched region. To maintain an overall flat surface morphology, the depth of oxide etching and thickness of deposited W gate electrodes are controlled to be approximately equal. A 200 nm thick SiO_2 gate dielectric is then deposited on top of the wafer using standard low-pressure chemical vapor deposition (LPCVD). The final device is obtained after patterning

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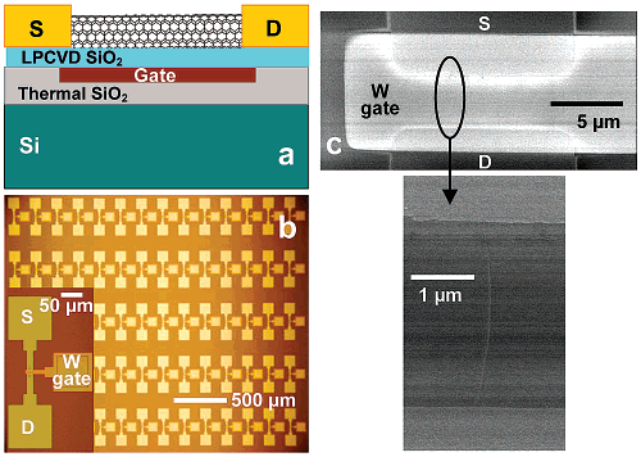

Figure 1. Patterned growth and integration for arrays of nanotube transistors with local bottom gates. (a) Schematic sideview of a SWNT-FET with a W local gate embedded in the SiO_2 substrate. The source (S) and drain (D) electrodes (distance between the edges of S and D = 3 μm) are made of Mo, fabricated prior to catalyst patterning and CVD growth.[12] The length of the embedded W gate is 7 μm, overlapping with S and D by ~2 μm. Note that preliminary results show this overlap can easily be reduced or removed to afford similar nanotube transistor characteristics as shown in this paper. (b) An optical image of an array of locally gated SWNT-FETs. Inset: A zoom-in optical image showing details of a SWNT-FET with W bottom gate. (c) A scanning electron microscopy (SEM) image of a SWNT-FET with bottom W gate. The W gate area appears bright due to charging in the SEM (the gate electrode is buried underneath a 200 nm insulating SiO_2 layer).

molybdenum source and drain electrodes,[12] followed by catalyst patterning and growth of SWNTs to bridge the preformed source/drain electrodes.[12] All patterning steps (for local gate, source/drain, and catalyst islands) in this work are carried out by optical lithography (Karl Suss MA-6 contact aligner) with mainly three masks and careful overlay alignment between successive steps. The catalyst used in this work is the same as that in ref 11, but growth takes place at 800 °C, under co-flows of CH_4,C_2H_4, and H_2 at 1000 × 0.72 (gas correction factor), 40 × 0.6, and 500 mL/min, respectively (Y. Li, H. Dai, unpublished). The W bottom gates provide a simple and efficient way for locally gating each individual FET and are compatible with the high-temperature SWNT growth process.

Shown in Figure 1b is a device array obtained by the synthesis and photolithography-based integration. A typical 4 × 4 mm^2 chip contains ~100 devices. The yield of nanotubes bridging the source-drain electrodes is typically ~50%, revealed by electrical probing. Among them, about 75% consists of individual SWNTs as revealed by atomic force microscopy (AFM) imaging. Approximately 60−70% of the as-made individual SWNT FETs are found to be p-type semiconductors by gate dependent electrical measurements in air. The high percentage of semiconductors is due to their "natural abundance" for SWNTs without chirality preference grown by CVD.[10] Thus, on a typical chip, we obtain ~20−30 SWNT FETs, each equipped with a local W bottom gate. This moderate yield is highly reproducible for different batches of samples. The individual SWNT FETs on a chip exhibit p-channel conductance from 100 to 300 kΩ. Variations in transconductance are also observed. We believe that these are mainly caused by the relatively large diameter distribution (1−4 nm) of the SWNTs and can be improved by synthesizing more homogeneous tube materials via catalyst control.[10,13] Nevertheless, the characteristics of SWNT FETs are sufficiently similar and consistent to each other to afford useful nanotube transistor arrays for this work. To make multistage logic gates, we simply wire-bond up to six FETs on a chip and then connect the transistors together using coaxial cables outside of the chip.

Device characterization is carried out with the nanotube chip placed in vacuum (10^{-8} Torr) at room temperature. Electrical measurements reveal that SWNT FETs remain p-type under these conditions. An interesting finding here, however, is that a p-type FET can be converted into n-type by applying a high local gate voltage combined with a large source-drain bias for certain duration. This conversion is shown in the current vs bottom gate voltage ($I-V_g$) curves in Figure 2a for a transistor before and after applying a local gate voltage of −40 V and a source-drain bias of 20 V for 5 min. We have observed such local "electrical n-doping" with at least 30 independent devices on 5−6 chips. We do note, however, that some of the p-FETs become rather insulating over a large gate range after this electrical manipulation step. The yield of p- to n- conversion by our local manipulation method is currently ~50%.

The mechanism underlying the p- to n- conversion of SWNT FETs by the local electrical manipulation process is explained as follows. Control experiments show that after exposing the n-type tube FETs to air, recovery to p-type behavior is reproducibly observed. This suggests that our electrical manipulation process in vacuum has caused desorption of molecular oxygen from SWNTs, leading to significant n-channel conduction. This is consistent with previous results that SWNTs similar to n-type SWNTs are obtained after desorbing oxygen by thermal annealing or photodesorption in vacuum.[14,15] Recovery to p-type upon air exposure can then be attributed to doping by adsorbed oxygen.[14−16] This then points to desorption of oxygen molecules during our electrical manipulation process. The current flowing across the tube at the high bias is up to ~50 μA under a large negative gate (SWNTs can survive such a high current in vacuum), which could simply cause molecular desorption by Joule heating. The detailed mechanism and other possible factors involved in our local conversion of nanotube FETs to n-type are being further investigated.

The ability of local manipulation of SWNT FETs into n-type has enabled us to obtain multiple n- and p-FETs on a SWNT chip and construct complementary logic devices. Figure 2b shows the output characteristics of an inverter, the simplest form of logic gates (NOT). It consists of an as-made p-type tube FET and an n-type FET, obtained by electrical manipulation. This complementary NOT logic gate exhibits a high voltage gain of ~8 (typical inverter gain 4−8), desired for multistage logic operations.

Complementary NOR, OR, NAND, and AND logic gates are built with up to six (3 p-type/3 n-type) SWNT-FETs. A NOR gate is obtained by connecting two p-FETs in parallel

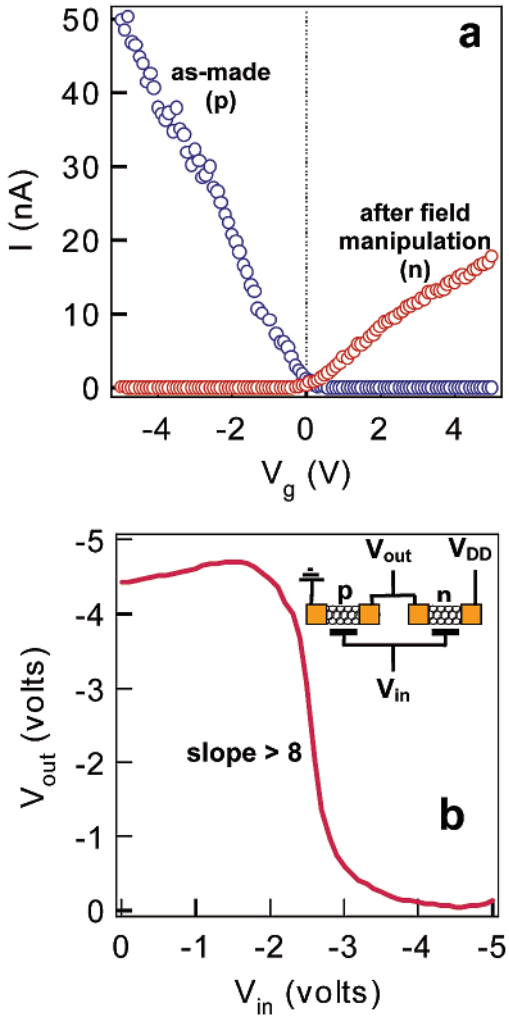

Figure 2. Local manipulation for n-type tube FETs for complementary devices. (a) Source-drain current vs gate voltage ($I-V_g$) curves of a SWNT-FET in air (blue) and after local electrical manipulation in vacuum (red), showing the p- to n-type conversion. Bias = 10 mV. (b) Transfer characteristics of an inverter made from a p-type nanotube FET and an n-type FET obtained by electrical manipulation. The operating voltage applied is $V_{DD} = -5$ V.

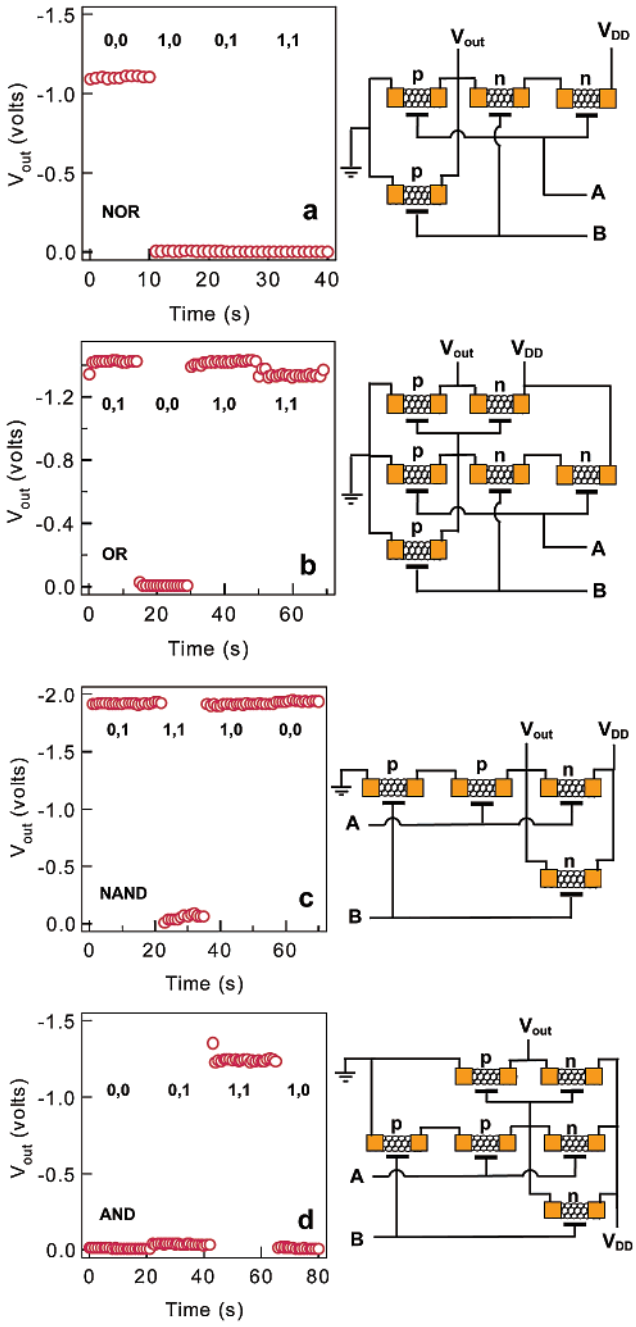

Figure 3. Multistage complementary nanotube logic. Ouput characteristics and structures of complemenary (a) NOR, (b) OR, (c) NAND, and (d) AND logic gates. The operating voltage is $V_{DD} = -1.5$ V for NOR, OR, and AND. $V_{DD} = -2.0$ V for NAND. The two inputs, A and B, used for each logic is −4 V for state 1 and 0 V for state 0.

and two n-FETs in series (Figure 3a). Its structure and NOR operation is very similar to that of complementary metal-oxide semiconductor (CMOS) NOR gates.[17] A complementary OR gate, shown in Figure 3b, is obtained by connecting the output of a NOR logic to the input of an inverter with a total of six tube FETs. By rearranging the connections between tube FETs, we also successfully demonstrate NAND (Figure 3c) and AND (Figure 3d) logic gates with four and six SWNT FETs, respectively.

For the first time, we obtain complementary SWNT ring oscillator with three SWNT based inverters. The output of each inverter is the input of the next. Returning the output of the third inverter to the first causes all the inverters to sequentially change logic state, resulting in a three-stage ring oscillator. The oscillating frequency of the device is measured to be ~220 Hz, much higher than previously achieved with unipolar nanotube devices (5 Hz). Nevertheless, this performance is still not optimized due to the current poor ability in interconnection as discussed below. The frequency of a ring oscillator is given by $f = 1/(2t_pN)$, where N is the number of stages and t_p is the propagation delay in voltage switching between successive inverter stages.[18] The propagation delay time t_p can be considered as due to the effective resistance-capacitance RC constant of the transistors. The measured frequency for our $N = 3$ stage oscillator, therefore, suggests an average $t_p \sim 0.75$ ms per stage for our device. Taking the average resistance of each tube FET during operation to be R on the order of 1 MΩ, we estimate that the capacitance

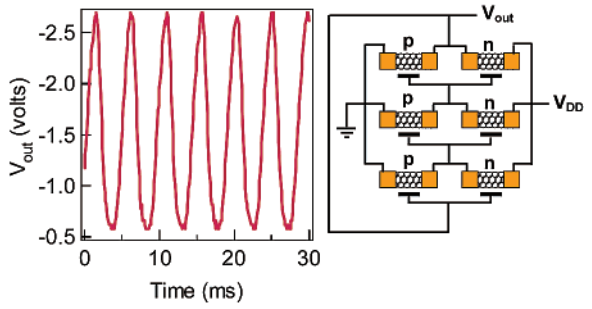

Figure 4. Ouput characteristics of a ring oscillator made of three complementary nanotube inverters. The output frequency is ~220 Hz. $V_{DD} = -4$ V.

of the device C ~ 750 pF. This high capacitance is in fact due to the coaxial cables used to connect the SWNT FETs, and is not the capacitance of the structures related to the nanotube FETs. The capacitance for an individual SWNT FET is estimated to be mainly the gate capacitance $C_g = 2\pi\epsilon\epsilon_0 L/\ln(2h/r) \sim 0.1$ fF (unit length capacitance 3×10^{-11}F/m), where the silicon oxide thickness $h = 200$ nm, dielectric constant $\epsilon \sim 4$, tube length $L = 3$ μm and radius $r \sim 1$ nm. The device capacitance is therefore orders of magnitude smaller than 750 pF, the extrinsic cable capacitance. The ring oscillator shown here thus is far from optimized and provides only a proof-of-concept with complementary nanotubes. Interconnecting tube FETs on a chip is clearly the next step for obtaining high performance devices and investigating the switching behavior intrinsic to SWNT transistor structures. The propagation delay is inversely proportional to carrier mobility,[18] and since the hole and electron mobilities have been shown to be up to 8000 cm^2/Vs for p- and n-tube FETs[19,20] and the resistance and channel lengths can be optimized, high performance nanotube ring oscillators (frequency >100 GHz) should be achievable.

To summarize, we have demonstrated nanotube array-based multistage complementary circuits. The nanotube transistor arrays are assembled via a patterned chemical synthesis approach, and from the synthesis, simple computing operations are made possible by using the high percentage of semiconducting SWNTs and the ability of local gating, manipulating, and doping individual SWNT-FETs. Many tasks and challenges lie ahead, including enabling device functions in nonvacuum conditions, obtaining massive and high-density transistor arrays, and interconnecting nanotubes on-chip.

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References

(1) Tans, S.; Verschueren, A.; Dekker, C. *Nature* **1998**, *393*, 49−52.
(2) Huang, Y.; Duan, X.; Cui, Y.; Lauhon, L.; Kim, K.; Lieber, C. *Science* **2001**, *294*, 1313−1317.
(3) Zhou, C.; Kong, J.; Yenilmez, E.; Dai, H. *Science* **2000**, *290*, 1552.
(4) Kong, J.; Dai, H. *J. Phys. Chem.* **2001**, *105*, 2890−2893.
(5) Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. *Science* **2001**, *294*, 1317−1320.
(6) Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, Ph. *Nano. Lett.* **2001**, *1*, 453−456.
(7) Liu, X.; Lee, C.; Zhou, C.; Han, J. *Appl. Phys. Lett.* **2001**, *79*, 3329−3331.
(8) *Carbon Nanotubes*; Dresselhaus, M. S., Dresselhaus, G., Avouris, Ph., Eds.; Springer: Berlin, 2001; Vol. 80.
(9) Wind, S.; Appenzeller, J.; Martel, R.; Derycke, V.; P, P. A. *Appl. Phys. Lett.* **2002**, *80*, 3817−3819.
(10) Kim, W.; Choi, H. C.; Shim, M.; Li, Y.; Wang, D.; Dai, H. *Nano Lett.* **2002**, *2*, 703.
(11) Kong, J.; Soh, H.; Cassell, A.; Quate, C. F.; Dai, H. *Nature* **1998**, *395*, 878.
(12) Franklin, N. R.; Wang, Q.; Tombler, T. W.; Javey, A.; Shim, M.; Dai, H. *Appl. Phys. Lett.*, in press.
(13) Li, Y.; Kim, W.; Zhang, Y.; Rolandi, M.; Wang, D.; Dai, H. *J. Phys. Chem.* **2001**, *105*, 11424−11431.
(14) Collins, P. G.; Bradley, K.; Ishigami, M.; Zettl, A. *Science* **2000**, *287*, 1801−1804.
(15) Chen, R.; Franklin, N.; Kong, J.; Cao, J.; Tombler, T.; Zhang, Y.; Dai, H. *Appl. Phys. Lett.* **2001**, *79*, 6951.
(16) Jhi, S.-H.; Louie, S. G.; Cohen, M. L. *Phys. Rev. Lett.* **2000**, *85*, 1710.
(17) Sedra, A.; Smith, K. *Microelectronic Circuits*; Oxford University Press: New York, 1991.
(18) Rabaey, J. *Digital integrated circuits: a design perspective*; Prentice Hall: Englewood Cliffs, NJ, 1996.
(19) Shim, M.; Javey, A.; Kam, N. W. S.; Dai, H. *J. Am. Chem. Soc.* **2001**, *123*, 11512−11513.
(20) Fuhrer, M. S.; Kim, B. M.; Dürkop, T.; Brintlinger, T. *Nano Lett.* **2002**, *2*, 755.

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