Assessment of High-Frequency Performance Potential of Carbon Nanotube Transistors

Jing Guo, Sayed Hasan, Ali Javey, Gijs Bosman, *Senior Member, IEEE*, and Mark Lundstrom, *Fellow, IEEE*

Abstract—Self-consistent quantum simulations are used to explore the high-frequency performance potential of carbon nantube field-effect transistors (CNTFETs). The cutoff frequency expected for a recently reported CNT Schottky-barrier FET is well below the performance limit, due to the large parasitic capacitance between electrodes. We show that using an array of parallel nanotubes as the transistor channel reduces parasitic capacitance per tube. Increasing tube density gives a large improvement of high-frequency performance when tubes are widely spaced and parasitic capacitance dominates but only a small improvement when the tube spacing is small and intrinsic gate capacitance dominates. Alternatively, using quasi-one-dimensional nanowires as source and drain contacts should significantly reduce parasitic capacitance and improve high-frequency performance. Ballistic CNTFETs should outperform ballistic Si MOSFETs in terms of the high-frequency performance limit because of their larger band-structure-limited velocity.

Index Terms—Carbon nanotubes (CNTs), field-effect transistors (FETs), radio frequency (RF).

I. INTRODUCTION

CARBON NANOTUBEs (CNTs) are being extensively explored for electronic device applications due to their excellent electrical properties. Since the first demonstration of CNT field-effect transistors (CNTFETs) in 1998 [1], [2], significant progress has been achieved in understanding device physics and in improving transistor performance. For example, a CNTFET that outperforms a state-of-the-art Si MOSFET in terms of delay at the same ON–OFF ratio has recently been demonstrated [3]–[5]. Due to near ballistic transport and the high band-structure-limited velocity in CNTs, CNTFETs also promise good potential for radio-frequency (RF) applications. Pioneering ac measurements of CNTFETs demonstrated that the CNT channel can respond to external voltages for a frequency up to 2.6 GHz [6]–[8]. Recently, a characterization of CNTFETs for a frequency of ∼10 GHz was reported [9]. So far, however, high-frequency measurements of CNTFETs have used devices that are far from optimized for high-frequency performance. To explore the potential of CNTFETs for RF applications, it is important to understand what limits high-frequency performance, how to optimize transistor design, and how CNTFETs compare to Si MOSFETs in terms of high-frequency performance.

In this work, we use self-consistent, quasi-static quantum simulations to examine the high-frequency performance potential for a state-of-the-art CNTFET [3]. We show that, although the transistor reported in [3] has been optimized for dc performance and delivers a near-ballistic dc current, its projected high-frequency performance is well below the performance limit due to large parasitic capacitances. Using an array of parallel nanotubes as the transistor channel or nanowires as source and drain contacts would significantly reduce the parasitic capacitance per tube and, thereby, improve high-frequency performance. Due to larger band-structure-limited velocity [10], we find that ballistic CNTFETs would outperform a hypothetical ballistic Si MOSFETs in terms of intrinsic cutoff frequency. The results presented here should prove useful for understanding and optimizing high-frequency characteristics of CNTFETs and assessing the potential of CNTFETs for nanoelectronic RF applications.

II. APPROACH

We performed a detailed numerical simulation to analyze and optimize the high-frequency performance of a recently reported CNTFET [3]. As shown in Fig. 1(a), the transistor was optimized for dc performance by integrating a 50-nm-long channel, a thin high-κ gate insulator, and good metal-nanotube contacts. Integration of good fabrication techniques leads to good dc performance. The measured channel conductance is one-half of the ballistic conductance limit ($4\,q^2/h$), and the measured source–drain current is $\sim 20\ \mu$A at a gate overdrive of $|V_g - V_T| \sim 1.0$ V. Because this transistor is one of the most mature CNTFETs reported to date, we focus our attention on projecting the maximum RF performance of this CNTFET. The qualitative results are general and readily extendible to other CNTFETs.

A self-consistent quantum simulation was developed to simulate dc characteristics of CNTFETs [11]. The open-boundary Schrödinger equation was solved in an atomistic pZ-orbital basis using a nonequilibrium Green's function (NEGF) formalism. The quantum transport solution was solved self-consistently with the Poisson equation. A previously described phenomenological model of the metal-nanotube contacts was used for solving the quantum transport equation [11]. In brief, each mode in the semiconducting CNT channel is coupled to a metallic mode in the contact with two input parameters. The first parameter is the Schottky barrier height, which describes the band discontinuity. The second one is the coupling strength,

J. Guo and G. Bosman are with the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611 USA (e-mail: guoj@ufl.edu).

S. Hasan and M. Lundstrom are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA.

A. Javey is with the Society of Fellows, Harvard University, Cambridge, MA 02138 USA.
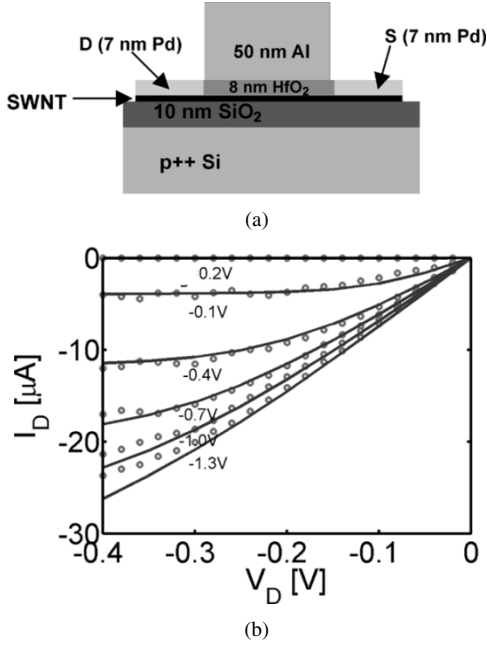
(a)

(b)

Fig. 1. (a) Recently reported high-performance CNTFET with the device parameters described in the text and (b) its $I_D - V_D$ characteristics at different gate voltages as denoted in the figure The lines are simulation results, and the circles are experiment measurements.

Fig. 2. Small-signal equivalent circuit model for a CNTFET. g_m is the transconductance, C_g is the intrinsic gate capacitance, and g_d is the channel conductance. The dashed rectangle shows the equivalent circuit of the intrinsic CNTFET. The parasitic capacitance $C_{\mathrm{ps}}(C_{\mathrm{pd}})$ between the gate and source (drain) electrode is obtained by a separate electrostatic calculation. $R_{\mathrm{ps}}(R_{\mathrm{pd}})$ is the parasitic source (drain) resistance.

which controls the density of metal-induced gap states (MIGS). Due to the lack of dangling bonds on the CNT surface, bonding between the CNT and the oxide is much weaker than the covalent bonds between the carbon atoms in the CNT. The effect of the oxide on the carrier transport properties of the CNT channel is omitted.

Ballistic transport in the CNT channel is assumed. (The effect of scattering will be briefly discussed in Section IV.) After simulating the I–V characteristics of the intrinsic CNTFET, the parasitic source (drain) resistance due to the thin Pd source (drain) film was added to obtain the extrinsic I–V characteristics [12]. Fig. 1(b), which plots the measured and simulated $I_D - V_D$ characteristics at different gate voltages, shows that the simulated I–V characteristics agree well with the measurement. The parameters used in the simulation were obtained from separate electrical characterization [3]. The CNT diameter is $d_{\mathrm{CNT}} \sim 1.7$ nm with a band gap $E_g \sim 0.50$ eV. The thickness of the HfO$_2$ top gate insulator is 8 nm. The Pd source (drain) is 7 nm thick and 8 μm wide. The gate electrode thickness is about 50 nm. The length of the gate, which self-aligns with the CNT channel, is $\sim$50 nm. A $\sim$4-nm-thick native oxide layer around the Al gate is omitted for simplicity. (The major effect of the $\sim$4-nm-thick native oxide is to decrease the parasitic capacitance between the gate and the source (drain) electrode by a factor of $\sim$2, which does not change the qualitative conclusions of the paper.) The threshold voltage of the transistor was treated as a fitting parameter, which accounts for the uncertainty of the work function for the gate electrode and the CNT channel and possible existence of oxide charge [4]. The results show that our understanding of carrier transport, transistor electrostatics, metal/tube contacts, and oxide/tube interface has matured to a point that the measured dc I–V characteristics are well described by theory.
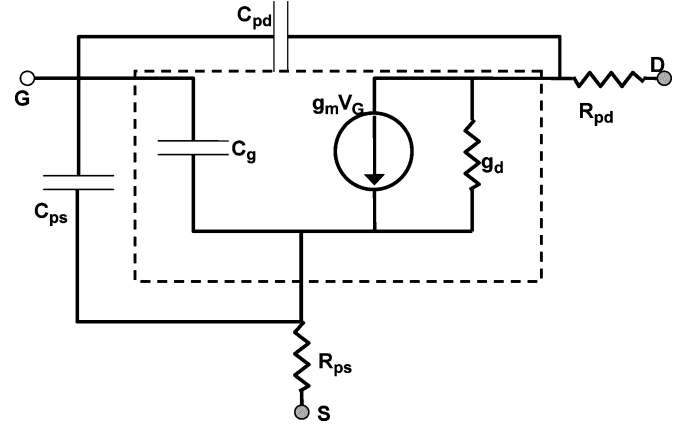
The dc simulations were used to investigate how many subbands deliver the current for the CNTFET in Fig. 1(a). The simulation results showed that, within the measured bias range (-1.3 V $< V_G < 0.5$ V at $V_D = 0.4$ V), over 90% of the total source–drain current is delivered by the first subband. The reason is that, for a CNTFET with an intrinsic channel, the current is controlled by tunneling through the Schottky barriers (SBs) at the metal/CNT interface. The CNT channel has a diameter of $\sim$1.7 nm, which results in a relatively large subband spacing ($\sim$0.25 eV). As a result, the Schottky barrier for the second subband is much higher than that for the first subband. Because the tunneling current exponentially decreases with the barrier height, the conduction through the lowest subband dominates [4].

A quasi-static treatment was used to assess high-frequency performance of CNTFETs. (The validity of the quasi-static treatment will be briefly discussed in Section IV.) We numerically extracted an equivalent small-signal model [13], [14] as shown in Fig. 2. The parameters of the equivalent circuit model for the intrinsic CNTFET, which is shown within the dashed rectangle in Fig. 2, are obtained by running self-consistent quantum simulations and numerically evaluating the derivatives. The intrinsic gate capacitance C_g and the transconductance g_m are

$$C_g = \left.\frac{\partial Q_{\mathrm{ch}}}{\partial V_g}\right|_{V_d}$$
$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d} \tag{1}$$

where Q_{ch} is the total charge in the CNT channel and I_d is the source–drain current. The source–drain conductance $g_D = \partial I_d/\partial V_d|_{V_g}$ is obtained by running dc simulations with slightly different $V_d (\Delta V_d = 10$ mV). The model describes the small-signal I–V characteristics of the intrinsic transistor by keeping the linear terms of the Taylor expansion for the source–drain current

$$dI_D \approx \frac{\partial I_D}{\partial V_D}dV_D + \frac{\partial I_D}{\partial V_G}dV_G = g_d dV_D + g_m dV_G \tag{2}$$

which indicates that the transconductance is in parallel with the channel conductance in the equivalent circuit. At low $|V_D|$ (linear region), $1/g_d$ accounts for the channel resistance, which includes the quantum resistance of a ballistic channel. At high $|V_D|$, $I_D - V_D$ characteristics are close to saturation, and g_d is small.

Additional elements are added to the equivalent circuit to take parasitic capacitances and resistances into account. The parasitic capacitance between the gate and source (drain) electrode $C_{ps}(C_{pd})$ is computed by a separate electrostatic calculation [15], because the size of the contacts can be much larger than the size of the CNT channel. Because the parasitic capacitances between the metal gate electrode and the metal source and drain electrode are nearly bias-independent, they can be treated as constant electrostatic capacitances. The parasitic resistance $R_{ps}(R_{pd}) \sim 1.7 \, \text{K}\Omega$ was obtained from the experiment [3]. The relatively large parasitic resistance is due to ultrathin metal films (~ 7 nm thick) used in the experiment. The model in Fig. 2 is similar to what was proposed by Burke [14], but $R_{ps}(R_{pd})$ is the parasitic resistance of the metal contacts, rather than quantum resistance of a ballistic tube and is not equal to $h/8q^2 \sim 3 \, \text{K}\Omega$.

The bottom oxide of this CNTFET (see Fig. 1) is relatively thin (~ 10 nm), which degrades the projected high-frequency performance because it results in additional parasitic capacitance between the bottom electrode and other electrodes, but a thicker bottom oxide, which would essentially eliminate the parasitic capacitance of the bottom electrode, can be readily fabricated in practice [16]. Therefore, we omit the parasitic capacitance between the bottom electrode and other electrodes. We use the cutoff frequency (the frequency at which the current gain is 1) to describe high-frequency performance of a transistor. For a CNTFET with an equivalent circuit in Fig. 2, the cutoff frequency is [17]

$$f_T \approx \frac{1}{2\pi} \frac{g_m}{C_g + C_{pS} + C_{pD}}. \tag{3}$$

The cutoff frequency of the intrinsic transistor without parasitic capacitance is

$$f_T \approx \frac{1}{2\pi} \frac{g_m}{C_g}. \tag{4}$$

A more accurate equivalent circuit model requires partitioning the intrinsic gate capacitance C_g to a capacitance between the gate and the source and a capacitance between the gate and the drain, but the partitioning has no effect on the transistor cutoff frequency [17].

III. RESULTS

We first examine RF performance potential of the CNTFET reported in [3] (see Fig. 1) by extracting values for the equivalent circuit parameters in Fig. 2 at on-state ($V_G = V_D = -0.4$ V). An intrinsic gate capacitance of $C_g \approx 2.29$ aF and a transconductance of $g_m \approx 26 \, \mu\text{S}$ are extracted. The extracted output conductance at the on-state is $g_d \approx 4.7 \, \mu\text{S} \approx 1/210 \, \text{K}\Omega$.

The parasitic capacitance per unit width between the gate and the source (drain) electrode C_w is computed by solving a
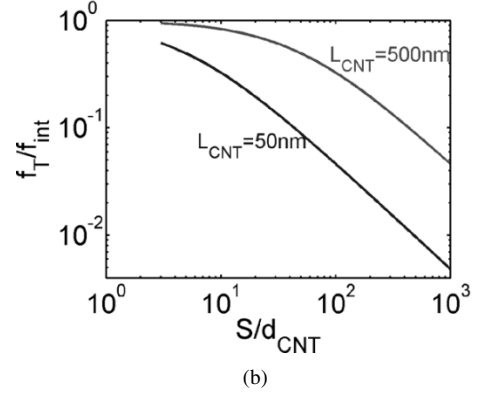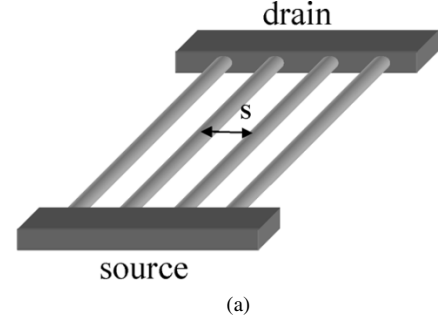

Fig. 3. (a) Carbon nanotube array as the transistor channel between the source and drain. (b) Simulated cutoff frequency (normalized by the intrinsic cutoff frequency) versus the tube spacing (normalized by the tube diameter) for the tube lengths $L_{CNT} = 500$ nm and $L_{CNT} = 50$ nm.

two–dimensional (2-D) Laplace equation for the experimental geometry as shown in Fig. 1(a) [12]. The thickness of the Pd source (drain) film is 7 nm, the HfO_2 gate insulator thickness is 8 nm, the Al top gate, which self aligns with the source and drain electrodes, is 50 nm thick. The parasitic capacitance per unit width is $C_w \approx 0.15 \, \text{fF}/\mu\text{m}$ and for the source (drain) contact with the width $W = 8 \, \mu\text{m}$, the parasitic capacitance is $C_{ps} = C_{pd} = C_w W \approx 1.23$ fF. After extracting parameters for an equivalent circuit, the cutoff frequencies of the CNTFET can be computed. At the on-state ($V_G = V_D = -0.4$ V), the projected cutoff frequency of the extrinsic experimental CNTFET is $f_T \approx (1/2\pi)g_m/C_g + 2C_w W \approx 1.7$ GHz, and the projected cutoff frequency of the intrinsic CNTFET is $f_{int} \approx (1/2\pi)g_m/C_g \approx 1.8$ THz. Because the electrode width ($\sim 8 \, \mu\text{m}$) is much larger than the tube diameter ($d_{CNT} \sim 1.7$ nm), and the parasitic capacitance is three orders of magnitude larger than the intrinsic gate capacitance, the projected f_T of the experimental FET is well below its performance limit. In order to improve high-frequency performance of the CNTFET, it is important to reduce parasitic capacitance per tube.

One approach to reduce parasitic capacitance per tube is to use a parallel array of nanotubes as the transistor channel, as shown in Fig. 3(a). If the source (drain) contact width is fixed at W, increasing N, the number of tubes in the array, increases the total channel transconductance to Ng_m and intrinsic gate capacitance to NC_g, where g_m is the transconductance per tube, and C_g is the intrinsic gate capacitance per tube. The cutoff frequency of a CNT array FET is

$$f_T \approx \frac{1}{2\pi} \frac{Ng_m}{NC_g + 2C_w W} = \frac{1}{2\pi} \frac{g_m}{C_g + 2C_w S} \tag{5}$$

where $S = W/N$ is the spacing between neighboring tubes in a uniform array of tubes. Equation (5) can also be interpreted as that, for a tube array FET, each tube in the channel drives an equivalent parasitic capacitance of $2C_wS$.

Fig. 3(b) plots the cutoff frequency of a tube array FET (normalized by its intrinsic cutoff frequency) versus the tube spacing (normalized by the tube diameter). When the tube spacing is large, parasitic capacitance is much larger than the intrinsic gate capacitance, and $f_T \approx g_m/(2\pi C_W S)$. Reducing the tube spacing reduces parasitic capacitance per tube and leads to an increase of f_T. In contrast, when the tube spacing is small, the intrinsic gate capacitance per tube, C_g, is larger than the parasitic capacitance per tube, $2C_wS$, and dominates. When the tube spacing is small, the projected, extrinsic cutoff frequency f_T approaches the intrinsic cutoff frequency $f_{\text{int}} \approx g_m/(2\pi C_g)$. Fig. 3(b) also shows that, for a longer channel, the intrinsic capacitance begins to dominate at larger tube spacing because C_g is larger. (Electrostatic coupling between neighboring tubes, which reduces the intrinsic gate capacitance per tube when the tube array is very dense [18], is omitted because the examined tube spacing $S > 3d_{\text{CNT}}$.) In practice, lack of control on the tube position and orientation may result in cross contacts between neighboring tubes. This could result in charge transfer and potential barriers at the connection points, which would lower carrier velocity and high-frequency performance.

It is important to notice that the parasitic capacitances are dominant here because micrometer-scale contacts are used. Significant performance improvements could be achieved if a nanometer-scale source (drain) contact can be used [14]. Next, we examine how much performance improvement can be achieved if a quasi-one-dimensional metallic wire can be integrated as the source (drain) contact. The examined transistor geometry is the same as the CNTFET in Fig. 1(a), except that metallic nanowire source and drain contacts with the same radius as the CNT channel are used.

To assess high-frequency performance, the values of the parasitic capacitance between the gate electrode and the nanowire source (drain) contact, $C_{\text{pS}} = C_{pD} \approx 1.4$ aF is computed by a separate electrostatic simulation using the method of moments [19]. Compared to the micrometer-scale source and drain contacts used in the experiment [3], the parasitic capacitance can be reduced by three orders of magnitude if quasi-one-dimensional contacts can be achieved. (Another effect of using quasi-one-dimensional metal contacts is that the Schottky barrier thickness is reduced due to a shorter electrostatic screening length [20], which leads to simultaneous increase of g_m and C_g. The effect is relatively small when the top gate insulator is already thin and is therefore omitted for simplicity.) The extrinsic cutoff frequency is $f_T \approx (1/2\pi)(g_m/(C_g + C_{\text{ps}} + C_{\text{pd}})) \approx 810$ GHz. Compared to the projected cutoff frequency of the CNTFET with micrometer-scale contacts ($\sim$1.7 GHz), the improvement is significant if a nanoscale metal source (drain) contact can be successfully integrated with the CNT channel. (Recently reported CNTFETs with heavily doped CNT segments as source and drain extensions operate as MOSFETs with quasi-one-dimensional source and drain contacts [21], [22]; their high-frequency performance will be assessed in a separate paper.)
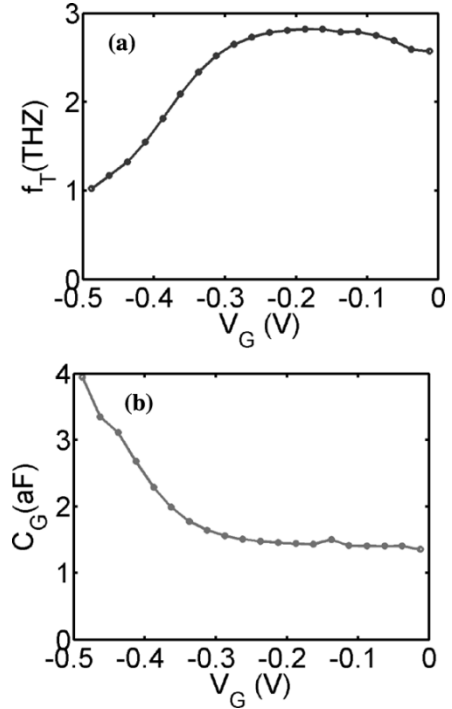

Fig. 4. (a) Simulated intrinsic cutoff frequency and (b) simulated intrinsic gate capacitance versus the gate voltage for the ballistic CNT SBFET.
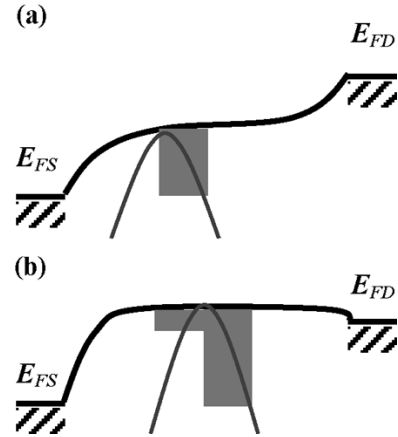

Fig. 5. Sketch of valence band profile at (a) a low gate overdrive and (b) a high gate overdrive for a ballistic CNT SBFET. The $+k$ states are occupied according to E_{FS} and the $-k$ states are occupied according to E_{FD}.

When the intrinsic gate capacitance dominates, the projected cutoff frequency f_T approaches the intrinsic cutoff frequency determined by g_m and C_g. Next, we explore how intrinsic cutoff frequencies of ballistic CNTFETs vary with the gate voltage. Fig. 4(a) shows that the intrinsic cutoff frequency of the CNT Schottky barrier (SB) FET drops significantly when $|V_g - V_t|$ is large. Fig. 4(b), which plots the intrinsic gate capacitance versus the gate voltage at $V_D = -0.4$ V indicates that the drop of the cutoff frequency is due to the increase of the intrinsic gate capacitance at large $|V_g - V_t|$. In order to understand why the gate capacitance increases at large gate overdrives, we sketched the band diagrams at a low gate overdrive and a high gate overdrive for a ballistic CNT SBFET, as shown Fig. 5(a) and (b), respectively. At low gate overdrives, only $+k$ states in the channel
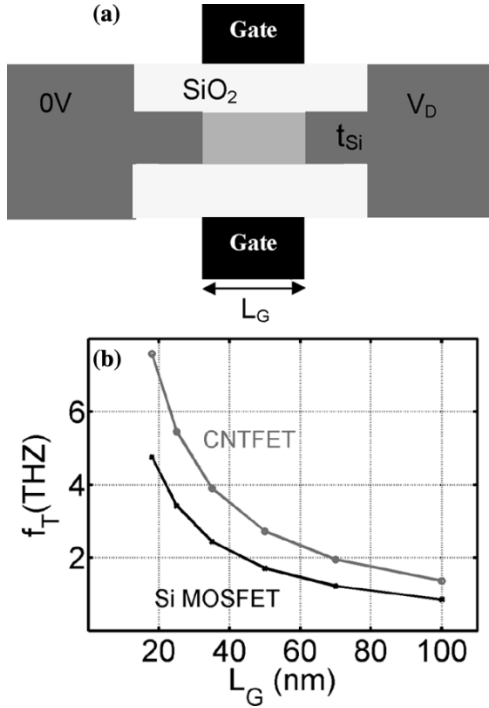
Fig. 6. (a) Modeled double-gate ultrathin-body Si MOSFET. (b) Intrinsic cutoff frequencies for the CNT SBFET and Si MOSFET versus the channel length. The CNTFET outperforms the Si MOSFET due to larger band-structure-limited velocity.

are occupied and contribute to the intrinsic gate capacitance. In contrast, at high gate overdrives, the first subband edge in the channel is below the drain Fermi level. Both $+k$ and $-k$ states are occupied and contribute to the channel capacitance. As a result, the channel capacitance significantly increases when the Van Hove singularity [23] of $-k$ states begins to be charged, and the cutoff frequency reduces.

Finally, we compare the high-frequency performance limit of a CNTFET to that of a hypothetical ballistic Si MOSFET. Fig. 6(a) shows the modeled double-gate, ultrathin-body Si MOSFET [24]. The transistor is biased at $V_G = V_D = 0.4$ V with an on-current of $\sim 1300 \ \mu A/\mu m$ and simulated using a self-consistent quantum simulation as described in [24]. (The intrinsic cutoff frequency of the examined n-type Si MOSFET remains approximately constant for $V_t < V_G < 0.4$ V.) Similar performance is expected from n-type and p-type CNTFETs with similar metal–CNT contacts due to symmetric conduction and valence band structures. The intrinsic cutoff frequency of the examined p-type CNT SBFET drops for $|V_G - V_t| > 0.3$ V, as shown in Fig. 4(a). The high-frequency performance is therefore assessed at $V_G = -0.3$ V and $V_D = -0.4$ V. Because the intrinsic cutoff frequency of a ballistic transistor is essentially determined by the band-structure-limited velocity, comparing the intrinsic cutoff frequency of transistors based on different channel materials is essentially comparing the band-structure-limited velocities. Fig. 6(b), which plots the projected intrinsic cutoff frequencies for the ballistic CNT SBFET and the ballistic Si MOSFET versus the transistor channel length, shows that the cutoff frequency of the CNTFET is ~50% higher than that of the Si MOSFET at the same channel length, due to larger band-structure-limited velocity in CNTs. Although we

used a ballistic double-gate Si MOSFET in the comparison, similar results apply to ballistic single-gate Si MOSFETs.

IV. DISCUSSION

A quasi-static approximation was used to assess high-frequency performance of the transistors. We first discuss the validity of quasi-static approximation. A rigorous treatment beyond quasi-static approximation requires inclusion of capacitive, resistive, and inductive elements for an equivalent circuit model. The quasi-static approximation includes the equivalent capacitive and resistive elements, but omits the equivalent inductive elements. In order to assess how good the quasi-static approximation is, the inductance of the CNT channel needs to be estimated. The quasi-static treatment works well when the signal varies slowly compared to the time constant determined by the intrinsic gate capacitance and the channel inductance. For a ballistic CNTFET as shown in Fig. 1(a), the kinetic inductance is several orders of magnitude larger than the magnetic inductance [25]. The total channel inductance is approximately the kinetic inductance, $L_k = (1/4) \int_0^{L_{ch}} h/q^2 v(x) dx$, where h is Planck's constant, $v(x)$ is the carrier velocity at the source Fermi level as a function of the channel position, and the factor of 1/4 is due to the valley degeneracy of 2 and spin degeneracy of 2 in a CNT. By making the approximation, $v(x) \approx v_F$, the kinetic inductance is estimated as

$$L_k = \frac{1}{4} \int_0^{L_{ch}} dx \frac{h}{q^2 v(x)} \approx \frac{h L_{ch}}{4 q^2 v_F} \approx 0.20 \text{ nH}. \qquad (6)$$

In order to assess how good the quasi-static approximation is, we computed a channel LC frequency as $f_{LC} \approx 1/(2\pi \sqrt{L_k C_g}) \approx 5.2$ THz for the ballistic CNT SBFET. The LC frequency is much larger than the extrinsic cutoff frequency of the CNT SBFET, which indicates that quasi-static approximation works well for the extrinsic cutoff frequency. It is larger than but at the same order of magnitude as the intrinsic cutoff frequency of the CNT SBFET, which indicates that kinetic inductance may begin to play a role when the intrinsic cutoff frequency is assessed.

We have assumed ballistic transport in CNTs. A previous study showed that the experimental CNTFET delivers a near-ballistic dc current for the following reason [26]. The dominant scattering mechanism in an intrinsic CNT is phonon scattering. Acoustic phonon scattering has a mean free path much longer than the channel length. Therefore, it is not important for a 50-nm CNTFET. Although optical phonon scattering has a short mean free path (~10 nm) and scatters holes even in a short-channel CNTFET, after emitting an optical phonon with an energy of $\hbar\omega_{OP} \sim 0.16$ eV, carriers lose a large energy and cannot overcome the potential energy barrier in the channel to return back to source. The CNTFET, therefore, delivers a near ballistic dc current [26]. Because phonon scattering only has a small effect on dc I–V characteristics, the transconductance remains approximately the same after phonon scattering is included. In contrast, phonon scattering changes charge density in the channel and the intrinsic gate capacitance. As a result, when the parasitic capacitance dominates (for assessing

extrinsic cutoff frequency), phonon scattering in the channel only has a small effect. When the intrinsic cutoff frequency is assessed, phonon scattering, however, decreases the intrinsic cutoff frequency. The reason is that optical phonon scattering results in random walk of carriers in the channel and degrades the carrier velocity.

V. CONCLUSION

We performed a detailed study to assess the high-frequency performance potential of CNT SBFETs using quasi-static, self-consistent quantum simulations. For state-of-the-art CNTFET structures optimized for dc performance, the high-frequency performance is far from optimized. Using a parallel tube array as the transistor channel reduces the parasitic capacitance per tube. Increasing tube density results in large improvement of the extrinsic cutoff frequency when the tube array is sparse, and the parasitic capacitance dominates, but smaller improvement when the tube array is dense, and the extrinsic cutoff frequency approaches the intrinsic cutoff frequency. Alternatively, using nanometer-scale contacts rather than micrometer-scale contacts significantly reduces parasitic capacitance and improves high-frequency performance. A ballistic CNTFET would outperform a ballistic Si MOSFETs in terms of the intrinsic cutoff frequency due to larger band-structure-limited velocity. The study should be useful for understanding and optimizing high-frequency performance of CNTFETs and assessing the potential of CNTFETs for RF applications.

ACKNOWLEDGMENT

REFERENCES

[1] S. J. Tans, A. R. M. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature*, vol. 393, pp. 49–52, 1998.

[2] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 73, pp. 2447–2449, 1998.

[3] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, and H. J. Dai, "Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays," *Nano Lett.*, vol. 4, pp. 1319–1322, 2004.

[4] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nantoube field-effect transistors," in *IEDM Tech. Dig.*, San Francisco, CA, 2004, pp. 703–706.

[5] R. V. Seidel, A. P. Graham, J. Kretz, B. Rajasekharan, G. S. Duesberg, M. Liebau, E. Unger, F. Kreupl, and W. Hoenlein, "Sub-20 nm short channel carbon nanotube transistors," *Nano Lett.*, vol. 5, pp. 147–150, 2005.

[6] J. Appenzeller and D. J. Frank, "Frequency dependent characterization of transport properties in carbon nanotube transistors," *Appl. Phys. Lett.*, vol. 84, pp. 1771–1773, 2004.

[7] D. J. Frank and J. Appenzeller, "High-frequency response in carbon nanotube field-effect transistors," *IEEE Electron Device Lett.*, vol. 25, no. 1, pp. 34–36, Jan. 2004.

[8] S. D. Li, Z. Yu, S. F. Yen, W. C. Tang, and P. J. Burke, "Carbon nanotube transistor operation at 2.6 GHz," *Nano Lett.*, vol. 4, pp. 753–756, 2004.

[9] X. Huo, M. Zhang, P. C. H. Chan, Q. Liang, and Z. K. Tang, "High-frequency S parameters characterization of back-gate carbon nantoube field-effect transistors," in *IEDM Tech. Dig.*, San Francisco, CA, 2004, pp. 691–694.

[10] J. Guo, M. Lundstrom, and S. Datta, "Performance projections for ballistic carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 80, pp. 3192–3194, 2002.

[11] J. Guo, S. Datta, M. Lundstrom, and M. P. Anantram, "Toward multi-scale modeling of carbon nanotube transistors," *Int. J. Multiscale Comput. Eng.*, vol. 2, pp. 257–277, 2004.

[12] Y. Taur and T. Ning, *Fundamentals of Modern VLSI Devices*. London, U.K.: Cambridge Univ. Press, 1998.

[13] L. C. Castro, D. L. John, D. L. Pulfrey, M. Pourfath, A. Gehring, and H. Kosina, "Method for predicting f_T for carbon nanotube FETs," *IEEE Trans. Nanotechnol.*, vol. 4, no. 6, pp. 699–704, Nov. 2005.

[14] P. J. Burke, "AC performance of nanoelectronics: toward a ballistic THz nanotube transistor," *Solid-State Electron.*, vol. 48, pp. 1981–1986, 2004.

[15] K. Nabors and J. White, "Fastcap—a multipole accelerated 3-D capacitance extraction program," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 10, pp. 1447–1459, 1991.

[16] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, pp. 654–657, 2003.

[17] W. Liu, *Fundamentals of III-V Devices: HBT's, MESFET's, and HEMTs*. New York: Wiley, 1999.

[18] J. Guo, S. Goasguen, M. Lundstrom, and S. Datta, "Metal-insulator-semiconductor electrostatics of carbon nanotubes," *Appl. Phys. Lett.*, vol. 81, pp. 1486–1488, 2002.

[19] S. Ramo, J. R. Whinnery, and T. Van Duzer, *Fields and Waves in Communication Electronics*, 3rd ed. New York: Wiley, 1993.

[20] J. Guo, J. Wang, E. Polizzi, S. Datta, and M. Lundstrom, "Electrostatics of nanowire transistors," *IEEE Trans. Nanotechnol.*, vol. 2, no. 4, pp. 329–334, Dec. 2003.

[21] A. Javey, R. Tu, D. B. Farmer, J. Guo, R. G. Gordon, and H. J. Dai, "High performance n-type carbon nanotube field-effect transistors with chemically doped contacts," *Nano Lett.*, vol. 5, pp. 345–348, 2005.

[22] J. Chen, C. Klinke, A. Afzali, and P. Avouris, "Self-aligned carbon nanotube transistors with charge transfer doping," *Appl. Phys. Lett.*, vol. 86, 2005.

[23] R. Saito, G. Dresselhaus, and M. S. Dresselhaus, *Physical Properties of Carbon Nanotubes*. London, U.K.: Imperial College Press, 1998.

[24] Z. Ren, R. Venugopal, S. Goasguen, S. Datta, and M. Lundstrom, "NanoMOS2.5: A two-dimensional simulator for quantum transport in dourble-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1914–1925, Sep. 2003.

[25] P. J. Burke, "Luttinger liquid theory as a model of the gigahertz electrical properties of carbon nanotubes," *IEEE Trans. Nanotechnol.*, vol. 1, no. 3, pp. 129–144, Sep. 2002.

[26] J. Guo and M. Lundstrom, "Role of phonon scattering in carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 86, p. 193 103, 2005.
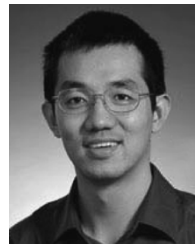
Jing Guo received the B.S. degree in electronic engineering and the M. S. degree in microelectronics and solid state electronics from Shanghai Jiao Tong University, Shanghai, China, in 1998 and 2000, respectively, and the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, in 2004.

He is currently an Assistant Professor of electrical engineering with the University of Florida, Gainesville. His current research work centers on modeling and simulation of carbon nanotube electronic and optoelectronic devices. He has previously worked on simulation of silicon nanotransistors and single-electron transistors.

Sayed Hasan received the B.Sc. degree in electrical and electronic engineering (with first-class honors) from Bangladesh University of Engineering and Technology (BUET), in 1998. He is currently working toward the Ph.D. degree in electrical and computer engineering at Purdue University, West Lafayette, IN.

He has worked on identifying design challenges of 10-nm scale MOSFETs, for which he used the nonequilibrium Green's function formalism. His current research topic concerns electron phonon interaction in carbon nanotubes and silicon nanowire-based transistors using semiclassical electron and phonon transport. For this, he uses a self-consistent Monte Carlo simulation.

Ali Javey received the B.S. degree in chemistry from Old Dominion University, Norfolk, VA, in 2001, and the Ph.D. degree in physical chemistry from Stanford University, Stanford, CA, in 2005.

He is currently a Junior Fellow with the Society of Fellows, Harvard University, Cambridge, MA. His research interests include electron transport spectroscopy, device physics, and hierarchical assembly of novel nanostructures, including one-dimensional nanotubes and nanowires.

Gijs Bosman (M'82–SM'89) received the B.S., M.S., and Ph.D. degrees in physics from the University of Utrecht, Utrecht, The Netherlands in 1971, 1976, and 1981, respectively.

In 1981, he joined the Department of Electrical and Computer Engineering, University of Florida, Gainesville, where he is currently a Professor. His research interests include the electrical noise and charge transport properties of semiconductor devices and circuits. He has published more than 100 refereed journal and conference papers on these topics.

Dr. Bosman is a member of the American and Dutch Physical Societies. In the fall of 2001, he was the general chair and host of the Sixteenth International Conference on Noise in Physical Systems and 1/f Fluctuations, held in Gainesville, FL. In addition to the College of Engineering Teacher of the Year Award for 1998–1999, he was the recipient of several university and departmental awards for teaching and research.

Mark Lundstrom (S'72–M'74–SM'80–F'94) received the B.E.E. and M.S.E.E. degrees from the University of Minnesota, Minneapolis, in 1973 and 1974, respectively.

He is the Scifres Distinguished Professor of Electrical and Computer Engineering at Purdue University, West Lafayette, IN, where he also directs the National Science Foundation Network for Computational Nanotechnology. He joined the Purdue faculty upon completing his doctorate on the West Lafayette campus in 1980. Before attending Purdue, he was with the Hewlett-Packard Corporation, where he was involved with integrated circuit process development and manufacturing. His current research interests center on the physics of semiconductor devices, especially nanoscale transistors. His previous work includes studies of heterostructure devices, solar cells, heterojunction bipolar transistors, and semiconductor lasers. During the course of his Purdue career, he has served as Director of the Optoelectronics Research Center and Assistant Dean of the Schools of Engineering.

Prof. Lundstrom is a Fellow of the American Physical Society and the recipient of several awards for teaching and research—most recently, the 2002 IEEE Cledo Brunetti Award and the 2002 Semiconductor Research Corporation Technical Achievement Award for his work with his colleague, S. Datta, on nanoscale electronics.