Quantum Well InAs/AlSb/GaSb Vertical Tunnel FET With HSQ Mechanical Support

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***Abstract*—A type-III (broken gap) band alignment heterojunction vertical in-line InAs/AlSb/GaSb tunnel FET, including a 2-nm-thin AlSb tunneling barrier is demonstrated. The impact of overlap and underlap gate is studied experimentally and supported further by quasi-stationary 2-D TCAD Sentaurus device simulations. Hydrogen silsesquioxane is used as a novel mechanical support structure to suspend the 10-nm-thin InAs drain with enough undercut to be able to demonstrate an overlap gate architecture. The overlap gate InAs/AlSb/GaSb TFET shows an ON current density of 22 μA/μm^2 at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 0.4$ V and the subthreshold slope is 194 mV/decade at room temperature and 46 mV/decade at 100 K.**

***Index Terms*—Heterojunction, nanofabrication, TCAD simulation, tunneling barrier, type III (broken gap) band alignment, vertical in-line tunnel FET.**

I. Introduction

Tunnel field effect transistors (TFETs) have been extensively explored for their potential as promising candidates for ultra-low power, low voltage nanoelectronic applications [1]–[13]. III–V materials, due to their small effective masses, promise a high tunneling probability and therefore, a high ON current [14]. In addition, the large variety of band alignments offered by III–V materials provides an opportunity to design a heterojunction with a small energy offset between the valence band on one side of the junction and the conduction band on the other side of the junction [15]. The overlap of the two bands, and thus the ON current of the transistor can be tuned by applying a voltage to a nearby gate electrode. InAs/GaSb is one material system that offers a type III (broken gap) band alignment and can provide high ON current TFETs [16].

A previous simulation work on III–V vertical in-line TFETs has highlighted the impact of the drain (InGaAs) layer thickness in the undercut access region [17] and the device geometrical design, including the gate length and gate undercut [11], [18]. For this general device architecture, the most promising configuration to operate in ultra-low voltage regime, and to be able to obtain a high ON current, is a type III band alignment. The III–V vertical TFETs with this configuration reported in the literature [8], [9], [17]–[19] do not have an ultra-thin tunneling barrier. As a result, the conduction and valence band edges at the tunneling junction are pinned, resulting in a fixed band offset that cannot be modulated by the gate.

In this paper, we report a platform to fabricate an overlap gate InAs/AlSb/GaSb vertical in-line TFET. This is the first III–V broken gap band alignment heterojunction TFET with a 2 nm thin AlSb tunneling barrier. HSQ layer was used to support a thin InAs layer together with the drain electrode of the tunnel FET. Without the HSQ layer, the InAs layer would bend or collapse during further processing.

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II. Nanofabrication of Overlap and Underlap Quantum Well InAs/AlSb/GaSb Vertical TFETs

A. The InAs/AlSb/GaSb Epitaxial Substrate Platform for a Type III Band Alignment

Fig. 1 depicts the device fabrication process. The initial 50 mm epitaxial substrate wafer includes 10 nm thin n-type InAs layer (Si doped), 2 nm un-doped AlSb layer, 3 nm un-doped GaSb layer and 50 nm p$^+$ GaSb layer (C doped, 1×10^{19} cm^{-3}). Two n-type doping levels of 1×10^{17} and 5×10^{18} cm^{-3} were explored for the InAs layer.

The 2 nm thin AlSb, a sandwiched tunneling barrier between the InAs and GaSb layers, would allow the InAs conduction band (ground quantum well energy state) to slide easily up and down in energy relative to the valence band of GaSb and therefore, leading to modulation of electron tunneling under the control of an applied gate voltage. Without the AlSb layer, the energy bands of InAs and GaSb would be fixed relative to their Fermi levels. The 10 nm thin InAs layer is confined between the gate oxide layer and the AlSb layer, forming a quantum well. The 200 nm heavily doped GaSb layer (7×10^{19} cm^{-3}) is designed to be thick enough for the aggressive drain mesa etching. The remaining non-etched GaSb layer serves as the source contact layer. The 90 periods of AlAs/AsSb supperlattice buffer layer functions as the isolation foundation for the devices.

B. Nanofabrication of Overlap and Underlap Gate Devices

MAA/PMMA bilayer resist stack was spin coated and electron beam lithography was used to form T-shape troughs in the resist, exposing the InAs at the bottom of each trough. 10 nm

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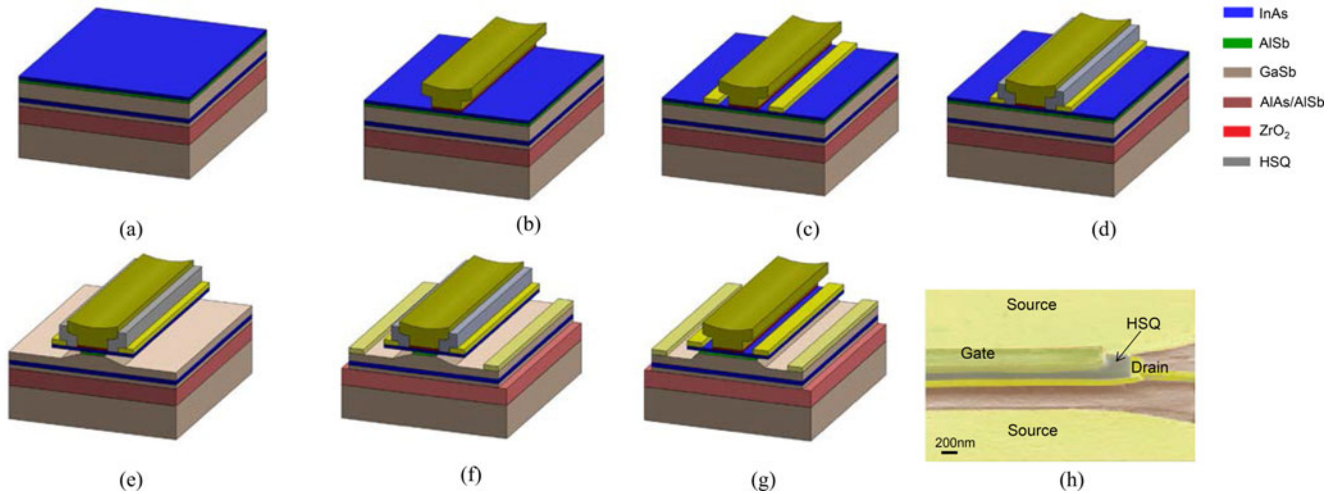

Fig. 1. Fabrication process flow of a HSQ-based overlap gate vertical in-line Tunnel FET: (a) Epitaxial wafer, (b) gate stack formation, (c) drain contact metallization, (d) HSQ support formation, (e) drain mesa formation, (f) source contact metallization and device isolation. (g) The schematic TFET structure without HSQ (e) support and an underlap gate. (h) The SEM side-view of a finalized device, including HSQ.

thick ZrO_2 deposited by atomic layer deposition at 120 °C served as the gate insulator. Ti/Au (20/160 nm) metal gate was deposited by e-beam evaporation. Subsequently, a resist lift-off in acetone resulted in a T-shaped gate electrode (see Fig. 1(b)). Different gate dimensions were explored. The gate widths were 12 or 24 μm, and the gate foot lengths (i.e., length of the bottom of the T-gate, W_G) were 0.64 or 0.80 μm. The T-gate head was 100 nm longer than the foot on each side, as controlled by the thickness of the MAA and the electron beam exposure time. Considering the 100 nm gate overhead shadow, self-aligned drain metal stacks of Ti/Au (5/35 nm) were formed by e-beam evaporation with respect to the T-gate as shown in Fig. 1(c). The self-aligned drain process produces identical separation between the foot of the gate and the drain which keeps the drain resistance same on both sides. Two drain electrodes on the two sides of the gate help to reduce the drain series resistance. The outer edges of the drain electrodes define the opening of the etch window for subsequent vertical and lateral etching of AlSb/GaSb. Therefore, the drain metal widths were designed to vary between 250 and 350 nm in order to obtain devices with different lateral AlSb/GaSb under or over-etch relative to the gate edge. This would allow investigation of the impact of the tunnel junction width (W_J) with respect to the gate width (W_G) on the device performances and therefore the underlap ($W_G < W_J$) and overlap ($W_G > W_J$) gate devices.

HSQ is an electron beam negative resists suitable for high resolution electron beam lithography. Upon e-beam exposure, HSQ gets converted to SiO_x [20] which is not soluble in major typical organic solutions. After the drain metal deposition step, a $\sim$100 nm thick layer of HSQ resist was spun, exposed by electron beam and developed with MF319. Afterward, the mesa junction etch step was performed with wet-etching, as detailed in [21], to form the structure shown in Fig. 1(e). The InAs layer beyond the outer edges of the drain electrodes was removed with a citric acid based hydrogen peroxide solution ($C_6H_8O_7$(s):H_2O:$H_2O_2 = 50$ g:50 mL:10 mL). The AlSb/GaSb stack was etched using a diluted $NH_3.H_2O$ solution (8%), which is highly selective to InAs. Here, HSQ acts as an etch mask, protecting the InAs source/drain extensions from the top side, providing a strong mechanical support to the InAs membrane as well to avoid deformation or collapse while undercutting the AlSb/GaSb underneath. A source contact metal stack of Pd/Ti/Pd/Au (10/20/20/80 nm) was evaporated on top of the heavily doped GaSb layer. Finally, the devices were isolated by etching isolation motes using a H_3PO_4-based solution to form the final overlap gate device depicted in Fig. 1(f).

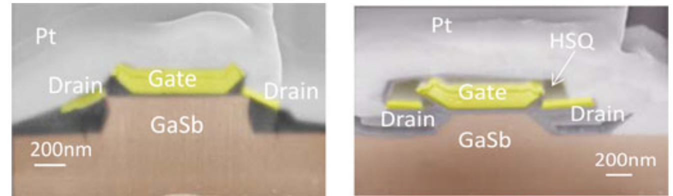

Fig. 2. (a) SEM images of an underlap TFET, without HSQ, after focused ion beam cutting, depicting the collapsed drain metals. (b) SEM image of an overlap TFET, with HSQ, depicting the straight suspended InAs membrane and the drain metals.

The underlap gate device can be fabricated without using HSQ mechanical support, shown in Fig. 1(g). A false-color side-view scanning electron microscopy (SEM) image of a finalized overlap gate device is also shown in Fig. 1(h), depicting the side-view of various device layers. Without the HSQ mechanical support layer, we found it difficult to sufficiently etch the AlSb/GaSb layer beneath the InAs layer to form proper undercut widths. Before the etchant front reaches the gate edge, the InAs cantilever would often bend or collapse as shown in Fig. 2(a). The InAs cantilever is a weak mechanical structure. By incorporating HSQ as the mechanical support layer, we were able to perform enough undercut etching to fabricate overlap gate devices with various junction widths without collapsing or bending InAs layer as shown in Fig. 2(b).

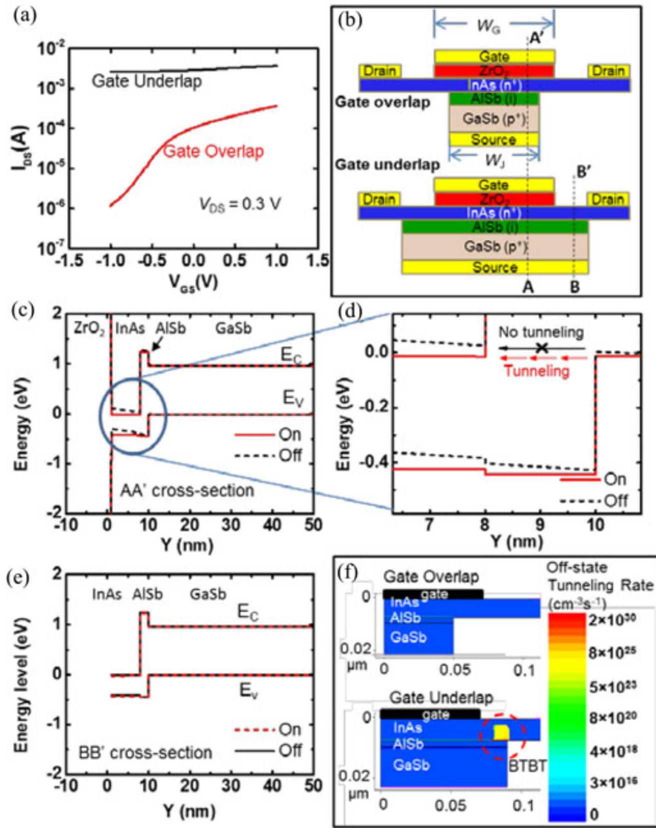

Fig. 3. (a) Transfer characteristics of overlap and underlap vertical tunnel FETs at $V_{\rm DS} = 0.3$ V (T = 300 K). (b) The overlap ($W_{\rm G} > W_{\rm J}$) and underlap ($W_{\rm G} < W_{\rm J}$) vertical in-line TFET configurations. (c) Energy band diagrams at AA' cross-section for both architectures in the ON and OFF states. (d) Zoomed-in energy band diagrams of (c) at the tunnel junction. (e) Energy band diagrams at BB′ cross-section for the on and off states. (f) Tunneling rate comparison for both overlap and underlap device architectures.

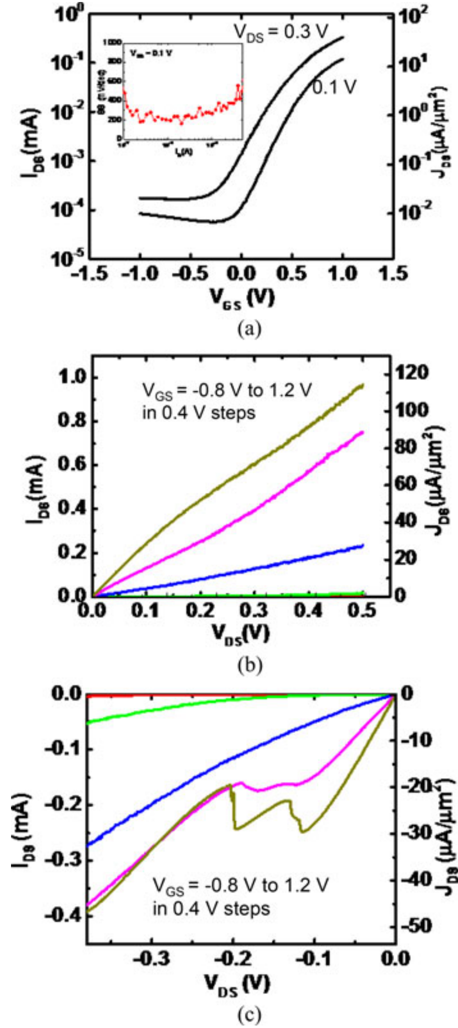

Fig. 4. Room temperature (a) transfer and (b) output characteristics of the representative device in reverse bias regime. (c) Output characteristics under forward bias. The junction area of the device is $0.7 \times 12\,\mu{\rm m}^2$. The inset in (a) depicts the subthreshold slope as a function of $I_{\rm DS}$.

III. The Impact of Underlap and Overlap Gate on the Vertical In-line Tunnel FET Performance

A. Electrical Characterization of Overlap and Underlap Gate Vertical TFETs at 300 K

In order to study the impact of tunneling junction width relative to gate width on the device performance, two devices including HSQ with drain metal widths of 250 and 350 nm were fabricated using a 5×10^{18} cm^{-3} n-type doped InAs layer. The drain mesa etching process (12 min in a diluted $NH_3.H_2O$ solution) yields a lateral AlSb/GaSb etching width of ∼360 nm. The 250 and 350 nm drain metal widths would form a gate overlap (junction with $W_{\rm J} \sim 0.6$ μm, $W_{\rm G} > W_{\rm J}$) and a gate underlap ($W_{\rm J} \sim 0.82$ μm, $W_{\rm G} < W_{\rm J}$) architecture, respectively. The gate foot size is 0.64×24 μm^2 in both devices. Fig. 3(a) shows the transfer characteristics of the two devices at 300 K and $V_{\rm DS} = 0.3$ V. The devices were characterized in a vacuum chamber (pressure is $\sim 1 \times 10^{-5}$ torr) using a prober and a HP 4155C Semiconductor Parameter Analyzer. The overlap gate device shows a much stronger gate dependence than the underlap gate device. The tunneling current in the overlap gate architecture can be fully controlled by the electric field produced by the gate bias. The drain current of the underlap gate device shows a weak dependence on the gate voltage. This device can be considered as an un-gated tunnel diode in parallel to a gated tunnel diode. The majority of the drain current in the subthreshold region would pass via the un-gated diode and therefore, a slight gate voltage dependence can be observed. On the other hand, in the overlap gate device, the tunnel junction is entirely underneath the gate foot area, leading to a strong gate electrostatic control on the device active region. Hence, a much higher $I_{\rm on}/I_{\rm off}$ ratio is observed, assuming the drain current at $V_{\rm GS} = 1$ V as $I_{\rm on}$ and the lowest drain current when the device is at OFF state as $I_{\rm off}$.

B. Two-Dimensional Technology Computer Aided Design (TCAD) Sentaurus Device Simulation of Overlap and Underlap Vertical Tunnel FETs

To study the impact of overlap and underlap gate, quasi-stationary 2-D TCAD Sentaurus device simulation was done to demonstrate the tunneling path of underlap and overlap gate devices [22]. The gate width is set to 70 nm, and the junction widths are 50 and 80 nm for the underlap and the overlap devices,

TABLE I
PERFORMANCE COMPARISON OF PUBLISHED III–V TFETs AT ROOM TEMPERATURE

Reference	I_{on}/I_{off}	I_D or I_D/W	J_D (μA/μm^2)	SS (mV/dec)	V_{GS} (V)	V_{DS} (V)
Nano-wire InAs/InGaAs [25]	10^6	0.27 μA/μm	21.6	79	0.3	0.3
Zhou, IEEE IEDM 2012, InAs/GaSb [8]	10^3	180 μA/μm	14.3	208*	0.5	0.5
Li, IEEE EDL 2012, AlGaSb/InAs [9]	10^3	78 μA/μm	78	138*	0.5	0.5
Bijesh, IEEE IEDM 2013, InGaAs/GaAsSb [10]	10^2	176 μA/μm	315	>500	0.5	0.5
Dey, IEEE EDL 2013, GaSb/InAs [11]	10^2	140 μA/μm	16 000*	320	0.3	0.5
Zhou, IEEE EDL 2012,InGaAs/InP [17]	10^6	2.073 mA	0.74	108*	0.5	0.5
Li, PSSC 2012 InAs/AlGaSb [26]	10^3	12.77 μA/μm	0.51	830	0.5	0.3
Yu, IEEE EDL 2013 $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ [19]	10^2	0.0375 mA	0.449	140	0.5	0.5
$In_{0.53}Ga_{0.47}As$ [6]	10^4	10 μA/μm	0.5*	216	2	0.5
This work	10^3	16 μA/μm	22	194	0.4	0.4
This work	10^3	30 μA/ μm	46.6	298	0.4	0.4

The current density is determined by dividing the drain current to the junction area. SS is the average subthreshold slope over more than one decade of drain current. The current values were taken from the $I_{DS} - V_{DS}$ curves (ON current). Symbol * represents the best estimated value from the publisehd data.

respectively. Nonlocal tunneling model is used to simulate band-to-band tunneling [22], [23]. Drift-diffusion transport model was used for carrier transport [22]. Multi-valley statistics for electrons with non-parabolic model is used in the InAs. The doping levels for InAs layer and GaSb layer are 5×10^{18} and 1×10^{19} cm^{-3}, respectively.

The corresponding energy-band diagrams along AA' and BB' cut lines (as marked in Fig. 3(b) schematics) are shown in Fig. 3(c) and (e) for both ON and OFF states. Along AA' for both devices, switching on or off can be performed by the gate bias. In contrast and along BB', the energy band diagram does not vary significantly by the gate voltage (see Fig. 3(e)).

Fig. 3(f) depicts the band-to-band tunneling rates for the underlap and overlap gate devices in the off state. In the un-gated region, the underlap gate device shows a significantly higher peak tunneling rate ($\sim 1 \times 10^{30}$ cm^{-3}s^{-1}) than the overlap gate device ($\sim 9 \times 10^{15}$ cm^{-3}s^{-1}), resulting a much higher off drain current for the underlap gate device. Hence, an overlap gate is required to achieve a high I_{on}/I_{off} ratio.

IV. ELECTRICAL CHARACTERIZATION OF OVERLAP GATE DEVICE

A. Device Performance at Room Temperature

Fig. 4(a)–(c) represents the *I–V* characteristics of an overlap gate device with a tunnel junction area of 0.7×12 μm^2 ($W_J = 0.7$ μm, $W_G = 0.8$ μm) and a 1×10^{17} cm^{-3} n-type doping in InAs. The device has a subthreshold swing (SS) of 194 mV/decade (Here, we report the average swing to avoid Phantom sub-60mV/decade subthreshold swing arising from measurement issues [24]) at $V_{DS} = 0.1$ V and an $I_{on}/I_{off} > 10^3$. The high SS, likely due to a trap-assisted tunneling mechanism and the interface states. The ON current density is 22 μA/μm^2 at $V_{DS} = 0.4$ V and $V_{GS} = 0.4$ V. Note that there was no significant change in device performance with 1×10^{17} and 5×10^{18} cm^{-3} doping levels in the InAs layer. Fig. 4(c) shows $I_{DS} - V_{DS}$ characteristics of the device at different gate voltages under forward tunnel junction bias. It clearly shows a gate-controlled negative differential resistance behavior, confirming an inter-band tunneling operation. The double peak results from the subbands of the quantized InAs layer, which is sandwiched between the ZrO_2 gate oxide layer and the wide-band gap AlSb layer [21]. Performance comparison of published III–V TFETs is shown in Table I (see Refs. [6], [8]–[11], [17], [19], [25], [26]).

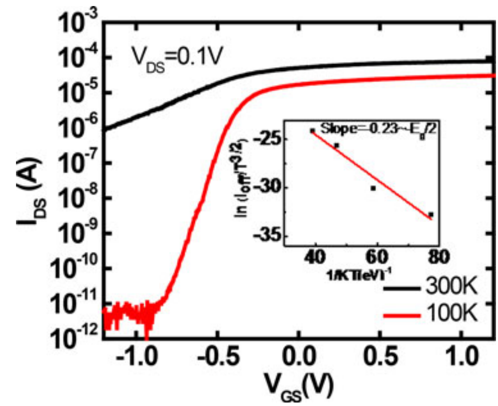

Fig. 5. Transfer characteristics of an overlap gate device at 100 and 300 K, with a tunneling junction area of 0.62×24 μm^2 at $V_{DS} = 0.1$ V.

B. Device Performance at Cryogenic Temperature

The transfer characteristics of an overlap device at two different temperatures (100 and 300 K) are plotted in Fig. 5. The gate foot size was 0.64×24 μm^2 ($W_J = 0.62$ μm). $I_{on}/I_{off}\, of \sim 10^6$ and a SS of 46 mV/decade are observed at 100 K for $V_{DS} = 0.1$ V. The drastic improvement of the subthreshold slope is possibly an indication of a trap-assisted tunneling mechanism in the subthreshold regime [3] and interface states. Low temperature measurement is performed to understand the interface quality, although devices are not expected to operate at cryogenic temperatures in practical systems.

We further measured the off-current at temperatures ranging from 100 to 300 K of a device with 7 nm InAs layer. Activation energy of the off-current was extracted from an Arrhenius plot as shown in Fig. 5(inset) and was found to be ~0.23 eV which corresponds to about half the band gap for a 7 nm InAs layer. The strong gate dependence tends to implicate trap-assisted

tunneling as the likely cause of the large SS in these devices [10]. The defects may be caused by material and interface degradation at the junction edges during the undercut etching process. Further work is required to develop processes to reduce such degradation.

V. Conclusion

In summary, InAs/AlSb/GaSb is demonstrated as the first type III band alignment quantum well vertical in-line TFET, including a 2 nm thin tunneling barrier. HSQ was used as the mechanical support to the 10 nm thin suspended InAs drain cantilever to make overlap gate architectures. The impact of underlap and overlap gates were studied experimentally, and 2-D TCAD device simulations were used to support the experimental observations. The overlap gate device is characterized at 100 and 300 K. At 100 K, $I_{\rm on}/I_{\rm off}$ ratio was more than 10^6 and SS was 46 mV/decade.

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Authors' photographs and biographies not available at the time of publication.