InAs FinFETs Performance Enhancement by Superacid Surface Treatment

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***Abstract*— In this paper, a post superacid (SA) treatment was proposed to enhance the performance of InAs FinFETs on SiO_2/Si substrates. Typically, the subthreshold swing (SS) has reduced from 217 to 170 mV/decade and the transconductance (g_m) has increased from 6.44 to 26.5 μS/μm after SA treatment. It was found that the interfacial In_2O_3 at the InAs/ZrO_2 interface was effectively reduced after SA treatment due to the strong protonating nature of the SA solution. As a result, the interface trap density was reduced leading to a pronounced reduction of sheet resistance after SA treatment. The modeling of transfer characteristics indicates that the carrier mobility is enhanced by 5.8∼7.1 folds after SA treatment due to interfacial traps reduction. The results suggest that SA treatment can be potentially extended to other III–V MOSFETs to enhance the device performances.**

***Index Terms*— FinFETs, superacid (SA), surface treatment.**

I. Introduction

SILICON-BASED transistors have been the workhorse of the semiconductor industry for several decades, enabling ever-increasing performance, density, and functionality. However, at the nanoscale, for technology nodes 7 nm and beyond, traditional scaling of silicon transistors has become increasingly difficult and does not give any performance improvement. In recent years, much attention has been paid to III–V n-MOSFETs, such as InP [1], $In_xGa_{1-x}As$ [2], and InAs [3] materials, due to their superior electron mobility and potential to enhance device performances. With Indium content enrichment, the injection velocity of $In_xGa_{1-x}As$ increases continuously rendering an attractive InAs channel material for n-MOSFET with an injection velocity of $\sim 4 \times 10^7$ cm/s. Simultaneously, the integration of III–V devices on a silicon substrate is in great need due to the tremendous infrastructure available for silicon processing. Indeed, heterogeneous integration of these materials on Si substrates is being vigorously explored [4]–[6]. Such technology offers a desirable combination of high channel mobility and the well-established, low-cost processing of Si technology. One of such techniques is the epitaxial transfer of InAs layers with nanometer scale thicknesses onto Si/SiO_2 substrates demonstrated for use as high-performance nanoscale transistors [7].

By employing the transferred InAs nanoribbons from this platform, InAs FinFETs can be made. Realizing feature sizes at sub-20 nm is one of the key steps to make these FinFETs. The dry etching process is a conventional tool to create such fine features due to its anisotropic etching property. Chlorine-based dry etching is often used to etch III–V materials. However, most of the chlorine-containing gases contain carbon and often problems are encountered with the deposition of polymer films during etching, resulting in a poor material surface quality and, therefore, degraded device performances. Various surface treatment methods to improve surface quality have been investigated, such as oxygen plasma treatment [8] and surface passivation techniques. However, these methods seem to be complex, costly, and time-consuming.

In this paper, we propose a simple and low-cost approach to improve the performance of InAs FinFETs fabricated by a dry etching process with post surface treatment by superacid (SA). The low field-effect mobility was observed to increase by 5.8∼7.1 folds reaching 671∼1378 $cm^2 \cdot V^{-1} \cdot s^{-1}$. To the best of our knowledge, this is the first demonstration of InAs FinFET mobility improvement by SA treatment. The detailed mechanisms are investigated and discussed.

II. Experimental Details

The InAs FinFETs were fabricated from InAs ribbons on SiO_2/Si substrate, which were obtained by the transfer method [7]. Epitaxially grown InAs films on AlGaSb/GaSb substrate were used as the InAs donor during the transfer process. Through standard lithography and wet etching, InAs ribbon arrays were first fabricated on the AlGaSb/GaSb substrate. After subsequent selective wet etch of the underlying

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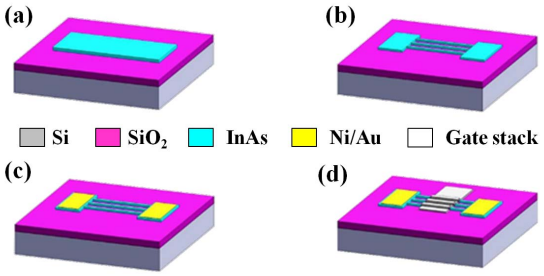

Fig. 1. Fabrication process flow of InAs FinFETs: (a) transfer of InAs ribbons on SiO_2/Si substrate; (b) fin formation on InAs ribbons; (c) metallization of S/D; and (d) deposition of gate oxide and gate metal.

AlGaSb layer, InAs ribbon arrays were then transferred on the SiO_2/Si substrate using an elastomeric PDMS slab, as shown in Fig. 1(a).

Fig. 1(b) and (c) further exhibits the schematic of the fabrication process for InAs FinFETs. By e-beam lithography (EBL) and inductively coupled plasma (ICP) dry etching methods, fins with widths of 20 and 25 nm were formed along the InAs ribbons [see Fig. 1(b)]. During this step, hydrogen silsesquioxane (HSQ) was used as EBL resist and subsequent dry etching mask. The ICP process was carried out at the ambient of $CH_4/H_2/Cl_2/Ar$ with a ratio of 8/5.5/5/15 for 25 s. The substrate holder was maintained at room temperature with ICP and RF power of 590 and 70 W, respectively. After dry etching, samples were dipped in diluted HF (HF:H_2O = 2:98) for 120 s to remove the HSQ mask. Next, contact windows were opened at the ends of the fins by EBL to form source/drain (S/D) metal contacts [see Fig. 1(c)]. After the removal of native oxide by diluted HF (HF: DI = 1:99), Ni/Au (40 nm/15 nm) metal was evaporated and lifted off. After that, 8-nm ZrO_2 was deposited as gate oxide by atomic layer deposition (ALD) at 130 °C with Tetrakis (ethylmethylamino) zirconium (IV) (TEMAZ) as Zr source and H_2O as oxygen source. Ultimately, 50-nm Ni was selectively evaporated as gate metal forming the final device with a channel length of 1 μm as shown in Fig. 1(d).

An organic SA, bis (trifluoromethane) sulfonamide (TFSI), which is a strong protonating agent and have a Hammett acidity function that is lower than pure sulfuric acid (H_2SO_4) [9], was prepared in a glove box for surface treatment on the completed InAs FinFETs. To prepare the TFSI solution, 24 mg TFSI powder was first dissolved in 12 mL 1, 2-dichloroethene (DCE) to form TFSI solution with solute concentration of 2 mg/mL; then 0.5 mL of the 2 mg/mL TFSI solution was diluted with 4.5 mL 1, 2-dichlorobenzene (DCB) forming a 0.2 mg/mL TFSI solution. The InAs FinFETs were immersed in the 0.2 mg/mL solution for 20 s at air ambient, then blow-dried with N_2.

The electrical performance of the InAs FinFETs before and after SA treatment was characterized by HP4156B semiconductor parameter analyzer. To facilitate analysis of chemical components at gate oxide/channel interface before and after SA treatment, X-ray photoelectron spectroscopy (XPS) were taken by PHI model 5600 with Al Kα dual sources (hν = 1486.6 eV) under a base pressure of 4×10^{-9} Torr [10], [11].

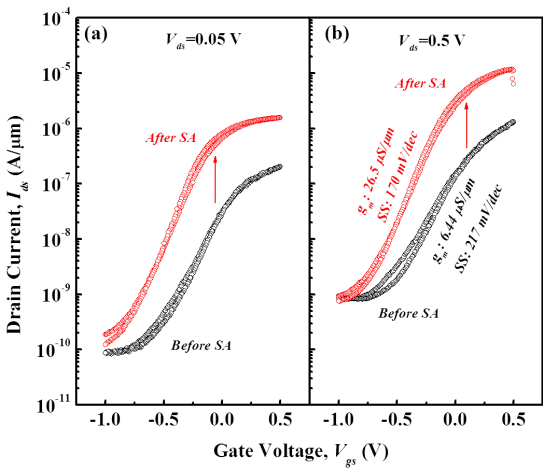

Fig. 2. Typical transfer characteristics of the InAs FinFETs with fin width of 25 nm before (black curve) and after SA (red curve) treatment under (a) V_{ds} = 0.05 and (b) V_{ds} = 0.5 V. A significant current increase and steeper *SS* after SA treatment can be observed.

III. Results and Discussions

A. I∼V Measurement

Fig. 2 shows typical transfer characteristics (I_{ds}–V_{gs}) of the FinFET with fin width of 25 nm before and after SA treatment at V_{ds} = 0.05 V [see Fig. 2(a)] and V_{ds} = 0.5 V [see Fig. 2(b)], respectively. Before SA treatment, a hysteresis of I∼V curves is observed when sweeping V_{gs} backward and forward due to the existence of abundant traps at the channel/gate oxide interface. With SA treatment, at V_{ds} = 0.05 V, the ON/OFF ratio increased from 2.35×10^3 to 8.18×10^3(∼3.5×) with ON-current from 0.20 to 1.56 μA/μm (∼7.8×). Similarly, at V_{ds} = 0.5 V, the ON/OFF ratio increased from 1.51×10^3 to 12.1×10^3(∼8×) with on-current from 1.30 to 13.15 μA/μm (∼10×). It should also be noted that, after SA treatment, the hysteresis phenomenon is not as pronounced. The extracted subthreshold swing (SS) is reduced from 217 to 170 mV/decade. The reduction of SS suggests that the density of interfacial traps (D_{it}) was effectively reduced after SA treatment. From the extracted SS, D_{it} can be quantitatively calculated based on the following equation [12]:

$$\frac{2.3\,\mathrm{kT}}{q}\left(1+\frac{C_{it}}{C_{ZrO_2}}+\frac{C_{body}}{C_{ZrO_2}}-\frac{\frac{C_{body}^2}{C_{ZrO_2}+C_{SiO_2}}}{1+\frac{C_{it}}{C_{SiO_2}}+\frac{C_{body}}{C_{SiO_2}}}\right)=\mathrm{SS}, \tag{1}$$

where k, T, and q are Boltzmann [12]: sed, sample temperature, and elementary charge, respectively; C_{ZrO2}, C_{SiO2}, and C_{body} represent the capacitance of ZrO_2, SiO_2, and the substrate per unit area, respectively; C_{it} is the capacitance caused by interface traps per unit area and is given by $C_{it} = qD_{it}$. For the presented device, D_{it} has reduced from 1.21×10^{13} cm^{-2} before SA treatment to 7.91×10^{12} cm^{-2} after SA treatment. The calculated D_{it} along with SS before and after SA treatment for several different devices were summarized in Table I. For all devices, both of SS and D_{it} values reduce

TABLE I
SUMMARY OF *SS* AND D_{IT} FOR DIFFERENT DEVICES BEFORE AND AFTER SA TREATMENT

Device (L_g=1 μm)		*SS* (mV/decade)	D_{it} (cm^{-2})
W_{fin}=25 nm	Before SA	156	$6.74x10^{12}$
	After SA	130	$4.69x10^{12}$
W_{fin}=25 nm (presented)	Before SA	217	$1.21x10^{13}$
	After SA	170	$7.91x10^{12}$
W_{fin}=20 nm	Before SA	98	$2.40x10^{12}$
	After SA	70	$6.20x10^{11}$
W_{fin}=20 nm	Before SA	530	$4.43x10^{13}$
	After SA	170	$8.76x10^{12}$

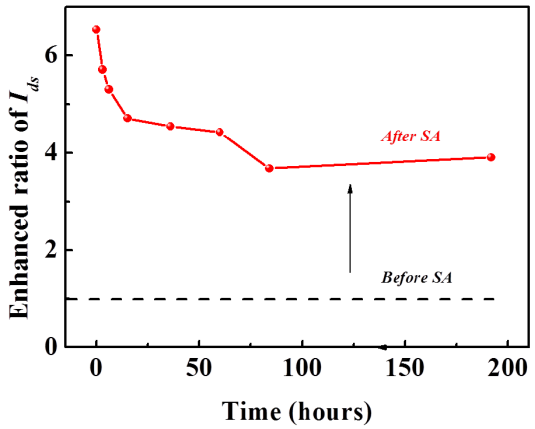

Fig. 3. Time-dependent study of I_{ds} enhancement ratio for the reproduced device (W_{fin}: 20 nm, L_g: 500 nm) after SA treatment under V_{gs} of 0.9 V and V_{ds} of 1 V.

distinctly after SA treatment indicating the passivation effect of SA on interfacial traps.

To verify the effectiveness of the proposed method, another batch of devices (W_{fin}: 20 nm, L_g: 500 nm) were fabricated and the improvement of the device performance was reproduced in a second lab (Previously done in UC Berkeley and now reproduced in University of Delaware). Fig. 3 displays the time-dependent study of I_{ds} for the reproduced device under V_{gs} of 0.9 V and V_{ds} of 1 V after SA treatment. The enhanced ratio of I_{ds} decreases gradually from 6.54 to 3.68 after ~80 h. However, as time further elapses, the enhanced ratio becomes almost constant within the studied period indicating stable enhancement of the device performance after SA treatment.

B. TLM Measurement

A linear transmission line model (TLM) was used to subsequently investigate the effect of SA treatment on the sheet resistance (R_s) and contact resistance (R_c) between InAs and Ni/Au. Electrodes with different gap spacing (l_d) were fabricated along the InAs ribbons on SiO_2/Si substrate, as shown in Fig. 4 (inset). The width of the ribbon was 4 μm (W) with contact areas of 4×4 μm^2, while l_d varied from 2 to 12 μm.

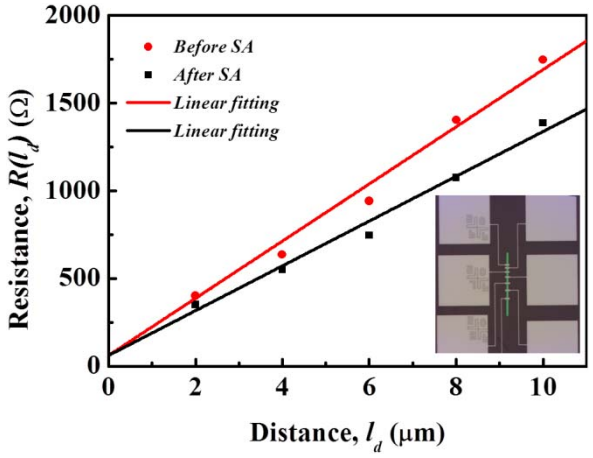

Fig. 4. Resistance (R) between adjacent pads as a function of gap spacing (l_d) from transmission line measurement under different conditions before (red) and after (black) SA treatment.

Through measuring the resistance (R) between adjacent pads, R_s and R_c can be extracted from the linear fitting of the $R \sim l_d$ curve by the following equation [13]:

$$R(l_d) = R_s \frac{l_d}{W} + 2R_c. \quad (2)$$

Fig. 4 shows the measured values of R under different l_d along with corresponding fitting results before and after SA treatment. External resistance had been eliminated by using Kelvin probes. The measured results reveal that R_s had reduced from 652.1 to 501.5 Ω/□, while R_c remained almost the same at 30.5 Ω after SA treatment suggesting enhancement of the InAs mobility due to the reduction of D_{it}. Consequently, the improvement of on-current of InAs FinFETs after SA treatment can be ascribed to a reduction of R_s.

It should be noted that the TLM measurements were carried out on InAs ribbons rather than on Fin structures. For InAs ribbons, the sidewalls were formed by wet etching instead of ICP dry etching. Therefore, the interface trap density at these sidewalls is expected to be less than that formed by dry etching. The reduction of sheet resistance was mainly due to the passivation of interfacial states on the top surface. While for Fin structures, the passivation effect on the two side walls should also be considered since the channel of FinFETs was controlled on both the top surface and side walls. Thus, the actual reduction of sheet resistance for FinFETs may be much more pronounced leading to a significant enhancement of carrier mobility.

C. XPS Measurement

To shed light on passivation mechanisms of the interfacial traps after SA treatment, high-resolution XPS measurements were carried out. Fig. 5(a) and (b) displays the measured spectrum of O 1s for an InAs film on Si before and after SA treatment, respectively. The peak positions have been calibrated by C 1s peak (284.8 eV) and the background intensity has been subtracted. From peak fitting results by PHI MATLAB code, two subpeaks due to native oxides are observed in O 1s spectrum before SA treatment. The peak at

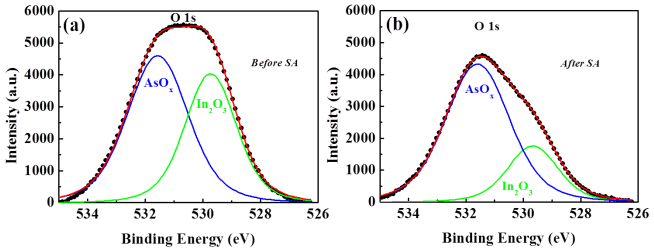

Fig. 5. Measured XPS spectra of O 1s and related fitting results for InAs (a) before and (b) after SA treatment, respectively. The native oxide of InAs, especially In_2O_3, was effectively reduced after SA treatment.

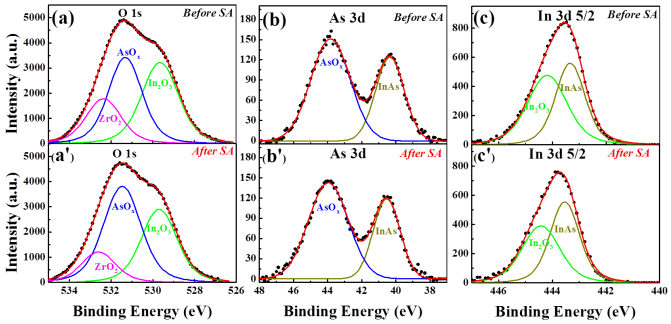

Fig. 6. XPS spectra of (a) O 1s, (b) As 3d and (c) In 3d 5/2 and related fitting results for InAs on Si substrate encapsulated with 4-nm ZrO_2 before SA treatment; XPS spectra of (a') O 1s, (b') As 3d and (c') In 3d 5/2 and related fitting results for InAs electronic device encapsulated with ZrO_2 after SA treatment.

529.7 eV corresponds to In_2O_3 while the peak at 531.5 eV corresponds to AsO_x(a mixture of As_2O_3 and As_2O_5) [14]–[16]. After SA treatment, the intensity of AsO_x remains almost constant, while the intensity of In_2O_3 reduces greatly. The integrated intensity ratio between AsO_x and In_2O_3 has increased from 1.34 before SA treatment to 3.13 after SA treatment. The result suggests that the native oxide of InAs, especially In_2O_3, can be effectively reduced after SA treatment due to strong protonating nature of the SA solution.

Fig. 6(a)–(c) displays the XPS spectrum of O 1s, As 3d, and In 3d 5/2 and related fitting results for InAs on Si substrate encapsulated with 4-nm ZrO_2 [15]–[17] before SA treatment, respectively. The corresponding results after SA treatment are shown in Fig. 6(a')–(c'), respectively.

From Fig. 6(a) and (a'), an additional peak of ZrO_2 located at 532.5 eV is observed. The intensity of AsO_x remains almost constant after SA treatment, while the intensities of In_2O_3 and ZrO_2 components decrease. The integrated intensity ratio between AsO_x and In_2O_3 has increased from 0.98 before SA treatment to 1.38 after SA treatment. In Fig. 6(b) and (b'), the fitting peaks at 40.4 and 43.9 eV correspond to AsO_x and InAs, respectively. The intensity of AsO_x and InAs peaks remain almost constant after SA treatment, agreeing well with the result from O 1s spectra. As for In 3d 5/2 spectra, the fitting peaks at 444.3 and 443.4 eV correspond to In_2O_3 and InAs, respectively. After SA treatment, the intensity of InAs remains almost constant, while the integrated intensity ratio between In_2O_3 and InAs decreases from 1.14 to 0.90 after SA treatment. The aforementioned results demonstrate that the

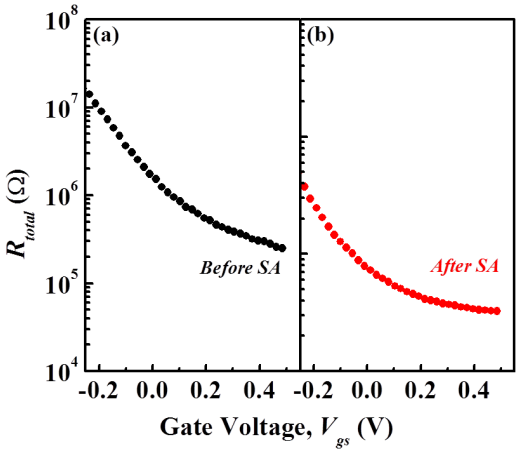

Fig. 7. Total series resistance (R_{total}) of InAs FinFET calculated by $R_{total} = V_{ds}/I_{ds}$ from experimental data (a) before and (b) after SA treatment.

interfacial oxide at the InAs/ZrO_2 interface, especially In_2O_3, is effectively reduced after SA treatment.

As reported, oxides are notorious for fast diffusion of hydrogen and its ion [18]. Although metal gate was deposited on ZrO_2 above the channel, hydrogen ions (H^+) can first diffuse vertically in the ZrO_2 layer in the gap between gate and source (drain), which was not covered by Ni, then diffuse laterally under the Au/Ni gate through ZrO_2 rendering reactivation of H^+ with In_2O_3 at the ZrO_2/InAs interface. The interfacial trap density is thus effectively reduced, leading to a significant mobility enhancement.

D. BSIM Model

To further investigate the effect of SA treatment on the carrier mobility of InAs FinFETs, we have modeled I–V characteristics before and after SA treatment based on the industry standard compact model BSIM-CMG [19]. The BSIM-CMG model has considered the quantum-mechanical effects for charge calculations, which is of great significance for III–V materials. Before modeling the I–V curves, the parasitic series resistance between source and drain (R_{ds}) and the channel resistance ($R_{channel}$) should be given. However, the accurate extraction of R_{ds} suffers from uncertainties due to limitations of the extraction methods which include data scalability and accuracy. Herein, we take a pragmatic approach to estimate the carrier mobility for our devices.

From linear I_{ds}–V_{ds} characteristics, the total resistance (R_{total}) between source and drain, which consists of R_{ds} and $R_{channel}$, can be calculated by $R_{total} = V_{ds}/I_{ds}$. For the reported device shown in Fig. 2, the dependence of R_{total} on V_{gs} before and after SA treatment has been summarized in Fig. 7(a) and (b), respectively. Since $R_{channel}$ is inversely proportional to (V_{gs}–V_{th}), where V_{th} is threshold voltage, R_{total} becomes smaller at a higher value of V_{gs}. For our goal of finding an estimated improvement of carrier mobility after SA treatment, we consider that R_{ds} falls in the range from 10% to 95% of R_{total} at the highest V_{gs} ($V_{gs} = 0.5$ V). The consideration follows from practical reasoning that a value

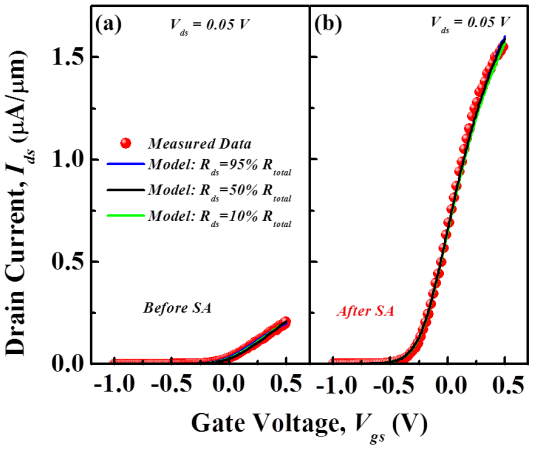

Fig. 8. Modeled I_{ds}–V_{gs} characteristics of InAs FinFETs (a) before and (b) after SA treatment at V_{ds} of 0.05 V based on the BSIM-CMG model. The modeling was performed taking R_{ds} 10% –95% of R_{total}.

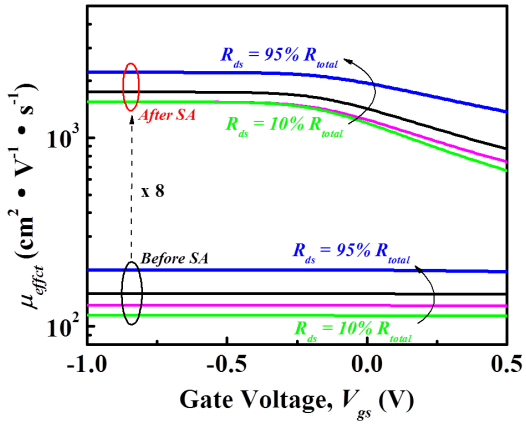

Fig. 9. Extracted effective carrier mobility (μ_{effect}) of InAs FinFETs versus V_{gs} before and after SA treatment by I_{ds}–V_{gs} modeling based on the BSIM-CMG model. The modeling was performed taking R_{ds} 10%∼95% of R_{total}. After SA treatment, the carrier mobility is enhanced by 5.8∼7.1 folds.

of R_{ds} larger than 95% of R_{total} would require nonphysical channel mobility to explain experimental drain current. For instance, if one attributes all R_{total} to R_{ds} (i.e., R_{ds} is 100% of R_{total}) at highest V_{gs}, it would require infinite channel mobility to match the measured drain current. The lower limitation of R_{ds} is summarized from typical values of actual devices [20]. With this range of R_{ds}, we have modeled the I_{ds}–V_{gs} characteristics of the InAs FinFETs before and after SA treatment taking R_{ds} 10%–95% of R_{total}, as shown in Fig. 8(a) and (b), respectively. As can be seen, the modeled curves agree very well with the experimental data for the considered R_{ds} values. The extracted effective carrier mobility as a function of V_{gs} before and after SA treatment is exhibited in Fig. 9. Under V_{gs} of 0.5 V, the carrier mobility before SA treatment is estimated to be 114∼195 $cm^2 \cdot V^{-1} \cdot s^{-1}$. After SA treatment, the carrier mobility is increased to 671–1378 $cm^2 \cdot V^{-1} \cdot s^{-1}$, about 5.8∼7.1 folds enhancement.

Ultimately, the extracted mobility values are validated by modeling the saturated transfer characteristics of InAs FinFET under V_{ds} of 0.5 V taking R_{ds} 10%∼95% of R_{total}. With a

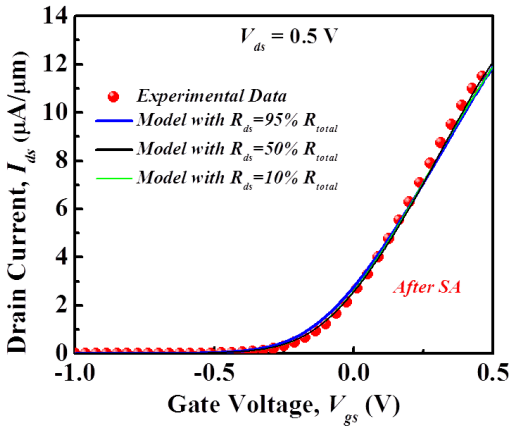

Fig. 10. Modeling of the saturation transfer characteristics of InAs FinFETs under V_{ds} of 0.5 V taking R_{ds} 10%∼95% of R_{total}. A physically reasonable range of 1-1.2 × 10^7 cm/s for saturation velocity was considered for the modeling.

physically reasonable range of 1–1.2 × 10^7 cm/s for saturation velocity (v_{sat}) [21], the modeled saturation I_{ds}–V_{gs} curves are presented in Fig. 10, which agree very well with the experimental data. The enhancement of carrier mobility is attributed to the reduction in interfacial traps between InAs and ZrO_2 after SA treatment as mentioned earlier since the interfacial charges have a trapping and scattering effect to the carriers. Such enhancement of device performance due to SA treatment can be potentially extended to other III–V MOSFETs consisting of III–V oxide interfacial layers.

IV. Conclusion

In summary, we propose a surface treatment method by SA to improve the performance of InAs FinFETs on SiO_2/Si substrate. For the reported device, the SS and g_m have reduced from 217 mV/decade and 6.44 × 10^{-6} S to 170 mV/decade and 2.65 × 10^{-5} S with SA treatment, respectively. Through XPS analysis, it was found that the interfacial oxide at the InAs/ZrO_2 interface was effectively reduced after SA treatment due to strong protonating nature of the SA solution. The TLM measurements show that the sheet resistance of the InAs ribbon can be greatly reduced from 652.1 to 501.48 Ω/□ while the contact resistance is not influenced after SA treatment. From modeling of the transfer characteristics based on the commercial BSIM-CMG model, it was found that the carrier mobility is enhanced from 114∼195 $cm^2V^{-1} \cdot s^{-1}$ before SA treatment to 671∼1378 $cm^2\ V^{-1} \cdot s^{-1}$ after SA treatment due to the reduction of interfacial traps. The results suggest that the SA treatment can be potentially extended to other III–V MOSFETs to enhance the device performances.

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