Prospect of Tunneling Green Transistor for 0.1V CMOS

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Abstract

Well designed tunneling green transistor may enable future VLSIs operating at 0.1V. Sub-60mV/decade characteristics have been convincingly demonstrated on 8" wafers. Large I_{ON} at low V_{DD} are possible according to TCAD simulations but awaits verification. V_{DD} scaling will greatly benefit from low (effective) band gap energy, which may be provided by type II heterojunctions of Si/Ge or compound semiconductors.

A Looming Barrier to IC Scaling

Reducing the voltage V_{DD} is a powerful way to reduce IC energy consumption, which is proportional to V_{DD}^2. Power usage was kept under control when V_{DD} was reduced in proportion to half-pitch up to 130nm as shown in Fig 1 [1]. The 14nm node is projected to operate at 0.7V, making the power consumption 25x larger than it would be if operated at 0.14V as the past trend suggests. While IC power consumption has been much discussed as a thermal management challenge, it is also responsible for a few percent of the electricity usage and growing fast. MOSFET current cannot rise faster than one decade for every 60mV increase in V_g (the subthreshold swing, SS). To reduce V_{DD} to 0.14V with I_{ON}/I_{OFF} ratio of mere 3 decades, SS needs to be 45mV/decade. A low voltage transistor (Green Transistor, gFET) is needed.

Green Transistor with Steep Turn On/Off

In MOSFETs (and BJTs), a potential barrier is raised and lowered by V_g to turn the current on and off (Fig. 2). Due to Boltzmann distribution, some electrons always have sufficient energy to pass over the barrier. The current can only be reduced by the rate of electron density drop with increasing energy, hence the 60 mV/decade limit [1]. To beat this limit, the carriers must not flow over a barrier. They may tunnel through it.

Fig. 3 shows a prototype tunnel transistor [1-4]. Electrons are generated by band-to-band tunneling in the P+ source when the gate voltage bends the energy band to satisfy two conditions—overlap of the valence and conduction bands and the a high electric field or thin tunnel barrier [5]. The generated electrons flow through the surface N-channel to the drain. Fig. 4 shows simulated I_d-V_g [6] assuming uniform source doping. In all > 3E19 cm^{-3} cases, steep turn on occurs at the onset of band overlap. Unfortunately the graded source doping profile and the averaging effect of the Poisson equation provide a continuous range of (effective) doping concentration near the tip of the source. At points of lower doping (Fig. 4) the turn-on voltages and electric field (therefore I_{ON}) are both lower. The envelope of these curves is the IV of a prototype tunnel transistor, with a disappointing sub-V_t swing.

Node (nm)	250	180	130	90	65	32	14
V_{dd} (V)	2.5	1.8	1.3	1.2	1.1	0.9	0.7

Fig. 1. IC V_{DD} scaling history and ITRS projection. Slowdown since 90nm leads to accelerated rise in energy consumption.

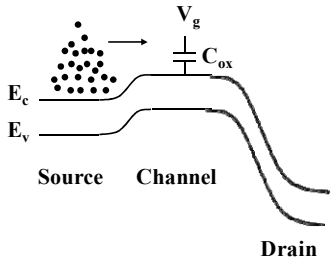

Fig. 2. Boltzmann statistics lead to the 60mV/decade limit because current is controlled with an energy barrier [1].

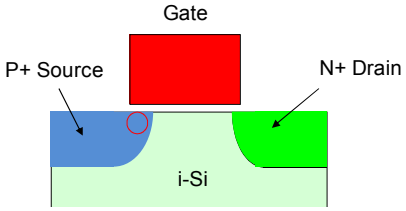

Fig. 3. In a prototype N-type tunnel transistor, electrons are generated by tunneling in the red-circle region.

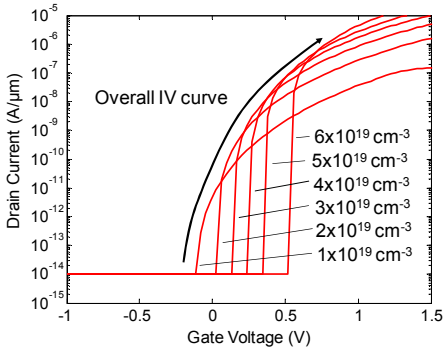

Fig. 4. Simulated I_{DS} is varied with source doping. Envelope of the curves leads to a poor sub-V_t swing of a tunneling transistor.

Fig. 5 shows a design that lowers the turn-on voltage of the heavily doped part of the source [1]. Fig. 6 shows the evolution of the IV of Si gFETs of this type as the pocket doping is increased [6]. Fig. 7 illustrates the concept of steep turn on at the sudden onset of the overlap of the conduction and valence bands.

Another approach is to use a very steep source doping profile to minimize the size of the low doping part of the source (but not the Poisson averaging effect). Fig. 8 shows that sub-60mV/decade average SS is achieved over six orders of magnitude of current with a device similar to Fig. 3 but fabricated on Si SOI substrate with a Ge source [7]. After gate and drain formation, the source region was etched and refilled with insitu doped poly-Ge at low temperature. Fig. 9 shows yet another gFET design that produces steep turn on/off. The graded source region is minimized with dopant segregation from NiSi and a thin semiconductor pocket is created between the gate dielectric and underlying NiSi [8]. The vertical electric field is enhanced in the thin pocket to further reduce the source edge effect. The measured 46 mV/decade SS could only be reproduced by simulation when a semiconductor pocket is present as shown is Fig. 9. Fig. 10 shows the X-SEM images of the device with a wedge-shaped pocket between the silicide and the gate dielectric. This geometry is produced by recessing the source before the salicide steps. A control device without the pocket was also fabricated for comparison. Fig. 11 shows the measured I_D-V_G characteristics of the gFET vs. the control device. The minimum SS of the gFET is 46mV/dec. Another lot successfully reproduced the result two months later with 47mV/dec SS. As seen in Fig. 12, the gFET shows sub-60mV/dec SS over 3 decades of drain current. Special care must be taken to screen out low SS data due to various causes (Fig. 14). Statistical distributions of swing show that more than 30% of the gFETs on an 8" wafer have sub-60mV/dec SS (Fig. 15). The measured I_D-V_D characteristics of the gFET (Fig. 16) are similar to MOSFET's.

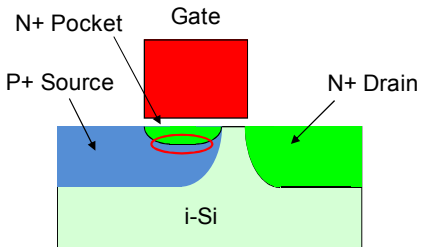

Fig. 5. One design of a low SS swing gFET. The N pocket lowers the turn-on voltage of the heavily doped source region.

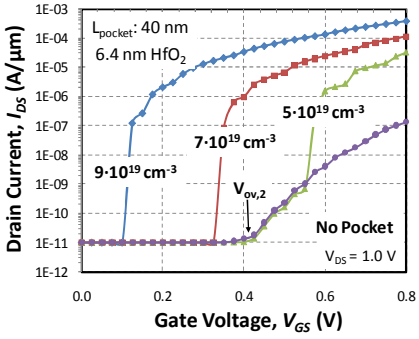

Fig. 6. N pocket doping reduces the turn-on voltage. Uniform 5E19 cm^{-3} doped P+ source. TCAD simulation.

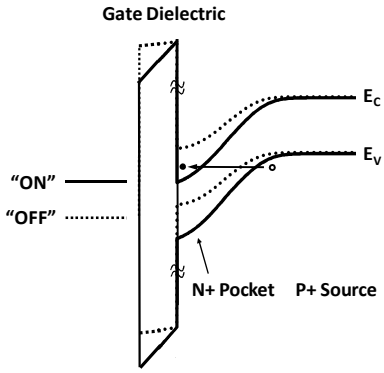

Fig. 7. Energy diagram from gate through pocket to source. Device is off when there is no overlap of valence and conduction bands.

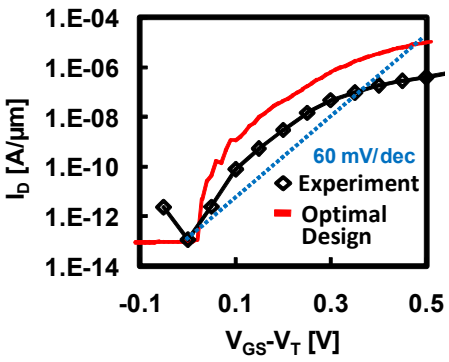

Fig. 8. Deposited insitu doped Ge source gFET produced sub-60mV/dec. average SS measured over 6 orders of current [7].

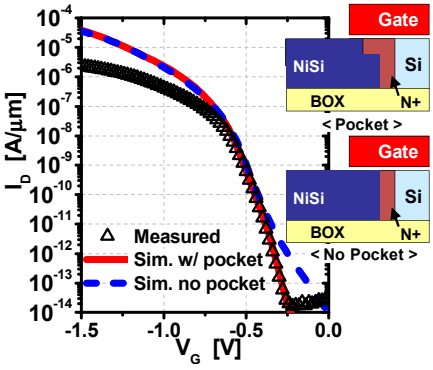

Fig. 9. Another design achieves less than 60mV/dec. swing with a semiconductor pocket between oxide and metal (NiSi) [8].

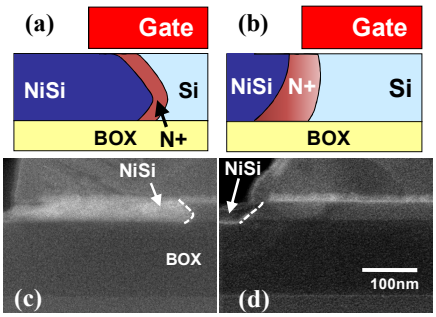

Fig. 10. Structure and cross-section SEM at source side of dopant segregated gFET (a), (c) and control device (b), (d). [8]

Prospects of Large I_{ON} at 0.1V V_{DD}

Simulations show that V_{DD} can be scaled by reducing E_g (Fig. 17). Only E_g was reduced in simulation, not any other tunneling parameters [1]. At E_g=0.36eV I_{ON} exceeds 1mA/μm at V_{DD}=0.2V with CV/I=0.4pS and can operate well at 0.1V (Fig. 18). A type II hetero-junction gFET [9] provides an effective tunneling band gap (E_{geff}) lower than the E_g of both materials (Fig. 19, 20). Materials A and B can be simply strained Si thin film on Ge for N-gFET with theoretical E_{geff} of around 0.18eV (Fig. 21), suitable for 0.1V gFET. Strained Ge on Si is attractive for P-gFET. A and B can be compound semiconductors such as InAs on AlGaSb with E_{geff} adjustable through the Ga/Sb ratio (Fig. 22). The low density-of-states and strong quantization of low effective-mass materials pose a serious challenge to gFET design.

Conclusion

Carefully designed tunneling green transistors can potentially enable 0.1V ICs. Sub-60mV/dec subthreshold swing has been demonstrated on 8'' wafers with statistical data. High current and low voltage operation needs small effective band gap energy which may be provided by type II heterojunctions of Si/Ge or compound semiconductors. gFET in Fig. 5 is insensitive to gate length variations (Fig. 23) because the tunnel path is enclosed in the source and shielded from the influence of the drain.

Acknowledgement

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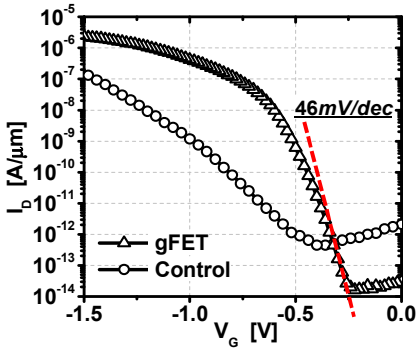

Fig. 11. I_D-V_G of measured gFET showing SS of 46mV/dec. (L_G=20μm, V_{DS}=-1.0V)

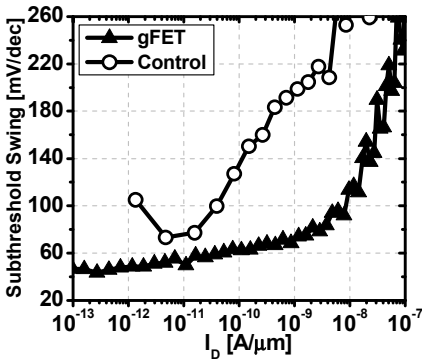

Fig. 12. SS < 60mV/dec over almost 3 decades of I_D for the gFET, but not seen in the control tunnel transistor.

	Ref. [2]	Ref. [3]	Ref. [4]	This Work
SS (mV/dec)	52.8	42	~300	46
I_{ON} (μA/μm)	12.1	0.01	1E-4	1.2
I_{ON}/I_{OFF}	1E4	1E4	1E2	7E7

Fig. 13. Comparison with other reported silicon tunnel transistors [8].V_{DS} = V_{GS}-V_{BTBT}= 1.0V.

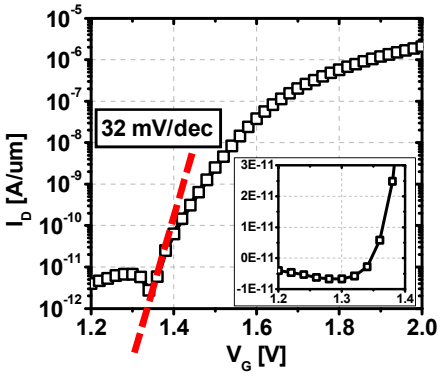

Fig. 14. Phantom low SS can show up without proper screening.

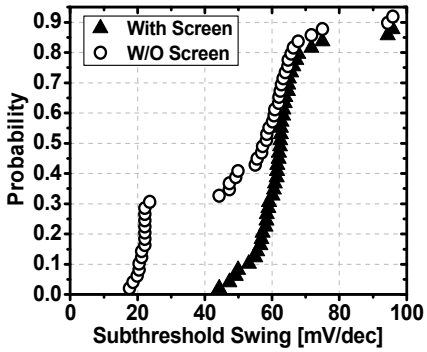

Fig. 15. SS distribution comparison of gFET swing with and without proper screen [8].

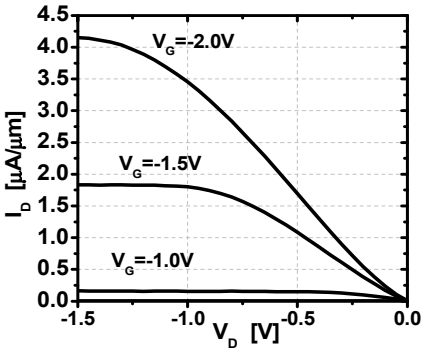

Fig. 16. Measured I_D-V_D of gFET showing typical tunneling transistor behavior [8].

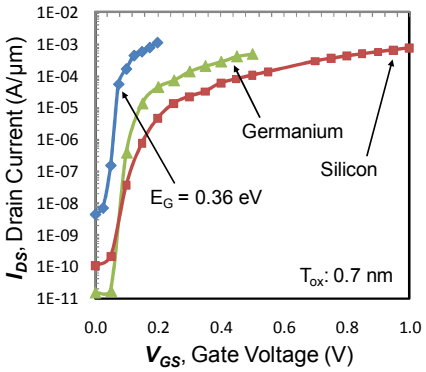

Fig. 17. Reducing the E_g is a new path for scaling the V_{DD} for ICs. CV/I is ~ < 1 pS. Only E_g is varied in simulation [1].

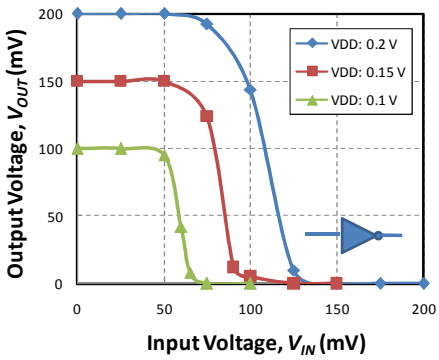

Fig. 18. P/N type gFETs of Fig. 17 with Eg=0.36eV produce excellent simulated inverter transfer curves even at 0.1V [1].

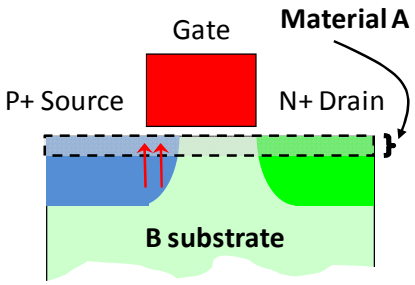

Fig. 19. A heterojunction gFET [9]. See Fig. 20 for explanation.

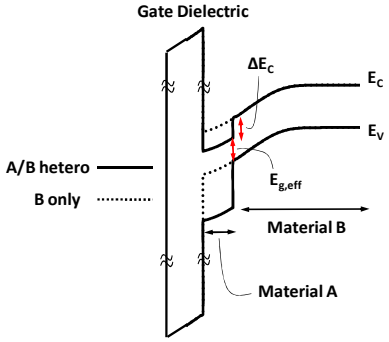

Fig. 20. The effective tunneling band gap in Type II heterojunction is smaller than those of A and B alone [9].

	Ref. [10]	Ref. [11]	Ref. [12]
ΔE_C	0.55	0.57	0.58
ΔE_V	0.31	0.25	0.21
$E_{g,s\text{-}Si}$	0.42	0.35	0.37
$E_{g,eff}$	0.19	0.17	0.16

Fig. 21. Theoretical E_{geff} of a Ge-strained Si gFET is around 0.18eV, good for V_{DD}<0.1V operation (see Fig. 17).

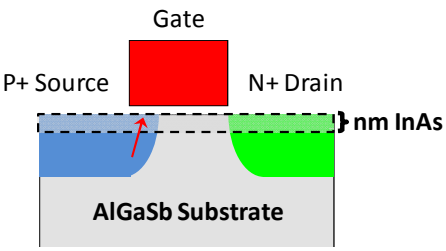

Fig. 22. gFET may employ heterojunction of compound semiconductor with tunable E_{geff}.

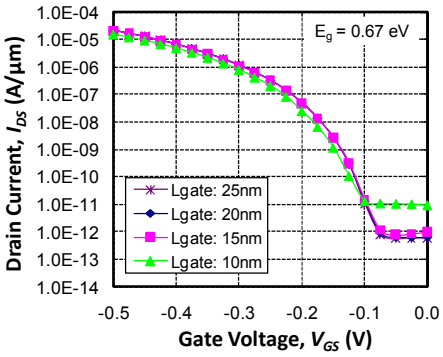

Fig. 23. Simulated gFET IV is insensitive to L_G variation because the tunneling region is in the N+ source, protected from the drain.