Carbon Nanotubes: From Growth, Placement and Assembly Control to 60mV/decade and Sub-60 mV/decade Tunnel Transistors

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Abstract

This paper presents recent progress on placement and orientation control of single-walled carbon nanotubes (SWNTs) by both CVD and PECVD growth in electric fields and on single crystal quartz substrates, and post-growth Langmuir Bloddget assembly of close-packed SWNTs. We also present fabrication of nanotube field effect-transistors (FETs) including MOSFET like devices with 60mV/decade switching and ambipolar P-I-N band-to-band tunnel (BTBT) transistors with subthreshold swings down to 25mV/decade.

Introduction

Single-walled carbon nanotubes (SWNTs) are candidate materials for future integrated circuits owing to their unique properties including 1D near-ballistic transport, high mobility for both electrons and holes, chemical robustness, lack of surface dangling bonds and sustained electrical properties when integrated into realistic device structures. A SWNT can be either metallic or semiconducting (Fig.1) depending on chirality, and the band-gaps of semiconducting SWNTs scale inversely with the tube diameter *d*. Obtaining purely metallic or semiconducting tubes with diameter, chirality, placement and orientation control have been major challenges for these materials. This review presents some of our efforts in addressing these issues. We also report our recent developments of ambiploar sub-60mV/decade SWNT tunneling FETs based on band to band tunneling.

Placement, Alignment and Diameter control

One approach to control the placement of SWNTs is to control the sites from which nanotubes are grown by patterning catalyst particles on a substrate. The initial idea of such patterned growth was demonstrated with micron scale islands of catalyst patterned on SiO_2/Si wafers (Fig.2a) (1). Approximate location control of SWNTs (without orientation control) was obtained by chemical vapor deposition (CVD) growth of nanotubes from the catalyst islands. Since the initial patterned CVD growth demonstration, single-catalyst particle patterning on substrates and orientation control of SWNTs grown by CVD have been actively pursued. Single catalyst-nanoparticle patterning (Fig.2b) for SWNTs growth by CVD was achieved recently (Fig.2c) (2). Arrays of regularly spaced ~2 nm catalyst (Fe or Co) nanoparticles were formed on SiO_2/Si by high-resolution electron-beam lithography (EBL) to afford ~20nm holes in PMMA, angle-evaporation (5°-6°) of ultrathin 1-2Å of Fe or Co into the holes, lift-off and thermal annealing at ~800°C to aggregate the metal atom in the holes to form down to ~2nm nanoparticles (2).

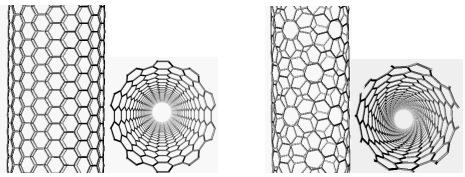

Figure 1. Schematic structures of a metallic (left) and chiral semiconducting (right) carbon nanotube.

An important goal of placement control of SWNTs is orientation control of nanotubes. Previously, we successfully applied electric-fields during patterned CVD growth and produced well aligned SWNTs suspended over trenches (Fig.3a) and on SiO_2/Si substrates (Fig.3b) (3, 4). More recently, lattice directed growth was successful in aligned CVD growth of SWNTs on single-crystal quartz and sapphire surfaces by two groups (5, 6). The driving force for the aligned nanotube growth was suggested to be due to strong interactions between SWNTs and the crystallographic steps on the substrates. Here, we report successful lattice-aligned growth of SWNTs on quartz by a novel plasma enhanced CVD (PECVD) method. We first calcined s-t cut quartz substrates in air at 900°C for 24 hours to form crystallographic steps on the surface, patterned silica supported Fe-Co-Mo (molar ratio of 10:10:1) catalyst on the quartz substrate by EBL, and carried out PECVD growth under a pressure of 0.35 torr at 800°C. The reaction gases included methane, hydrogen and oxygen for a growth time of 15min (7). The PECVD growth afforded well-aligned SWNTs with lengths up to 40 μm without any mis-aligned tubes (Fig.3c).

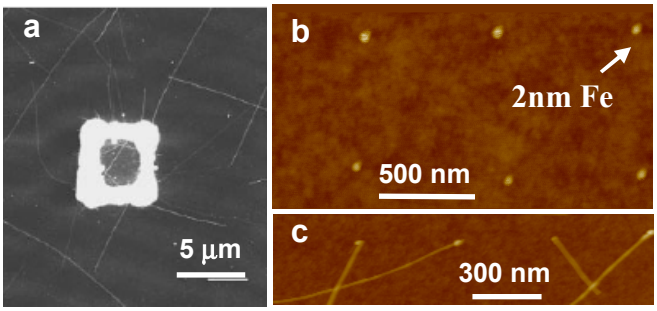

Figure 2. Patterned growth of SWNTs. (a) previous (Ref.1) growth from micron-sized catalyst island (white structure). (b) AFM image of a regular array of individual Fe clusters (Ref.2). (c) Recent SWNTs grown from single-particle array (Ref.2).

The PECVD method is advantageous over simple CVD in higher growth reproducibility of long tubes, elimination of

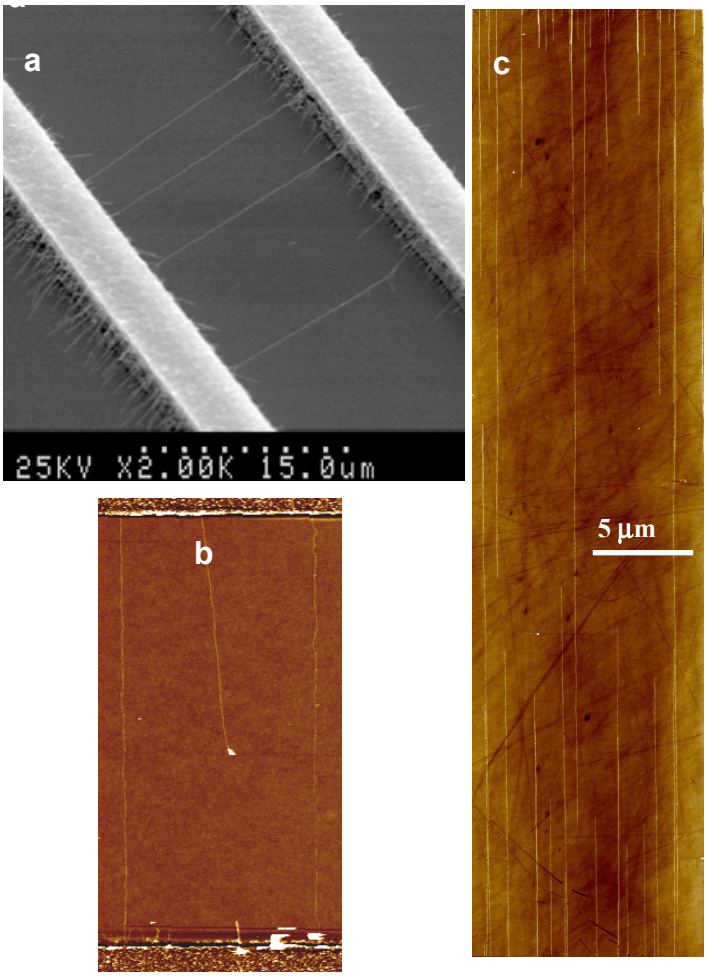

Figure 3. Oriented growth of SWNTs. (a) Aligned suspended SWNTs grown in an electric field. (b) Aligned SWNTs grown on SiO_2 substrate in an electric field. (c) Aligned SWNTs grown by PECVD on crystalline quartz substrate and aligned along the quartz crystal lattice.

mis-aligned tubes, narrower diameter distribution and preferential growth of semiconducting SWNTs (8).

Diameter control is important to SWNT transistor applications since the band-gap of a nanotube scales as *1/d*. It

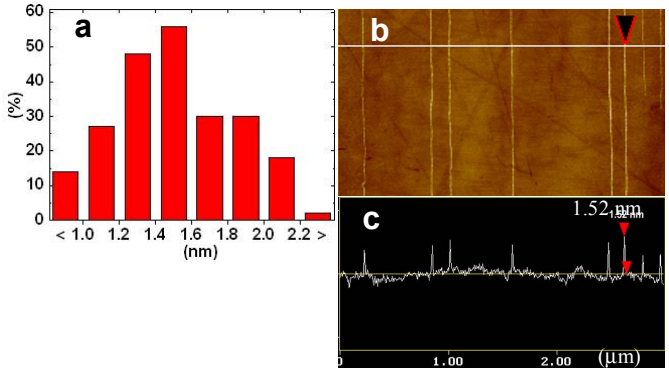

Figure 4. (a) Diameter distribution of aligned SWNTs grown on quartz. (b) An AFM image and (c) height profile along the gray line in b.

is desirable to obtain narrowly distributed SWNTs in the diameter range of ~1.3nm to ~1.8nm. Above 1.8nm, the nanotube band-gap becomes too small to maintain low off currents for SWNT FETs. Below ~1.2nm, ohmic contacts for SWNTs are difficult (9). Using PECVD, we were able to optimize the growth condition and obtain aligned SWNTs with the majority of the nanotubes in the diameter range of 1.2nm to 1.8nm (Fig.4). Further narrowing of the diameter distribution is still needed for future electronic applications.

Langmuir Bloddget Assembly of SWNTs

Assembly of pre-made, chemically processed SWNTs on substrates is also a promising approach to nanotube placement. Langmuir Bloddget (LB) film has been known for decades as an effective method for making well-organized organic monolayer patterns (10). LB films have also been made for nanowires or nanorods (11). Here, we report LB films of SWNTs. We first suspended Hipco SWNTs in an organic solvent dichloroethane (DCE) by sonicating nanotubes and centrifugation to remove un-suspended materials. SWNTs thus suspended in DCE have lengths in the range of 100-500nm and diameters between 1.0 to 1.6nm. LB film of SWNTs was made by adding SWNT DCE solutions to water

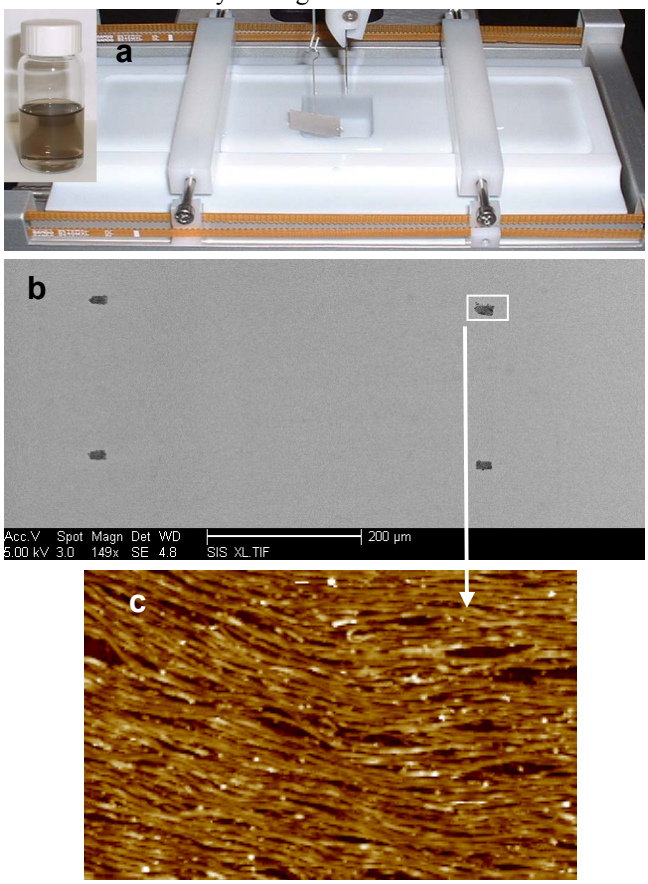

Figure 5. Langmuir bloddget LB assembly of SWNTs. (a) A photo of a LB trough. Inset: a SWNT suspension in DCE. (b) A SEM image showing a patterned SWNT LB film on SiO_2. (c) A zoom-in AFM image of SWNTs LB film in a patterned region.

in a LB trough (Fig.5a) to form a layer of SWNTs floating on water surface upon vaporization of DCE. Aligned SWNT

film was then formed by compressing the SWNTs on water surface using two barriers. Such a film was then transferred to a substrate by simple dipping.

Figure 5 shows a typical SWNT LB film transferred onto a SiO_2/Si substrate. Lithographic patterning and oxygen plasma was carried out on the as-made LB film to etch away SWNTs in unwanted areas and form patterned structures (Fig.5b). Within the patterned LB films, SWNTs were densely packed and quasi-aligned (Fig. 5c). The patterned LB films will allow large numbers of parallel SWNTs to be used for a FET channel. The spacing between adjacent nanotubes in a LB film should be controllable by various chemical means down to a few nanometers and is currently being pursued.

60mV/dec SWNT FET devices

On the device application side, relatively thick films (~8nm) of high-κ materials (ZrO_2 and HfO_2, κ~15-25) have been used for SWNT FETs. Recently, we developed non-covalent functionalized SWNTs with ploy-T DNA molecules (dT40) for uniform and conformal atomic layer deposition (ALD) of high- κ dielectrics on SWNTs with thickness down to 2-3 nm (Fig.6a, 6b) (12). SWNTs were grown by chemical vapor deposition on SiO_2/Si substrate from an array of patterned catalyst sites. Source (S) and drain (D) electrodes (distanced ~1.5 μm) were fabricated by EBL with 0.5nm Ti/20nm Au as S/D contacts. For DNA functionalization of the SWNT segments between the S/D electrode pairs, an

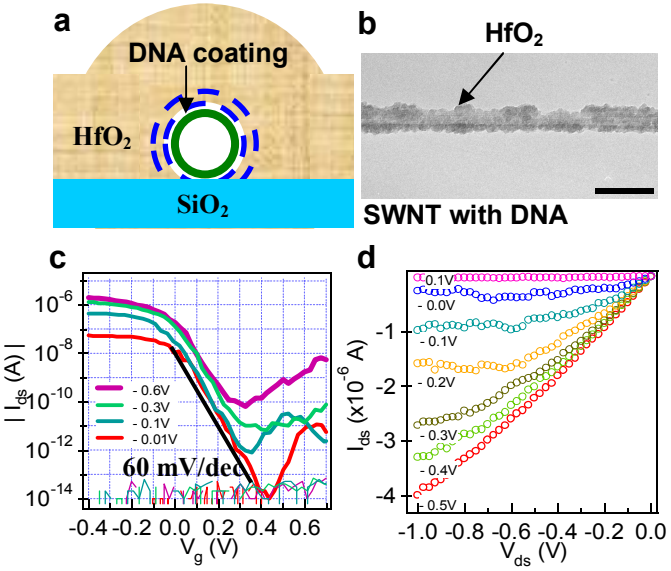

Figure 6. 60mV/decade SWNT FETs. (a) A schematic of conformal HfO_2 coating on a DNA functionalized SWNT. (2) A TEM image. (c) Transfer characteristics of a SWNT FET (MOSFET-like, with contact regions P-doped by back-gating) with 2-3nm HfO_2 gate oxide. (d) I-V characteristic.

oligonucleotide consisting of 40 thymine bases (dT40) was used. The SWNT device chip was placed in a 10 μM dT40-DNA water solution for 30min, followed by 2-min gentle sonication of the chip in pure water and then rinsing and drying under a nitrogen stream. This gave rise to non-covalent absorption of DNA on SWNT sidewalls. ALD of HfO_2 on the chip was then performed at 90ºC to form 2-3nm films at a rate of ~ 0.13nm per ALD cycle. After the ALD step, top-gate (Pt) under-lapping the S/D (100nm gate length) was formed by EBL patterning of PMMA, Pt (18nm) metal evaporation and lift off in acetone. The thin 2-3nm HfO_2 gate dielectric layers in our devices enabled us to approach the ultimate vertical scaling limit of nanotube MOSFETs and reliably achieve subthreshold slope (SS) of SS~60 mV/decade at room temperature (Fig.6c, 6d). Without functionalization, ALD on SWNTs lacked nucleation sites, the dielectric deposition was spotty, non-uniform and non-conformal and required thick deposition to avoid gate leakage.

Sub 60mV/dec P-I-N Tunnel devices

Vertical scaling of SWNT FETs is useful to exploring new device types including tunnel transistors. It is well known that for MOSFETs, SS is limited at 60mV/dec at room temperature due to the thermal tail of Fermi-Dirac distribution. It has been suggested that sub-60mV/dec switching can be obtained with PIN transistors operating in the band-to-band tunneling (BTBT) regime (13, 14). Here, we report that by *p*- and *n*-doping of the S and D respectively of SWNT FETs, we obtain SWNT P-I-N FETs (gate-dielectric t_{ox}~3nm) with SS down to ~25mV/dec for both *p*- and *n*-channel conduction. The fabrication process is shown in Fig. 7a as follows: (1) patterned CVD growth of SWNT was done on 500nm SiO_2/P^{++}Si substrate, Ti/Au was deposited as the S/D metal at a S-D distance of 2μm. (2) A ~200nm wide top-gate stack was defined at the middle of the SWNT by EBL, 2-3nm Al_2O_3 (dielectric constant ~10) was deposited by ALD, followed by 15nm Al gate metal deposition and liftoff. (3) A layer of PMMA was spun on the device, followed by EBL to open a window on the S-side of the channel, leaving the other half covered (with p-type contact). N-type potassium doping was then done in vacuum for the exposed S side of the nanotube, completing the PIN configuration of the device (Fig.7a).

Fig. 7c shows the typical transfer characteristics of a SWNT P-I-N device. A -20V backgate bias is applied at all times to minimize the Schottky barrier and fully turn on the *p*-side (D side) of the device electrostatically. Fig. 7b shows the PIN device band diagrams at various top-gate voltages. At negative topgate biases, a tunnel barrier exists at the *n-i* junction, and carriers must tunnel through this barrier into the valence band for *p*-channel conduction. At positive top-gate biases, a tunnel-barrier exists at the *p-i* junction and tunneling into the conduction band of the nanotube affords *n*- channel conduction. When the top-gate bias is near zero, the Fermi levels of the *p*- and *n*-part of the nanotube is in the bandgap of the *i*-region, resulting in suppressed tunneling current for the off-state. Since conduction in a P-I-N device is via quantum mechanical tunneling, the subthreshold switching is no longer subject to the 60mV/dec MOSFET limit at room temperature. In our experiments, we observed SS<60mV/dec for 2-3 orders in a P-I-N device in both *p*- and *n*-sides of the subthreshold regions, and SS ~25mV/dec for about 2 orders. This to our knowledge was the first experimental realization of ambipolar SWNT P-I-N FETs with sub-60mV/dec.

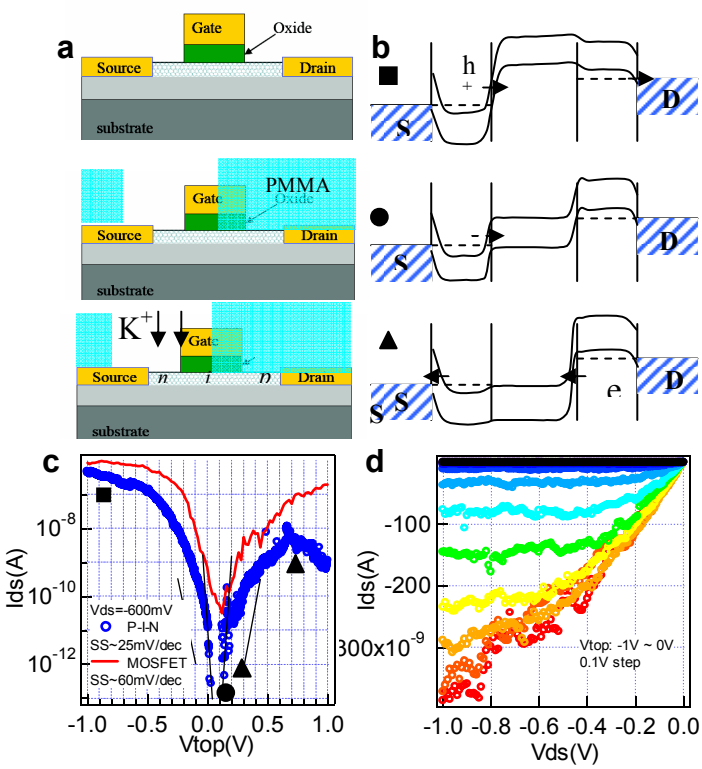

Figure 7. SWNT P-I-N tunnel FETs. (a) Schematic process flow and device structure. (b) Band diagrams for PIN operations at three different topgate regions marked in c. (c) Transfer characteristics of a SWNT PIN FET and MOSFET. Blue curve is for PIN, and the red curve is the same device before K doping. V_{ds} is 600mV for both curves. (d) I-V characteristics of the PIN FET. Topgate bias is from -1V to 0V at a step of 0.1V

For comparison, the behavior of the same device in the MOSFET configuration (before doping) is also shown in Fig. 7c with SS~60mV/dec. Unfortunately, the PIN does not exhibit a constant SS in the sub-threshold regions with SS ~ 25mV/dec over only 2-3 decades of current up to 15pA. The on currents of the tunnel devices are lower than those of SWNT MOSEFTs, limited by tunneling through the barriers. Very low off current can be obtained with PIN FETs due to negligible tunnel current through the ~200nm body barrier (in the *i*-region) in the off-state. Due to tunneling operation, SS for the PIN FET is nearly independent of temperature (Fig.8).

P-I-N-tunnel devices may be suitable for low power and wide temperature-range applications (14). In order to increase the on-current, it is necessary to form ultra-thin tunnel barriers since the on-current is exponentially dependent on the barrier width. One approach to this is to employ the thinnest possible dielectric layer for the top-gate stack. This will have the least fringing field effect and thus minimum tunnel barrier width. The SS value is affected by various factors in PIN FETs including phonon scattering. Phonon assisted tunneling may degrade SS according to simulation (15). To reduce phonon scattering, one could scale down the device to approach the electron-phonon scattering mean free path.

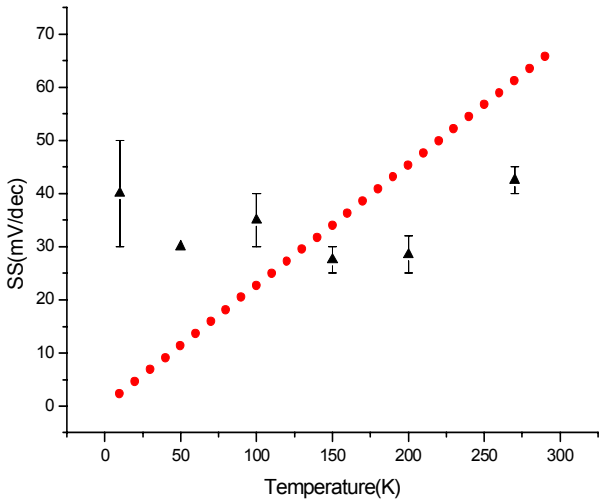

Figure 8. SS of a PIN device as a function of temperature (black symbols). Red circles are SS values expected for a MOSFET.

Conclusions

In summary, progress has been made in placing SWNTs on substrates by patterned growth and chemical assembly methods. Future effort will include patterning individual seed nanoparticles for aligned growth at near 100% yield. For both growth and assembly approaches, much effort is needed to control the pitch between nanotubes down to a few nanometers while maintaining parallel orientation. The diameter distribution of SWNTs needs to be narrowed and optimized for high performance FET applications. The optimum diameter of SWNTs for electronics applications should be in the 1.3-1.8nm range. Metallic vs. semiconducting nanotubes need to be either selectively grown or separated by chemical means with 100% efficiency. These challenges require much further effort. On the device side, novel tunnel devices of SWNTs can be obtained, although effort is needed in order to optimize the on current and obtain sub-60mV/decade SS over many decades of current.

Reference

(1) J. Kong, H. Soh, A. Cassell, et al., Nature **395**, 878 (1998).
(2) A. Javey and H. Dai, J. Am. Chem. Soc. **127**, 11942 (2005).
(3) Y. Zhang, et al., Appl. Phys. Lett. **79**, 3155 (2001).
(4) A. Ural, Y. Li, and H. Dai, Appl. Phys. Lett. **81**, 3464 (2002).
(5) S. Han, X. Liu, and C. Zhou, J. Am. Chem. Soc. **127**, 5294 (2005).
(6) M. S. C. Coskuns, J. Rogers, J. Am. Chem. Soc. **127**, 567 (2006).
(7) G. Y. Zhang, et al., PNAS **102**, 16141 (2005).
(8) Y. M. Li, et al., Nano Lett. **4**, 317-321 (2004).
(9) W. Kim, A. Javey, R. Tu, et al., Appl Phys Lett **87**, 1 (2005).
(10) A. Ulman, An Introduction to Ultrathin Organic Films: From Langmuir-blodgett to Self-Assembly; academic Press: Boston, 1991.
(11) *See* F. Kim, S, Kwan, J, Akana, P. D. Yang, J. Am. Chem. Soc., **123**, 4360 (2001); D. Whang, S. Jin, Y. Wu, C. M. Lieber, Nano Lett. **3**, 1255 (2003); S. Jin, D. Whang, M. C. McAlpine, R. S. Friedman, Y. Wu, C. M. Lieber, Nano Lett. **4**, 915 (2004).
(12) Y. Lu et al., J. Am. Chem. Soc. **128**, 3518 (2006).
(13) J. Appenzeller, et al., IEEE Trans. Elec. Dev. **52**, 2568 (2005).
(14) S. Koswatta et al., IEDM 518 (2005).
(15) S. Koswatta et al., Appl. Phys. Lett. **87,** 253107 (2005).