Performance Analysis and Design Optimization of Near Ballistic Carbon Nanotube Field-Effect Transistors

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ABSTRACT

A near ballistic carbon nanotube field-effect transistor (CNTFET) that integrates an ultra-short channel, low-barrier metal contacts, and a thin high-κ gate insulator is modeled and analyzed using self-consistent quantum simulations. Numerical simulations, which solve a quantum transport equation self-consistently with a 3D Poisson equation using the non-equilibrium Green's function (NEGF) formalism, are used to understand the transistor physics and to suggest design optimization. Important device issues of (1) how close the transistor operates to its ballistic limit, (2) What are the roles of phonon scattering and higher subband conduction, (3) how to further optimize the CNTFET, and (4) How the CNTFET compares to a state-of-the-art Si MOSFET, are explored and discussed.

INTRODUCTION

Carbon nanotube field-effect transistors (CNTFETs) have received much attention since the first demonstration in 1998 [1, 2]. Significant advances have been achieved in both understanding the transistor physics and improving device performance.

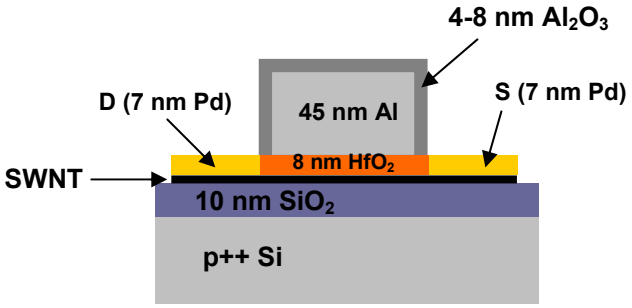

FIG. 1 A recently reported CNTFET with a 50nm-long channel and 7nm-thick Pd source/drain contacts [3]. The HfO_2 top gate insulator is 8nm-thick with a dielectric constant of $\kappa \approx 16$. The diameter of the intrinsic carbon nanotube channel is $d_{CNT} \approx 1.7$ nm.

A high performance CNTFET, which integrates a short (50nm-long) CNT channel, thin HfO_2 top gate insulator, and low-barrier metal source/drain contacts, has recently been demonstrated (Fig. 1) [3]. Due to the integration of short-channel, thin high-k top gate insulator, and a good S/D metal contact, the CNTFET demonstrates the best performance to date. A room-temperature channel conductance of $0.5 \times 4e^2/h$ and a source-drain current of ~20μA are achieved at $|V_G\text{-}V_T| \sim 1$V. The excellent performance and maturity of this CNTFET make a serious theoretical analysis important.

In this work, we examine device physics and suggest design optimization for the high-performance CNTFET by using self-consistent quantum simulations. An atomistic quantum transport equation is self-consistently solved with a 3D Poisson equation using the non-equilibrium Green's function (NEGF) formalism. The results are useful for understanding the device physics of near ballistic CNTFETs, and for identifying important issues to further improve CNTFET performance.

APPROACH

To analyze this experimental FET, we performed self-consistent quantum simulations. The Schrödinger equation was self-consistently solved using the non-equilibrium Green's function (NEGF) formalism with a three-dimensional (3D) Poisson equation. For the NEGF formalism, an atomistic, p_z orbital description for the entire carbon nanotube channel was used. The nanotube channel was treated as a ballistic conductor. All subbands that contribute to the charge and current in the channel are included. A phenomenological treatment of the metal contact was used, with the metal-CNT Schottky barrier height and a coupling parameter which controls the metal-induced-gap-states (MIGS) as input parameters [4]. This model describes the CNTFET operation as non-conventional metal source/drain transistors [5]. To determine the self-consistent potential, a 3D Poisson equation is solved using method of moments for the experimental geometry. A separate, semiclassical Monte Carlo simulation was used to explore the role of phonon scattering in CNTFETs under high bias.

ANANLYSIS of EXPERIMENT

Fig. 2 plots the experimental and simulated I-V characteristics. The parameters used in the simulation were obtained from an independent electrical characterization of the transistor [3]. There are two fitting parameters used in the simulation The first one is the transistor threshold voltage, which accounts for the uncertainty of the gate electrode work function, and possible existence of interface charges. The second one is the coupling parameter which controls the

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MIGS for a metal-CNT contact. The simulated I-V characteristics agree well with experimental measurement. Fig. 2a shows that the CNTFET displays both p-type and n-type conduction (ambipolar conduction), although the SB height for electrons is the whole band gap and the SB height for holes is 0. The minimal leakage current of the amibipolar I-V exponentially increases with the drain voltage increases. The reason for strong n-type conduction is (as pointed in Ref. [6] and [7]) that electrons tunnel through very thin SB at the drain end of the channel at high gate voltages. The SB thickness for electrons at high gate bias is controlled by the gate oxide thickness, which is very thin for this CNTFET. Furthermore, the small effective mass of electrons in CNTs facilitates the quantum-mechanical tunneling. Electrons with small effective mass can tunnel through a high yet thin SB at the drain end of the channel and form electron current at high gate voltages. As a result, the I-V for this high-performance transistor is ambipolar. Such ambipolar characteristics with a large leakage current are not desirable for conventional CMOS circuit applications. Design optimization, therefore, is needed to reduce the leakage, as will be discussed later.

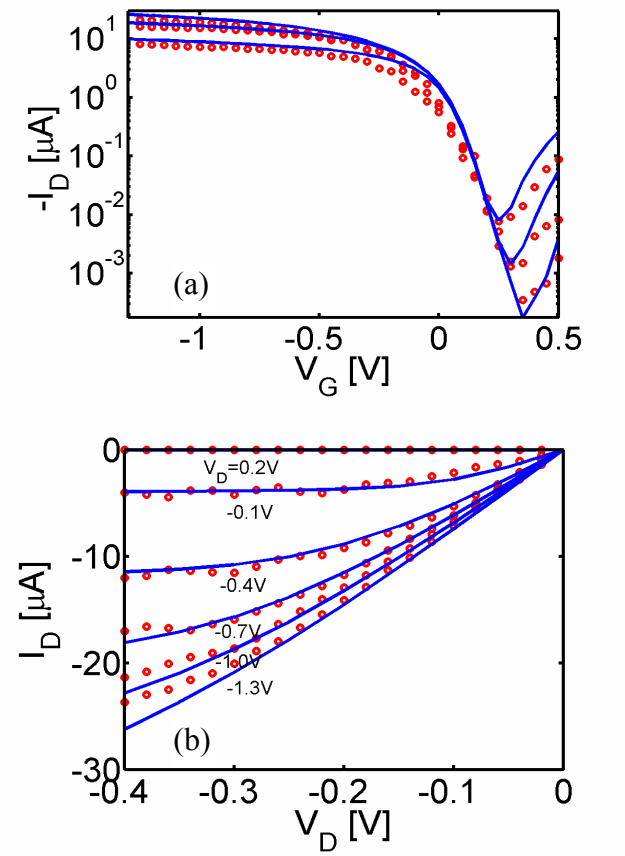

FIG. 2 (a) I_D vs. V_G characteristics at V_D=*-0.1, -0.2,* and *-0.3*V. (b) I_D vs. V_D characteristics at V_G=0.2 to -1.3V, -0.3V/step, for the CNTFET shown in Fig. 1 (circles: experiment, solid lines: simulations). For the simulated CNTFET, the Schottky barrier height for holes is $\phi_{bp} = 0$ and the tube diameter $d_{CNT} \approx 1.7$ nm. No interface and oxide charges are included. Only two fitting parameters are used in simulation as described in the text.

To explore how close the experimental FET operates to its ballistic limit, we simulated the I_D vs. V_G characteristics for a ballistic CNTFET with zero SB, $\phi_{bp} = 0$ [8], and zero parasitic source/drain resistance (the solid line). (Uncertainty of the metal-CNT Schottky barrier height, $0 < \phi_{bp} < 70meV$, remains, but the transistor I-V is insensitive to ϕ_{Bp} variation in a small range when the gate insulator of the high-performance CNTFET is thin [7].) Fig. 3 shows that experimental FET delivers close to 100% on-current of the ballistic current of the $\phi_{bp} = 0$ CNTFET. For ballistic FETs, a Schottky barrier FET will deliver less on-current than the corresponding MOSFET (a MOSFET behaves in many respects as a Schottky barrier FET with a negative barrier) [9]. Fig. 3 also shows that if a sufficiently negative barrier could be achieved (or, alternatively, if a CNT MOSFET could be produced) then the already high on-current could be doubled.

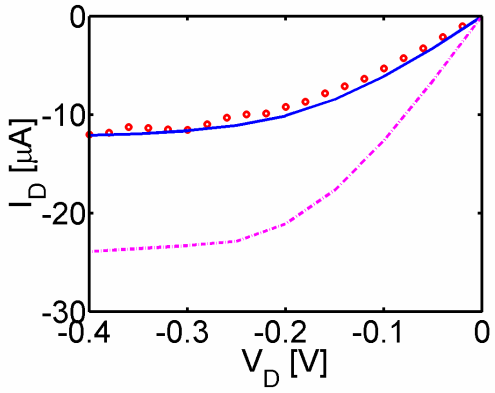

FIG.3 The experimental (circles) and simulated (solid and dash-dot lines) I_D vs. V_D at $V_G = -0.4V$. The solid line is simulated for a ballistic-channel CNTFET with a zero SB for holes ($\phi_{bp} = 0$). The dash-dot line simulated for a ballistic CNTFET with a sufficiently negative SB height $\phi_{bp} = -0.3eV$. The source/drain parasitic resistance $R_{S,D} = 0$ in simulations.

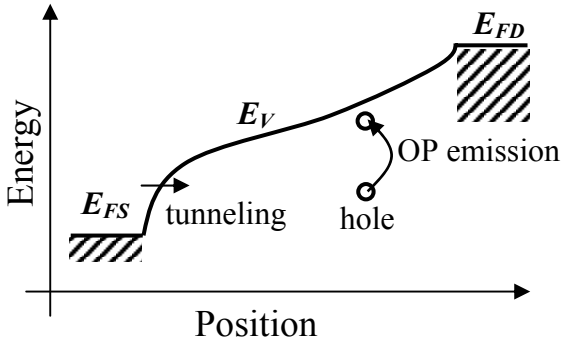

FIG.4 The valence band profile at on-state for a $\phi_{bp} = 0$ CNTFET. Acoustic phonon scattering has a long mean-free-path and thus a small effect on the source-drain current for a 50nm-channel-length CNTFET [10]. The source injected hole can emit an optical phonon with $\hbar\omega_{OP} \sim 0.16$ and get back scattered near drain, but the backscattered hole encounters a much thicker and higher SB and has little chance to return back to the source.

Figure 4 explains why scattering in the channel only has a small effect on the DC characteristics of the transistor. Phonon scattering is the most important scattering mechanism in high-quality, single-wall carbon nanotubes [10]. Acoustic phonon scattering has a long mean free path (~1μm) [10], therefore, it only has a small effect on the source-drain current for L_{ch}~50nm. Optical phonon (OP) scattering (with $\hbar\omega_{OP} \sim 0.16eV$) has a much shorter mean free path (~10nm) and scatters carriers even in a short channel [11]. Due to the short mean free path, the carrier can emit an OP near the drain end of channel as shown in Fig. 4. After OP emission, the backscattered hole encounters a much thicker and higher SB because lose of a large OP energy $\hbar\omega_{OP} \sim 0.16eV$. The back scattered hole has little chance to tunnel through the SB and return back to the source. Although OP emission scatters carriers near the drain end of the channel, it only has a small effect on the DC characteristics of the transistor.

We next explore the role of higher subband conduction. A previous study showed that for CNTFETs with heavily doped channel, several subbands conduct current at typical bias range [12]. To understand how many subbands deliver current for our CNTFET with an intrinsic tube channel, we plots the percentage of the 1st subband and 2nd subband current in the total current in Fig. 5. The contribution of total current from higher subbands is small (<10%) over the whole measured voltage range. The inset, which plots the 1st and 2nd subband profile at V_G=-1.3V, explains the reason. The SB for the 1st subband at both the source and drain contacts is zero and the SB for the 2nd subband is much higher (~0.25eV) due to the large subband spacing (~0.25eV) in a small diameter tube (d_{CNT}~1.7nm). Because the tunneling probability through a SB depends exponentially on the barrier height and thickness, the current of the 2nd subband is small compared to that of the 1st subband. As a result, the 1st subband conduction dominates for the analyzed experimental FET.

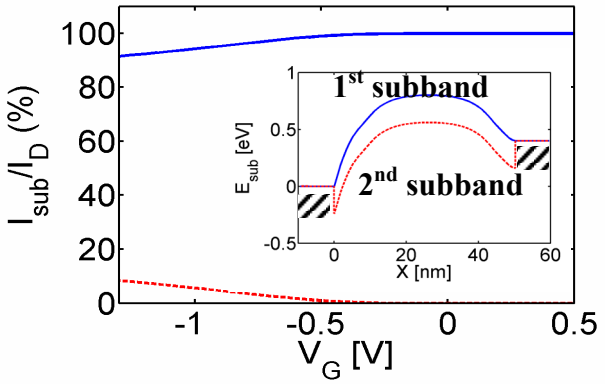

FIG.5 The percentages of the 1st (solid) and 2nd (dashed) subband currents in the total current vs. the gate voltage. The simulated SB height for holes is $\phi_{sp} = 0$ and the drain bias $V_D = -0.4$ V. The inset shows the valence band profile for the 1st and the 2nd subband at a large gate overdrive, $V_G = -1.3$ V.

DESIGN OPTIMIZATION

The performance of the experimental CNTFET can be further improved by design optimization. As shown in Fig. 6, the highest achievable on-off ratio for the experimental CNTFET at V_{DD} = 0.4V is only ~100, due to large leakage current caused by ambipolar conduction [6, 7]. The dashed lines show the I_D-V_G characteristics of a CNTFET with the following design optimizations: (1) using a smaller diameter (d_{CNT}~1.0nm) tube as the channel, (2) assuming that a zero SB can still be achieved even after a smaller diameter tube is used, (3) using a thinner HfO_2 top gate oxide, t_{top}=3nm, and (4) reducing the parasitic source/drain resistance to $R_{S,D}$<<1K Ω . The minimal leakage current can be greatly reduced and the maximum on-off current ratio can be significantly improved if a smaller diameter tube (which results in a larger band gap) is used. (Assuming, of course, that low barrier metal contacts can still be achieved.) In addition, the 8nm high-κ gate insulator is rather thick. Reducing the gate oxide thickness to 3nm improves the transconductance.

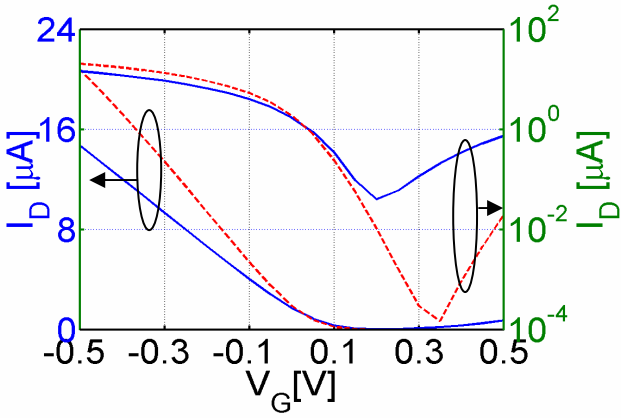

FIG. 6 I_D vs. V_G characteristics for the CNTFET in Fig. 1 (the solid lines) and for the projected optimized CNTFET (the dashed lines) on linear (the left axis) and log (the right axis) scales.

COMPARING Si MOSFETs and CNTFETs

As the performance of CNTFETs progresses, it is important to compare CNTFET performance to Si MOSFETs. A valid comparison requires us to: (1) assess transistor performance at the same power supply voltage, (2) include both the on-state and off-state performance, and (3) fairly compare device metrics for different channel geometries. Fig. 7 is an attempt to compare the state-of-the-art 130nm-node-technology Si MOSFETs with the gate length L_G=70nm [13] to our experimental CNTFET also with the same L_G=50nm [3]. Fig. 7a plots the transistor intrinsic delay τ vs. I_{ON}/I_{OFF} for both transistors, which is generated using the method described in Fig. 7b. For a specified power supply voltage V_{DD}, an on-current and off-current is obtained by reading the current

value at the edges of the gray window. The transistor intrinsic delay is computed as $\tau = C_G V_{DD} / I_{ON}$. For the Si MOSFET, the gate capacitance is obtained from the C-V measurement at inversion region. For the CNTFET, C_G is extracted from the slope of the charge on the tube (Q_{CNT}) vs. the top gate voltage (V_{top}) plot above V_t for a CNT capacitor with the same gate geometry as the experimental FET. A data point on the τ vs. I_{ON}/I_{OFF} plot is obtained. By assuming total control of the transistor threshold voltage, which corresponds to sweeping the gray window along the V_G axis (which corresponds to adjusting the transistor threshold voltage), a τ vs. I_{ON}/I_{OFF} curve is generated.

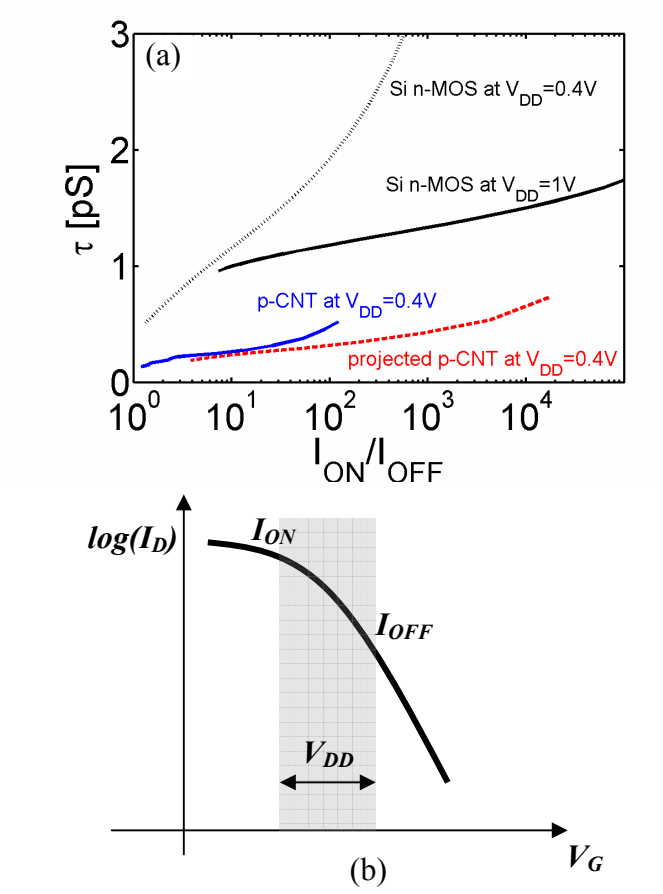

FIG.7 *Comparing CNTFETs to Si MOSFETs.* (a) The intrinsic transistor delay vs. the on-off ratio for a state-of-the-art, 130nm-node, Si n-type MOSFET [13] at the power supply voltage V_{DD}=1V (the solid line) and V_{DD}=0.4V (the dotted line), an experimental p-type CNTFET [3] at V_{DD}=0.4V, and a theoretically projected CNTFET described in Fig. 6 at V_{DD}=0.4V (the dashed line). The Si MOSFET has a gate length L_G~70nm and the CNTFETs has a L_G~50nm. (b) I_D vs. V_G characteristics of a p-type transistor, which shows how the curves in (a) are generated (see text).

We generated a τ vs. I_{ON}/I_{OFF} curve for each transistor involved in the comparison. The advantage of using τ and I_{ON}/I_{OFF} for comparison is that they don't depend on the channel geometry, and I_{ON}/I_{OFF} considers both the off and on states. The results show that for an on-off ratio of 100, the intrinsic delay of the CNTFET at V_{DD}=0.4V is about 1/2 of the Si MOSFET delay at V_{DD}=1V, and 3-4 times smaller than the Si FET delay at V_{DD}=0.4V. Fig. 7 also shows that if the optimized device could be realized, it would significantly extend the maximum achievable on-off ratio of the current experimental CNTFET, and display a considerable performance advantage over Si MOSFETs under low V_{DD} operation.

SUMMARY

A recently demonstrated CNTFET is analyzed in detail using self-consistent quantum simulations. The simulated I-V characteristics agree well with the experiment, which shows that the self-consistent quantum simulation captures the essential physics of the experimental CNTFET. The following results are obtained (1) The CNTFET delivers near ballistic current and OP emission only has a small effect on the DC current. (2) Conduction through the lowest subband dominates in the measured bias range. (3) Further performance improvement can be achieved by using a smaller diameter tube as the channel, scaling the thickness of the high-κ gate insulator, producing lower barrier contacts, and reducing the parasitic source/drain resistance. (4) A technique to fairly compare a CNTFET to a Si MOSFET is developed. The results show that the CNTFET outperforms the state-of-the-art Si transistor, in terms of the device delay, at a given on-off ratio.

ACKNOWLEDEGEMENT

The authors want to thank Prof. D. Antoniadis and O. Nayfeh of MIT for providing the Si MOSFET data in Fig. 7, S. Hasan, N. Neophytou, and S. Koswatta of Purdue for discussions. This work was supported by the NSF Network for Computational Nanotechnology (nCn), the MARCO Focused Research Center on Materials, Structures, and Devices, and the start-up fund for J. G. in the University of Florida.

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