Ultrathin-Body High-Mobility InAsSb-on-Insulator Field-Effect Transistors

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***Abstract*—Ultrathin-body InAsSb-on-insulator n-type field-effect transistors (FETs) with ultrahigh electron mobilities are reported. The devices are obtained by the layer transfer of ultrathin $InAs_{0.7}Sb_{0.3}$ layers (thickness of 7–17 nm) onto Si/SiO_2 substrates. InAsSb-on-insulator FETs exhibit an effective mobility of $\sim$3400 $cm^2/V \cdot s$ for a body thickness of 7 nm, which represents $\sim 2\times$ enhancement over InAs devices of similar thickness. The top-gated FETs deliver an intrinsic transconductance of $\sim$0.56 $mS/\mu m$ (gate length of $\sim$500 nm) at $V_{DS} = 0.5$ V with I_{ON}/I_{OFF} of 10^2–10^3. These results demonstrate the utility of the transfer process for obtaining high-mobility n-FETs on Si substrates by using mixed anion arsenide–antimonide as the active channel material.**

***Index Terms*—Field-effect transistors (FETs), InAsSb, ultrathin body (UTB), XOI.**

I. Introduction

HIGH-MOBILITY semiconductors show great promise as the channel material of ultrafast low-power field-effect transistors (FETs) and have been actively explored in the past few decades [1]–[4]. Among all known semiconductors, mixed anion $InAs_xSb_{1-x}$ has one of the highest electron mobilities and saturation velocities [5]. However, it also has one of the smallest bandgaps [5], [6]. For such devices, ultrathin-body (UTB) architectures are essential to enable acceptable leakage currents. Conventionally, $InAs_xSb_{1-x}$ devices have been fabricated as complex quantum well structures on III–V or Si substrates. While the devices exhibited promising initial results, due to leakage from gate and/or not fully depleted body, they suffered from high I_{OFF} [7]–[10]. In consideration of supporting substrates, Si is a well-established material and is highly preferred over III–V semiconductors. However, using direct MBE growth to integrate both n- and p-channel materials onto Si for CMOS will be very challenging due to the large lattice mismatch between different desired materials and Si/SiO_2. Previously, we demonstrated the transfer of InAs ultrathin membranes onto Si/SiO_2 substrates to form high-performance n-type FETs (n-FETs), termed "XOI" in analogy to the well-established silicon-on-insulator field. The mobility of InAs XOI devices was found to be as high as $\sim$5000 $cm^2/V \cdot s$ for body thicknesses of $\sim >$ 20 nm and decreases to $\sim$1600 $cm^2/V \cdot s$ when scaled down to 8 nm in thickness [11]. Here, we extend the XOI concept to $InAs_xSb_{1-x}$ as a demonstration of even higher mobility III–V FETs, particularly for UTB thicknesses of < 10 nm which are required for scaled transistors based on small-bandgap semiconductors.

II. Experiments

First, ultrathin $InAs_{0.7}Sb_{0.3}$ layers of different thicknesses ($T_{InAsSb} = 7$ and 17 nm) were transferred onto Si/SiO_2 substrates following the epitaxial layer transfer technique described previously [11]. $InAs_{0.7}Sb_{0.3}$ was grown on a 60-nm $Al_{0.4}Ga_{0.6}Sb$ sacrificial layer on a GaSb substrate by molecular beam epitaxy. The InAsSb layer was then pattern etched by using a mixture of citric acid (1 g/mL of water) and hydrogen peroxide (30%) at 1:20 volume ratio (etch rate of $\sim$0.7 nm/s), and the AlGaSb layer was selectively etched by ammonium hydroxide (1.5% in water). Ni ($T_{Ni} = 40$ nm) source (S) and drain (D) electrodes were fabricated using lithography and metallization. For top-gated FETs, a 10-nm-thick ZrO_2 gate dielectric was deposited by atomic layer deposition at 115 °C, followed by a forming gas anneal at 150 °C for 10 min. Subsequently, Ni top-gate (G) electrodes, overlapping the S/D, were fabricated. Fig. 1(a) shows a TEM image of the 7-nm InAsSb layer on Si/SiO_2 with a Ni/ZrO_2 high-κ stack, while the HRTEM image in Fig. 1(b) shows the single crystallinity of the InAsSb channel, exhibiting highly abrupt interfaces between InAsSb and Si/SiO_2 without any visible voids.

III. Results and Discussions

In order to probe the electrical properties of InAsSb XOI FETs, back- and top-gated devices with varied gate lengths (L_G) were fabricated and characterized. For back-gated FETs, 50-nm-thick thermally grown SiO_2 was used as the gate

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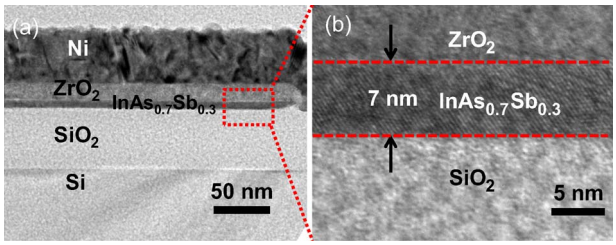

Fig. 1. (a) TEM image of an ∼7-nm-thick $InAs_{0.7}Sb_{0.3}$ XOI (body oxide thickness of 50 nm) substrate. The nanoribbon is coated with a ZrO_2/Ni bilayer (∼25 and ∼50 nm, respectively). (b) HRTEM image showing the single-crystal structure of an $InAs_{0.7}Sb_{0.3}$ nanoribbon with atomically abrupt interfaces with ZrO_2 and SiO_2 layers on the top and bottom surfaces, respectively.

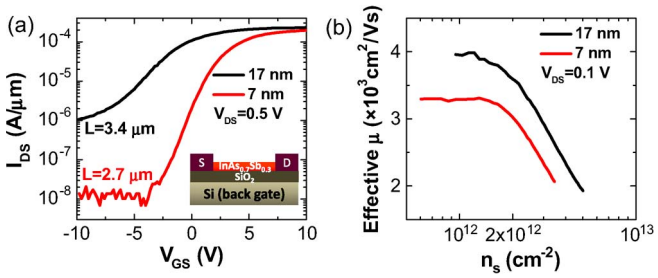

Fig. 2. (a) Typical back-gate I_{DS}–V_{GS} for 7- and 17-nm-thick $InAs_{0.7}Sb_{0.3}$ XOI n-FETs on 50-nm SiO_2 at $V_{DS} = 0.5$ V. The inset shows the schematic of the back-gated devices. (b) Effective mobility extracted from I_{DS}–V_{GS} characteristics at $V_{DS} = 0.1$ V.

dielectric. Fig. 2(a) shows the transfer characteristics of the 7- and 17-nm-thick InAsSb XOI FETs at $V_{DS} = 0.5$ V, for $L_G = 2.7$ and 3.4 μm, respectively. The back-gated 7-nm-thick device exhibits an I_{ON}/I_{OFF} ratio of $\sim 10^4$, which is more than two orders of magnitude greater than that of the 17-nm device. This significant improvement in OFF current can be attributed to better electrostatic control from gating a thinner body [12]. The raising of bandgap by confinement will also contribute to a lower OFF current, since the barrier for thermionic emission of carriers would be higher. Specifically, since InAsSb has a large Bohr radius (between 34 and 65 nm, which are for bulk InAs and InSb, respectively [13]), heavy quantum confinement is expected in UTB membranes. An approximate expression for the ground-state energy of electrons and holes can be derived by solving the 1-D Schrodinger equation for a finite potential well. The effective bandgaps would be 0.6 and 0.32 eV for 7- and 17-nm $InAs_{0.7}Sb_{0.3}$, respectively. Fig. 2(b) shows the extracted effective mobilities (μ_{eff}) as a function of the 2-D carrier density at $V_{DS} = 0.1$ V for the long-channel back-gated FETs (with $T_{ox} = 50$ nm) shown in Fig. 2(a). The mobility was obtained from the expression

$$\mu_{\text{eff}} = \frac{\partial I_{DS}}{\partial V_{DS}} \frac{L_G}{C_{ox}(V_G - V_T - 0.5V_{DS})}$$

where V_T is the threshold voltage extracted from the linear I_{DS}–V_{GS} curve and $C_{ox} = \varepsilon_{ox}\varepsilon_0/T_{ox}$ is the gate oxide capacitance per unit area ($\varepsilon_{ox} \sim 3.9$ is the dielectric constant of SiO_2, ε_0 is the vacuum permittivity, and $T_{ox} = 50$ nm is the SiO_2 thickness). Here, we utilized the simple parallel-plate model, and the effects of quantum capacitance and fringe field are ignored, which is a valid assumption given the thick gate oxide (i.e., small oxide capacitance) of the back-gated devices and that the channel width is much greater than thickness.

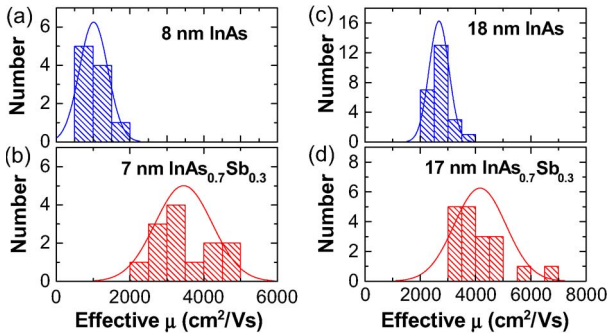

Fig. 3. Histogram plots of effective mobility (at $n_s = 2 \times 10^{12}$ cm^{-2}) in InAs and InAsSb XOI n-FETs of (a) $T_{InAs} = 8$ nm, (b) $T_{InAs0.7Sb0.3} = 7$ nm, (c) $T_{InAs} = 18$ nm, and (d) $T_{InAs0.7Sb0.3} = 17$ nm.

The effective mobility histograms extracted for long-channel $InAs_{0.7}Sb_{0.3}$ (thicknesses of 7 and 17 nm) and InAs (thicknesses of 8 and 18 nm) XOI FETs are shown in Fig. 3. Note that the dimensions (including channel width W, which is *typically* ∼320–380 nm) of each device were directly measured by SEM and used to normalize the current and extract the mobilities. InAsSb devices exhibit average effective mobilities of ∼3400 and ∼4100 cm^2/V · s at $n_s = 2 \times 10^{12}$ cm^{-2} for the 7- and 17-nm thicknesses, respectively. Note that the mobility degradation with thickness is mainly due to enhancement of surface roughness and surface polar phonon scattering [14]. These mobility values present ∼2× enhancement over InAs XOI FETs with similar thicknesses (Fig. 3). The variation of the mobility may be caused by the different amount of interface trap states (D_{it}) introduced during processing. This mobility improvement coincides with the previously reported Hall mobility difference between $InAs_{0.7}Sb_{0.3}$($\mu_{\text{Hall}} \sim 42\,000$ cm^2/V · s) and InAs ($\mu_{\text{Hall}} \sim 22\,000$ cm^2/V · s) [15] at a doping concentration of 5×10^{16}–3×10^{17} cm^{-3}, which is around the electron density in our unintentionally doped samples. Hence, it is promising to further enhance the mobility by increasing the Sb content of the channel, although this comes at the cost of a lower bandgap.

Next, the electrical properties of top-gated InAsSb XOI FETs are explored. As shown in Fig. 4(a) and (b), a 7-nm-thick InAsSb FET ($L_G = 500$ nm) exhibits $I_{ON}/I_{OFF} \sim 2 \times 10^2$ when defining I_{OFF} at $V_T - 1/3V_{DD}$ and I_{ON} at $V_T + 2/3V_{DD}$ at room temperature (V_T is taken at $I = 10^{-6}$ A/μm) and exhibits an I_{ON} of ∼0.38 mA/μm at $V_{DS} = V_{GS} = 0.6$ V. A subthreshold swing of $SS \sim 178$ mV/dec is obtained, which is larger than that of InAs FETs ($SS \sim 125$ mV/dec) [16]. This suggests that the InAsSb interfaces exhibit a higher density of trap states than InAs. The source contact resistance R_S of the 7-nm-thick InAsSb was extracted using the transmission line method. The extracted R_S is ∼200 Ω · μm, which is close to that of the 8-nm InAs FETs (∼230 Ω · μm) [16].

The extrinsic transconductance g_m of the top-gated FET ($L_G \sim 500$ nm) at $V_{DS} = 0.5$ V peaked at ∼ 0.51 mS/μm. The intrinsic transconductance

$$g_{\text{mi}} = g_m/(1 - g_m R_S - g_d R_{SD})$$

was extracted to exclude the contact resistance effects ($R_{SD} = R_S + R_D = 2R_S$). The peak intrinsic transconductance of the device is ∼0.56 mS/μm. Fig. 4(c) shows g_m and g_{mi} as a

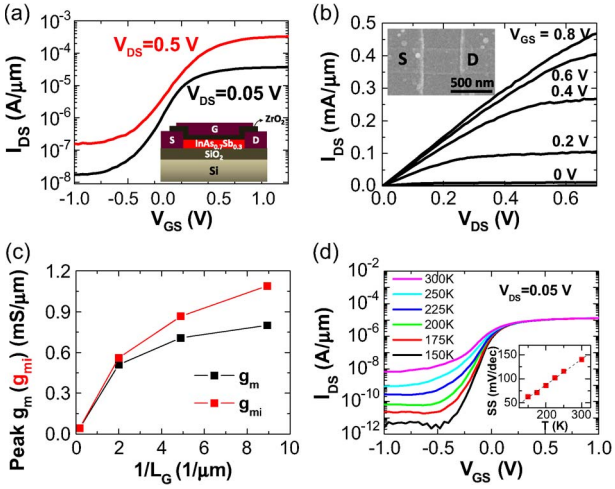

Fig. 4. (a) Top-gate $I_{\rm DS}$–$V_{\rm GS}$ for a 7-nm-thick $InAs_{0.7}Sb_{0.3}$ XOI n-FET at $V_{\rm DS} = 0.05$ and 0.5 V. The gate length is ∼500 nm. Inset shows schematic of top-gated InAsSb XOI FETs. (b) $I_{\rm DS}$–$V_{\rm DS}$ curve of the same device in (a). Inset shows the top-view SEM image (false color) of a representative device. (c) g_m and $g_{\rm mi}$ as a function of the gate length. (d) Top-gate $I_{\rm DS}$–$V_{\rm GS}$ as a function of temperature at $V_{\rm DS} = 0.05$ V. Inset shows SS as a function of T, with linear fitting.

function of inverse gate length, which exhibits nonlinearity for shorter channel lengths, possibly arising from quasi-ballistic transport. Further study needs to be done to improve the $I_{\rm OFF}$ and SS of sub-500-nm-channel-length devices. Compared to previously reported $InAs_{0.8}Sb_{0.2}$ QWFETs ($L_G = 1$ μm and $g_{\rm mi} = 0.50$ mS/μm) on GaAs substrates and InSb QWFETs ($L_G = 85$ nm and $g_{\rm mi} = 0.71$ mS/μm) on Si, our InAsSb XOI FETs show a peak $g_{\rm mi}$ of ∼0.56 mS/μm for $L_G \sim 500$ nm [Fig. 4(c)] while eliminating the complexity from growing thick buffer and δ doping layers [9], [10]. Moreover, it has higher $I_{\rm ON}/I_{\rm OFF}$ at room temperature.

Fig. 4(d) shows the temperature-dependent transfer characteristics. The interface trap density ($D_{\rm it}$) was extracted from $D_{\rm it} = C_{\rm it}/q^2$, with $C_{\rm it}$ from

$$\frac{dSS}{dT} = \frac{2.3k}{q}\left(1+\frac{C_{\rm it}}{C_{\rm ox1}}+\frac{C_{\rm InAsSb}}{C_{\rm ox1}}-\frac{\frac{C_{\rm InAsSb}^2}{C_{\rm ox1}C_{\rm ox2}}}{1+\frac{C_{\rm it}}{C_{\rm ox2}}+\frac{C_{\rm InAsSb}}{C_{\rm ox2}}}\right).$$

With $\varepsilon_{\rm ox1} = 16$, $t_{\rm ox1} = 10$ nm, $\varepsilon_{\rm ox2} = 3.9$, $t_{\rm ox2} = 1200$ nm, $\varepsilon_{\rm InAsSb} = 15.7$, and $t_{\rm InAsSb} = 7$ nm, $D_{\rm it}$ is determined to be $\sim 1 \times 10^{13}$ cm^{-2}eV^{-1}, which is slightly higher than that of InAs XOI FETs ($\sim 3 \times 10^{12}$ cm^{-2}eV^{-1}) [16]. Note that this $D_{\rm it}$ value presents only a rough estimate of the order of magnitude for the average trap density within the bandgap. The traps close to or beyond the conduction band edge are not extracted using this analysis technique, but they can also alter the charge carrier density and transport properties. Detailed capacitance–voltage characterization in the future is needed to better understand and optimize the surface/interface properties.

IV. Conclusion

In conclusion, high-electron-mobility $InAs_{0.7}Sb_{0.3}$ transistors have been fabricated on Si substrates using the XOI configuration. The devices exhibit excellent electrical properties, while future work on improving the InAsSb/high-κ interface needs to be done. In the future, even higher Sb content and thinner body InAsSb XOI n-FETs, together with InGaSb XOI p-FETs, are promising to be integrated for high-speed and low-power complementary MOSFET circuits.

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H. Fang and S. Chuang contributed equally to this work.

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