Chem Soc Rev

RSC Publishing

TUTORIAL REVIEW

Carbon nanotube electronics – moving forward†

Chuan Wang,[ab] Kuniharu Takei,[ab] Toshitake Takahashi[ab] and Ali Javey*[ab]

Cite this: *Chem. Soc. Rev.*, 2013, **42**, 2592

Single-walled carbon nanotubes (SWNTs) possess fascinating electrical properties and offer new entries into a wide range of novel electronic applications that are unattainable with conventional Si-based devices. The field initially focused on the use of individual or parallel arrays of nanotubes as the channel material for ultra-scaled nanoelectronic devices. However, the challenge in the deterministic assembly has proven to be a major technological barrier. In recent years, solution deposition of semiconductor-enriched SWNT networks has been actively explored for high performance and uniform thin-film transistors (TFTs) on mechanically rigid and flexible substrates. This presents a unique niche for nanotube electronics by overcoming their limitations and taking full advantage of their superb chemical and physical properties. This review focuses on the large-area processing and electronic properties of SWNT TFTs. A wide range of applications in conformal integrated circuits, radio-frequency electronics, artificial skin sensors, and displays are discussed – with emphasis on large-area systems where nm-scale accuracy in the assembly of nanotubes is not required. The demonstrations show SWNTs' immense promise as a low-cost and scalable TFT technology for nonconventional electronic systems with excellent device performances.

Received 9th August 2012

DOI: 10.1039/c2cs35325c

www.rsc.org/csr

1. Introduction

Single-walled carbon nanotubes (SWNTs) can be considered as monolayer graphene sheets with a honeycomb structure that are rolled into seamless, hollow cylinders. Owing to their small size (diameter around 1–2 nm), as well as their superior electronic properties without surface dangling bonds, SWNTs hold great potential for a wide range of applications in solid-state devices and are envisioned as one of the promising candidates for beyond-silicon electronics. SWNTs can be categorized by their chiral vectors defined on the hexagonal crystal lattice using two integers (m and n). The chiral vectors correspond to the direction along which a graphene sheet is wrapped to result in a SWNT. The electronic properties of SWNTs heavily depend on their chiral vectors and the SWNTs can be either metallic ($m = n$ or $m - n$ is a multiple of 3) or semiconducting (all other cases).[1–4] Using this rule of thumb, one can infer from the possible (n, m) values that one third of SWNTs are metallic and the other two thirds are semiconducting. For practical use as the active channel component of electronic devices, semiconducting SWNTs are commonly used. The advantages of semiconducting SWNTs over other conventional semiconductors are multifold. First of all, the charge carriers in carbon nanotubes have long mean free paths, on the order of a few hundred nanometers for acoustic phonon scattering mechanism. As a result, scattering-free ballistic transport of carriers at low electric fields can be achieved in carbon nanotubes at moderate channel lengths (*e.g.*, sub-100 nm).[5] Second, the carrier mobility of semiconducting nanotubes is experimentally measured to be >10 000 $cm^2\ V^{-1}\ s^{-1}$,[6,7] at room temperature which is higher than the state-of-the-art silicon transistors. Finally, their small diameters enable excellent electrostatics with efficient gate control of the channel for highly miniaturized devices. Thereby, SWNTs have stimulated enormous interest in both fundamental research and practical applications in nano- and macro-electronics.

Researchers have previously demonstrated excellent field-effect transistors (FETs)[5,8–12] and integrated circuits[13–17] using individual SWNTs. Fig. 1a and b depict the transfer (I_{DS}–V_{GS}) and output (I_{DS}–V_{DS}) characteristics of the state-of-the-art individual SWNT-FET with self-aligned source/drain contacts and near ballistic transport.[11] Impressive performance with sub-threshold slope (SS) of 110 mV dec^{-1}, on-state conductance of $0.5 \times 4e^2\ h^{-1}$ and saturation current up to 25 μA per tube (diameter ~ 1.7 nm) has been achieved in devices with channel lengths down to 50 nm.[11] Better SS of ~70 mV dec^{-1}, which is close to the theoretically limit of 60 mV dec^{-1}, has also been achieved in transistors with slightly longer channel lengths (500 nm).[10]

[a] *Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA*

[b] *Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA. E-mail: ajavey@eecs.berkeley.edu*

† Part of the chemistry of functional nanomaterials themed issue.

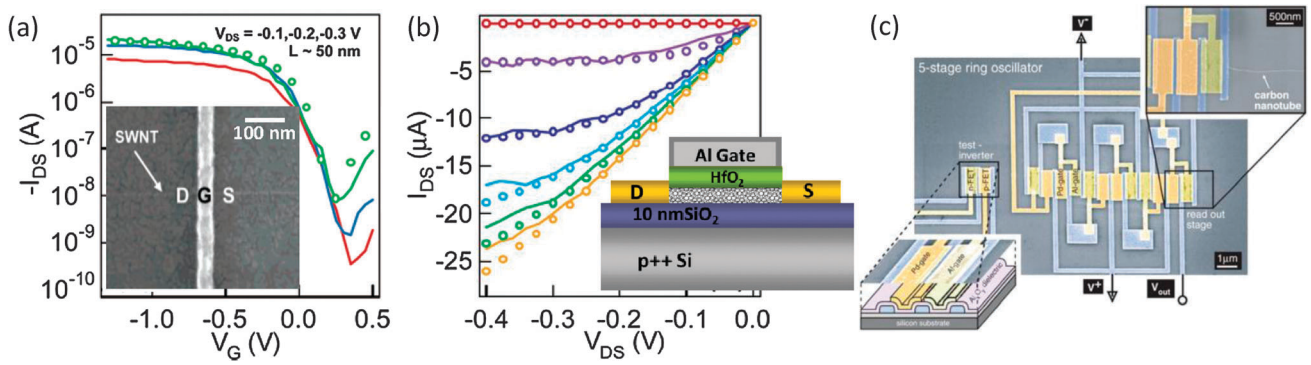

Fig. 1 State-of-the-art individual SWNT transistors and circuits. (a) I_{DS}–V_{GS} characteristics of a self-aligned ballistic SWNT-FET with a channel length of 50 nm. Inset: SEM image of the device. (b) Experimental (solid line) and simulated (open circle) I_{DS}–V_{DS} characteristics of the same device shown in panel (a). Inset: Schematic of the device. Reproduced with permission from ref. 11 (Copyright 2004 American Chemical Society). (c) SEM image of a 5-stage ring oscillator constructed on an individual SWNT. Reproduced with permission from ref. 16 (Copyright 2006 The American Association for the Advancement of Science (AAAS)).

More recently, SWNT-FETs with sub-10 nm channel lengths have been demonstrated.[12] Such devices exhibit an impressive SS of 94 mV dec^{-1}, current on/off ratio of 10^4, and on-current density of 2.41 mA μm^{-1}, which outperform silicon FETs with comparable channel length. Using SWNT-FETs, integrated circuits with various functionalities have been demonstrated. Notable examples include a 5-stage ring oscillator (Fig. 1c) and pass-transistor-logic-based integrated circuits (full adder, multiplexer, decoder, D-latch, *etc.*).[16,17]

Despite the tremendous progress made with individual nanotube transistors and circuits, major technological challenges remain, including the need for deterministic assembly of nanotubes on a handling substrate with nm-scale accuracy, minimal device-to-device performance variation, and development of a fabrication process scalable and compatible with industry standards. Hence, the use of carbon nanotubes for nanoelectronic applications is still long from being realized. On the other hand, the use of SWNT networks, especially based on semiconductor-enriched samples, present a highly promising path for the realization of high performance thin-film transistors (TFTs) for macro- and flexible electronic applications. The most significant advantages of using SWNT *random* networks for TFTs lie in the fact that the SWNT thin-films are mechanically flexible, optically transparent, and can be prepared using solution-based room temperature processing, all of which cannot be provided by amorphous and poly silicon technologies.[18–20] Compared with organic semiconductors,[21–25] the other competing platform for flexible TFTs, the SWNT thin-films offer significantly better carrier mobility (~2 orders of magnitude improvement). Thereby, large-area TFT applications seem to offer an ideal niche for carbon nanotube based electronics, taking advantage of their superb physical and chemical properties without being hindered from their precise assembly limitations down to the nm-scale.

Numerous research efforts have been devoted to the successful realization of large-scale chemical vapor deposition (CVD) growth of high-density horizontally aligned SWNTs on single crystal quartz or sapphire substrates.[26–34] Transfer techniques have been further developed, enabling the demonstration of high-performance transistors and integrated circuits using the aligned nanotubes on various types of rigid and flexible substrates.[35–42] However, considering the fact that roughly one third of the as-grown nanotubes are metallic, techniques such as electrical breakdown[43] are necessary to remove the leakage-causing metallic paths, which adds complexity, is not scalable, and significantly degrades the device performance due to the high applied fields during the process. Preferential growth of aligned semiconducting SWNTs has been reported recently,[32,44,45] which is an important step forward; however, the purity is not yet high enough to achieve transistors with high on/off current ratio (I_{on}/I_{off}) for digital applications. Therefore, for the purpose of obtaining devices with better I_{on}/I_{off}, it is more attractive to have networks of SWNTs with higher percentage of semiconducting tubes and/or with random orientation where individual nanotubes do not directly bridge the source/drain electrodes, thereby minimizing the metallic pathways.[46–50]

Fig. 2 illustrates the most common assembly methods for random nanotube networks including direct CVD growth,[51,52] dry filtration,[53] evaporation assembly,[54] spin coating,[55–57] drop coating,[58–63] and printing.[64–68] CVD-grown nanotube networks have been widely explored for TFTs (Fig. 2a) and medium scale flexible integrated circuits have been demonstrated by Rogers *et al.*[51] For this method, metal catalysts are typically deposited on the entire substrate using either evaporation or spin coating methods followed by CVD growth using hydrocarbon precursors such as methane, ethylene, ethanol, methanol *etc.* Despite the tremendous success in making flexible nanotube TFTs and circuits with promising electrical performance, the drawback is the existence of metallic nanotubes, which degrades the current on/off ratio of the devices. Although stripe-patterning (Fig. 2a right panel) has been proposed to improve the device on/off ratio by cutting the percolative transport through metallic paths in the transistors,[51] the channel length needs to be made relatively large in this case, limiting the degree of integration in the future. The dry filtration method (Fig. 2b) has been used by Ohno and co-workers to achieve high-performance flexible nanotube TFTs and D-flip-flop circuits.[53] In this method, SWNTs grown by plasma enhanced CVD are captured using a filter membrane and the density of the nanotubes can be easily

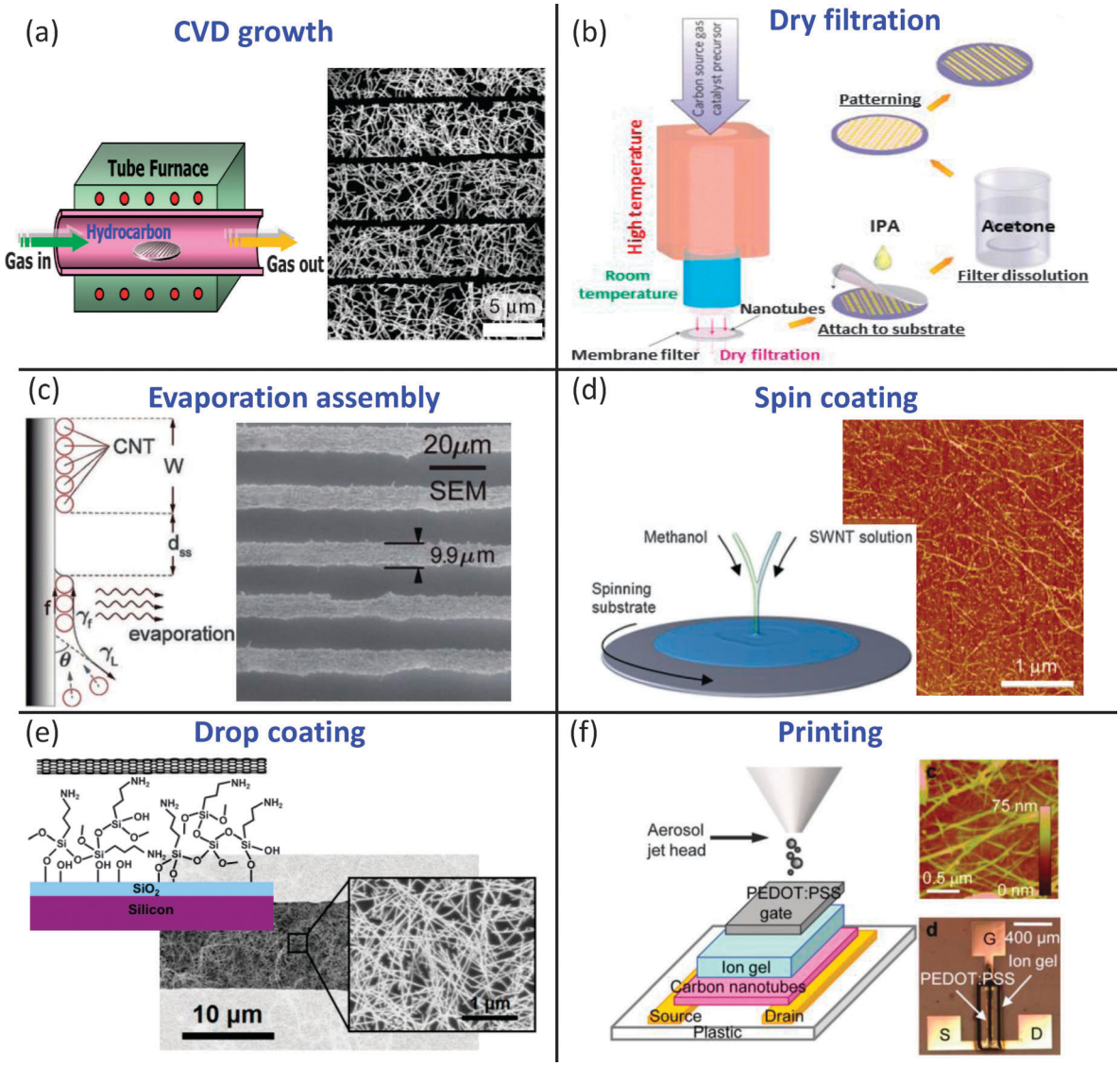

Fig. 2 Different methods used for assembling SWNT networks. (a) CVD growth. Reproduced with permission from ref. 51 (Copyright 2008 Nature Publishing Group). (b) Dry filtration. Reproduced with permission from ref. 53 (Copyright 2011 Nature Publishing Group). (c) Evaporation assembly. Reproduced with permission from ref. 54 (Copyright 2008 American Chemical Society). (d) Spin coating. Reproduced with permission from ref. 55 (Copyright 2004 American Chemical Society). (e) Drop casting. Reproduced with permission from ref. 59 (Copyright 2009 American Chemical Society). (f) Printing. Reproduced with permission from ref. 64 (Copyright 2010 American Chemical Society).

controlled by the collection time. The collected nanotube networks can be subsequently transferred to fabrication substrates by dissolving the filter using acetone. The IBM group used a novel evaporation assembly method to obtain aligned nanotube strips with high purity semiconducting nanotubes (Fig. 2c).[54] Although submicron devices with good performance have been achieved, the scalability of this assembly method can be a potential problem. SWNT networks can also be obtained by dropping the nanotube solution onto a spinning substrate (Fig. 2d).[55] The drawback with this method is also scalability because the deposited SWNTs often align along different orientations depending on the location on the substrate, preventing wafer-scale fabrication with high uniformity. The other two solution-based SWNT assembly methods – drop coating (Fig. 2e) and printing (Fig. 2f) – are found to be more promising for large scale applications of nanotube TFTs. For the drop coating method, the substrates are first functionalized with amine-containing molecules, which are effective adhesives for SWNTs. By simply immersing the substrate into the nanotube solution, highly uniform nanotube networks can be obtained throughout the wafer, enabling the fabrication of nanotube TFTs with high yield and small device-to-device variation.[59,60,62,63] Printing (Fig. 2f) represents another low-cost approach for fabricating large-scale nanotube TFTs and circuits where the SWNT channel, electrodes, and gate dielectric can all be printed using ink-jet[64,65] or gravure printing[66–68] processes. This approach is useful for making cost-effective large-area nanotube circuits requiring only moderate performance as the resolution that can be

achieved using the printing process is generally lower than the conventional photolithography. Each of these methods discussed above presents unique opportunities and challenges. In this review paper, we primarily focus on the use of semiconductor-enriched SWNT random networks. We will first discuss the assembly techniques for high density and uniform SWNT networks, and fabrication schemes for large-area, high-performance TFTs on mechanically rigid and flexible substrates. Electrical properties study and performance benchmarking are also discussed in detail. Lastly, we review a wide range of potential applications for SWNT TFTs in integrated circuits, radio-frequency electronics, artificial skin sensors, and displays.

2. Solution-processed TFTs using high purity semiconducting SWNTs

2.1 Nanotube separation and TFT fabrication

As discussed above, one of the major challenges limiting the electronic applications of SWNTs is the coexistence of metallic and semiconducting nanotubes, with roughly one third of the as-grown being metallic. The metallic SWNTs cause significant leakage of current when the transistors are in the off state, and thus need to be selectively removed. As a result, high-purity semiconducting SWNTs have long been desired in order to facilitate high I_{on}/I_{off}. To address this problem, many groups have been actively working on nanotube separation based on electronic types. Hersam *et al.* proposed and demonstrated the use of density gradient ultracentrifugation (DGU) to achieve diameter,[69] electronic type,[70] or even chirality-based[71] separation. By mixing the pristine unsorted SWNTs with surfactants, a density gradient between metallic and semiconducting SWNTs is created and upon ultracentrifugation, the metallic and semiconducting nanotubes are separated from each other as shown in Fig. 3a. In the photograph of the test tube, the brown band contains primarily semiconducting nanotubes and the green band contains mainly metallic ones. The high purity semiconducting and metallic nanotubes are further evidenced by the UV-Vis-NIR absorption spectra. Noteworthily, the semiconductor-enriched

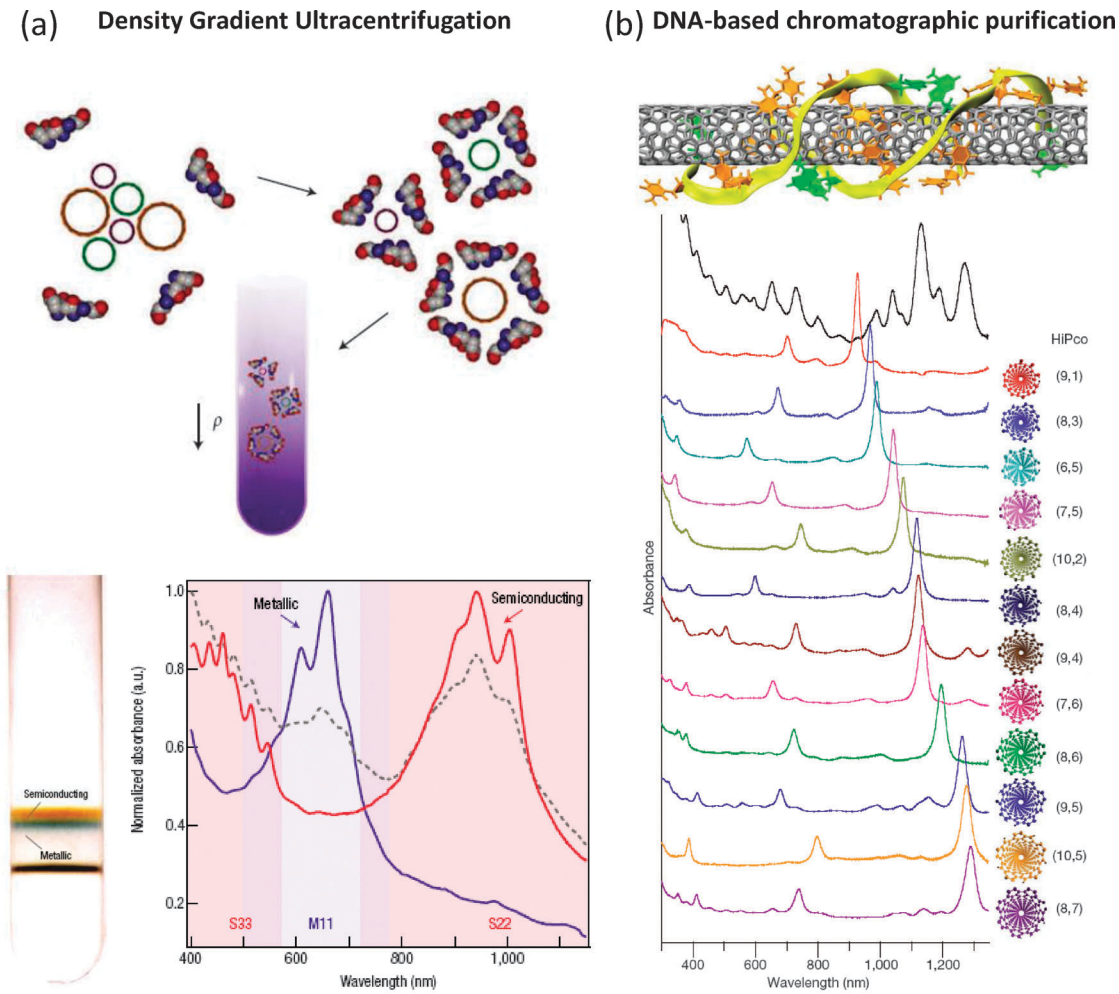

Fig. 3 (a) A density gradient between metallic and semiconducting SWNTs is created by mixing the pristine SWNTs with surfactants. Upon ultracentrifugation, the metallic and semiconducting nanotubes can be separated from each other as shown in the UV-Vis-NIR absorption spectra. Reproduced with permission from ref. 70 (Copyright 2006 Nature Publishing Group). (b) SWNTs with different chiralities can be separated by chromatographic purification by using DNA with different sequence motifs. Reproduced with permission from ref. 72 (Copyright 2009 Nature Publishing Group).

nanotubes are now commercially available, which makes it easy for research groups worldwide to explore device applications based on this purified material system. Even with high purity semiconducting nanotubes, there are still many different possible chiralities, and thus different bandgaps. This factor can negatively affect the device performance and uniformity. In order to achieve chirality-specific purification of SWNTs, DNA modification with different sequence motifs have been used and purified SWNTs with different chiralities have been obtained using chromatographic purification (Fig. 3b).[72]

Solution-based deposition of the above-described high purity semiconducting nanotubes at macro scales has been reported.[59,60,62,63] Most commonly, the substrates are first functionalized with amine-containing molecules or polymers such as aminopropyltriethoxysilane (APTES)[59,60] or poly-L-lysine[62,63] whose molecular structures are shown in Fig. 4a. By dipping the substrate into APTES or poly-L-lysine, amine-terminated layers are formed on the SiO_2 surface which works as an effective adhesive layer for SWNTs (Fig. 4b). The amine-functionalized substrate is subsequently immersed into high-purity (up to 99%) semiconducting nanotube solution followed by de-ionized (DI) water and isopropanol rinse, and blown dry in nitrogen. Using the method described above, highly uniform SWNT random networks can be achieved at a full wafer-scale. As shown in Fig. 4c, the scanning electron microscopy (SEM) images taken at different locations on a 3-inch Si/SiO_2 wafer indicate that uniform nanotube deposition is achieved. The importance of substrate functionalization is clearly illustrated in Fig. 4d and e. From the images, one can find that the samples with (Fig. 4d) and without (Fig. 4e) an adhesion layer exhibit rather drastic difference in terms of nanotube density and surface coverage.

Using the solution-deposited semiconductor-enriched nanotube thin-films, high performance TFTs can be fabricated on both rigid and flexible substrates. A schematic illustration of a representative fabrication process is shown in Fig. 5a. For the device fabrication on flexible substrates, polyimide is commonly explored, which can be spin coated and cured on a silicon handling wafer.[62,63] Polyimide is a high temperature plastic, allowing the dielectric layer and other passive components

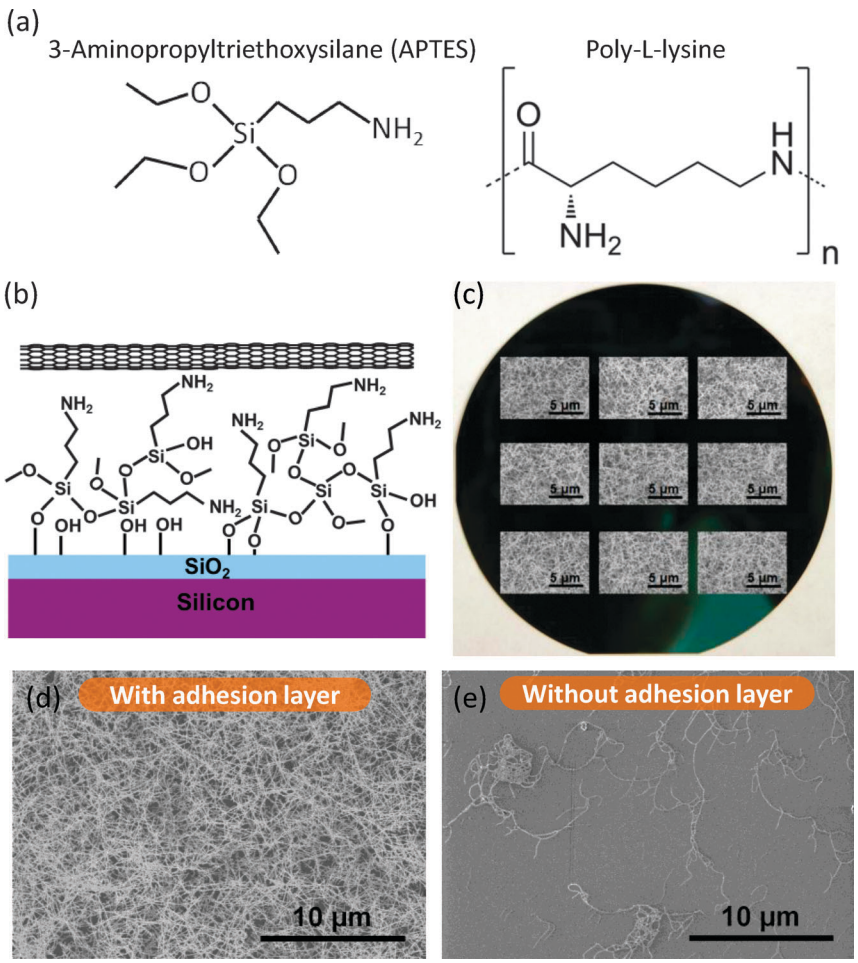

Fig. 4 (a) Molecular structure of adhesive layers commonly used for large-scale semiconducting nanotube network deposition. (b) Schematic diagram of APTES-assisted nanotube deposition on the Si/SiO_2 substrate. (c) SEM images showing that highly uniform nanotubes are deposited at different locations on a 3 inch Si/SiO_2 wafer. (d, e) SEM images of semiconducting nanotube networks deposited on Si/SiO_2 substrates with (d) and without (e) APTES functionalization. Reproduced with permission from ref. 59 (Copyright 2009 American Chemical Society).

to be deposited at temperatures as high as 300 °C. The rest of the fabrication process which typically involves gate formation, dielectric deposition, nanotube deposition, source/drain formation, and unwanted nanotube etching is universal for both the rigid and flexible platforms.[60,63] Atomic layer deposition (ALD) is used to deposit high-κ oxide layers such as Al_2O_3, HfO_2 or ZrO_2 as the gate dielectric. For the back-gated device geometry, a thin layer (thickness ~2 nm) of SiO_x is often evaporated on top of the high-κ gate dielectric to facilitate a more efficient deposition of SWNTs on the substrate using the amine chemistry described above. In order to precisely define the active channel region, photolithography and oxygen plasma are used to etch away the unwanted nanotubes. For flexible TFTs, the polyimide layer is peeled off from the silicon handling wafer once the fabrication is complete, leaving behind the high performance devices on an extremely bendable plastic substrate. A representative schematic diagram and corresponding SEM and atomic force microscopy (AFM) images of fully-fabricated nanotube TFTs on Si/SiO_2 and flexible polyimide substrates are shown in Fig. 5b[60] and c,[63] respectively. From both SEM and AFM images, one can find that the channel consists of high density, uniform SWNT networks, which is critical for achieving uniform device and circuit performance.

2.2 Electrical characteristics

The electrical properties of the SWNT networks have been systematically studied to evaluate the feasibility of using such a material system for high-performance TFTs. First of all, the device characteristics of SWNT TFTs are found to heavily depend on the nanotube density.[61,62] By controlling the duration of nanotube deposition, the density of the network can be controlled as shown in Fig. 6.[62] Fig. 6a shows the AFM images of the semiconducting nanotube networks formed after different durations of deposition, showing the monotonic increase of nanotube density from ~30 to 65 tubes μm^{-2} as the deposition time is increased from 5 to 90 minutes.[62] The I_{DS}–V_{GS} characteristics for the devices made with different nanotube densities are shown in Fig. 6b. Based on the results, histograms of the extracted device on/off current ratio (I_{on}/I_{off}) and unit-width (W) normalized transconductance (g_m/W) are presented in Fig. 6c and d. According to these figures, one can find that as the nanotube density increases (*i.e.*, longer deposition time),

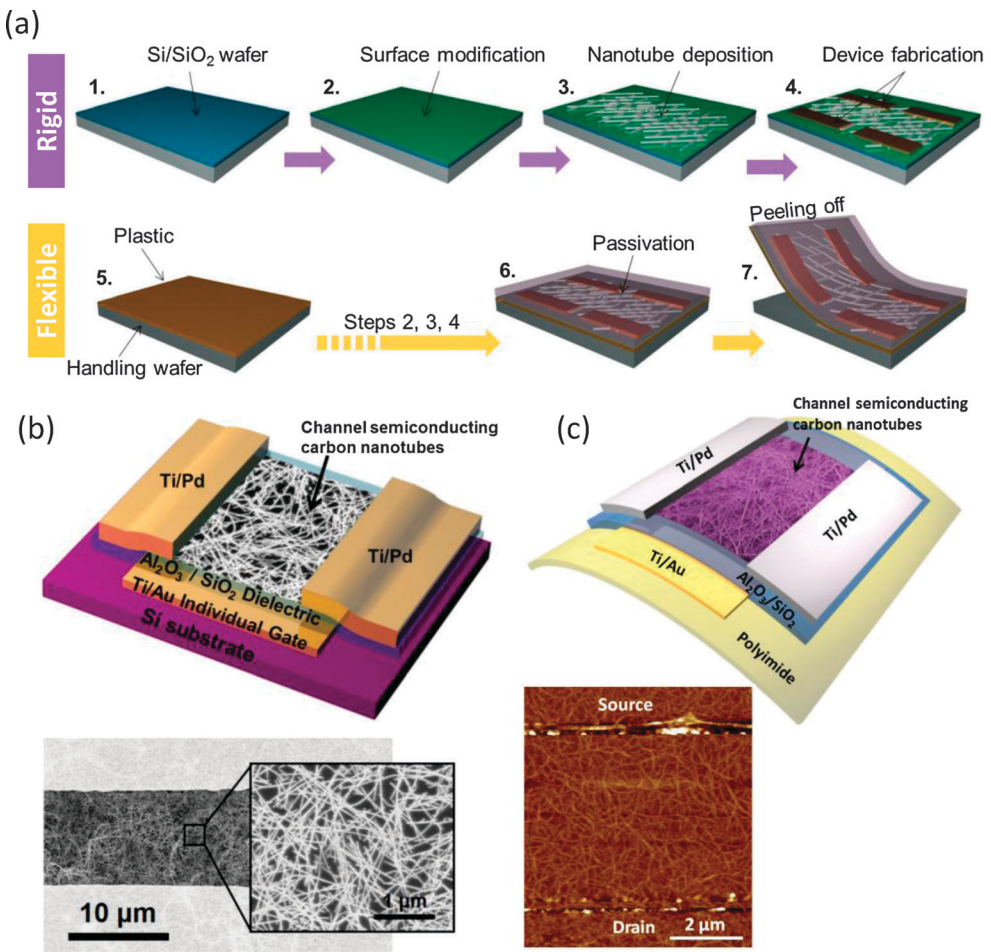

Fig. 5 (a) Schematic illustration showing the fabrication of semiconducting nanotube TFTs on rigid and flexible substrates. (b) Schematic diagram and SEM image of a TFT made on a Si/SiO_2 substrate. Reproduced with permission from ref. 60 (Copyright 2010 American Chemical Society). (c) Schematic diagram and AFM image of a TFT made on a flexible polyimide substrate. Reproduced with permission from ref. 63 (Copyright 2012 American Chemical Society).

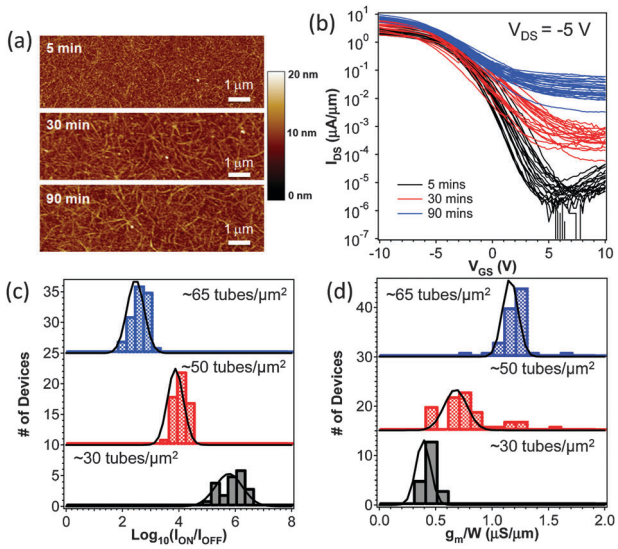

Fig. 6 (a) AFM images showing semiconducting nanotube networks formed after different durations of solution deposition. (b) I_{DS}–V_{GS} characteristics of semiconducting nanotube TFTs with different nanotube densities obtained by different deposition times. (c, d) Histogram showing the distribution of the on/off current ratio (c) and unit-width normalized g_m (d) for TFTs with different nanotube densities. Reproduced with permission from ref. 62 (Copyright 2011 American Chemical Society).

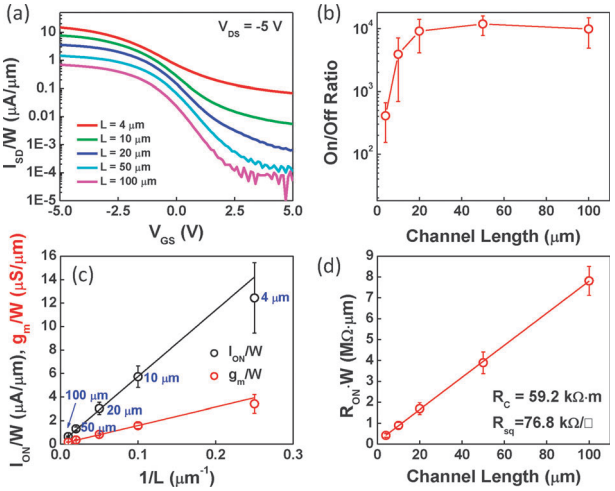

Fig. 7 (a) I_{DS}–V_{GS} characteristics of flexible nanotube TFTs with various channel lengths (4, 10, 20, 50, and 100 μm) measured at $V_{DS} = -5$ V. (b) Plot of I_{on}/I_{off} as a function of channel length for $V_{DS} = -5$ V. (c) I_{on}/W at $V_{GS} = -5$ V and peak g_m/W as a function of $1/L$ for $V_{DS} = -5$ V. (d) Normalized on-state resistance at $V_{GS} = -5$ V as a function of the channel length. Reproduced with permission from ref. 63 (Copyright 2012 American Chemical Society).

the g_m/W improves while the I_{on}/I_{off} decreases. This trade-off needs to be taken into consideration when optimizing the device performance for different types of applications. For example, high I_{on}/I_{off} is generally desired for digital logic applications in order to minimize the static power consumption, so it is preferred to use TFTs with lower nanotube density. On the other hand, for high-speed analog or radio-frequency (RF) applications where g_m is most important, the use of higher density nanotube networks is more beneficial. The lower I_{on}/I_{off} for high nanotube density networks arises from the higher probability of a direct metallic path between source/drain electrodes given that ~1% of the commercially available semiconductor-enriched nanotubes are still metallic. Furthermore, clear bundling of nanotubes is observed for longer deposition times (Fig. 6a) which may also contribute to the OFF state current. In the future, the use of higher semiconductor-enriched solutions can further improve the I_{off} for the same I_{on}. Importantly, the gate control of the random network is clearly strong, arising from the small overall thickness of the network (on the order of a few nm). This is an important feature of the devices, owing to the small diameter of SWNTs.

The scaling properties of the semiconducting nanotube TFTs have also been systematically investigated in ref. 63. Fig. 7a shows the I_{DS}–V_{GS} characteristics of representative devices with channel lengths from 4 to 100 μm measured at $V_{DS} = -5$ V, from which the device figures of merit such as on-current density (I_{on}/W), g_m/W, and I_{on}/I_{off} are extracted and plotted as a function of channel length (L). Fig. 7b indicates that as the channel length increases from 4 to 100 μm, the average on/off current ratio undergoes significant improvement from ~400 to 10 000, which can be attributed to the decrease in the probability of percolative transport through the metallic nanotubes. For devices with shorter L that is comparable to the length of the SWNTs used for the study (~1 to 2 μm), the probability of metallic impurities directly bridging the source/drain gets significantly higher, resulting in lower I_{on}/I_{off}. Fig. 7c shows that the I_{on}/W and g_m/W (at $V_{DS} = -5$ V) of the devices are roughly proportional to $1/L$, consistent with the conventional MOSFET device models and indicating good uniformity of the transistors. For such solution-processed nanotube TFTs, I_{on}/W and g_m/W as high as 15 μA μm^{-1} and 4 μS μm^{-1} have been achieved with L = 4 μm and $V_{DS} = -5$ V. Interestingly, Fig. 7b and c reveal a similar trade-off between on-current, transconductance, and on/off ratio. The results indicate that for a given nanotube density, longer channel length (*e.g.* 10 μm) is preferred for digital logic circuits, while smaller channel length (<4 μm) should be chosen for analog and RF applications. Furthermore, in order to the extract the contact resistance, the normalized on-state resistance (R_{on} W) is plotted as a function of L as shown in Fig. 7d. From the y-axis intercept divided by 2, a contact resistance (R_c) of ~59 kΩ μm is extracted. It is worth noting that this R_c value is relatively high because for the nanotube network transistors only a fraction of the contact area is active for a given unit width. In the future, improving the nanotube density could help to further reduce the overall contact resistance. Nevertheless, the R_c value reported here is low enough for the long channel devices often explored in TFT applications, where the channel resistance is the dominant resistance component.

2.3 Field-effect mobility

In order to fairly benchmark the performance of SWNT TFTs with other technologies, it is important to examine the

field-effect carrier mobility. Carrier mobility is a measure of how fast the charge carriers can travel within the semiconductor material under an electric field. It directly relates to the I_{on}, g_m, and maximum operating speed of the transistors, especially at relatively longer channel lengths where the devices operate in the diffusive regime, and is widely used as a figure of merit for benchmarking semiconductor materials. By knowing the gate capacitance (C_{ox}) and the extracted g_m/W, the field-effect device mobility of the nanotube TFTs can be derived using the following relation:

$$\mu_{device} = \frac{L}{V_d C_{ox} W}\frac{dI_d}{dV_g} = \frac{L}{V_d C_{ox}}\frac{g_m}{W}$$

In order to accurately assess the mobility, it is important to directly measure the C_{ox} of the devices. Most published works have relied on either the parallel plate model[53] or a more rigorous analytical cylindrical model by considering the electrostatic coupling between the nanotubes.[73] Using the parallel plate model, the C_{ox} would be overestimated, leading to lower extracted device mobility. The analytical model offers better accuracy. However, due to the uncertainty in quantifying the density and diameter for a random network containing hundreds of thousands of SWNTs, the extracted device mobility can still have large uncertainty, depending on the density and diameter values used in the calculations.

Recently, capacitance–voltage (C–V) measurements have been used to directly measure the gate capacitance of the nanotube network TFTs.[51,63] The C–V measurement setup is illustrated in Fig. 8a,[63] where the gate of the transistor is connected to the HIGH terminal and the source and drain are both connected to the LOW terminal of the C–V analyzer (Agilent B1500A). This measurement set-up is similar to the commonly explored technique for the C–V analysis of ultrathin body Si devices. TFTs with slightly underlapped gate are chosen in order to minimize the effect of the parasitic capacitances (Fig. 8b). The C–V characteristics of devices with different L are measured under a moderate frequency of $\sim$100 kHz and the C_{ox} values in the accumulation region ($V_{GS} = -5$ V) are extracted (Fig. 8c). By using devices of different size, the C_{ox} per unit area can be accurately evaluated from the slope of the linear fit and the field-effect mobilities can be derived using the relation described above. According to Fig. 8d, one can find that the parallel plate model (blue trace) indeed underestimates the mobility while the analytical model (red trace) overestimates it. The actual device mobility (green trace) for the solution-processed SWNT network is extracted to be $\sim$50 cm^2 V^{-1} s^{-1} for 98% semiconducting nanotubes with a density of $\sim$40 tubes μm^{-2}. This is close to the device mobility of low-temperature polysilicon (LTPS)[19] and significantly better than amorphous silicon[18] and organic semiconductors.[22–25] The fact that such an impressive mobility can be achieved in devices made using a facile solution-based process makes the nanotube TFTs ideal for a wide range of applications.

2.4 N-type nanotube TFTs

For digital logic applications, it is desirable to have complementary metal-oxide semiconductor (CMOS) operation since it gives rail-to-rail swing, large noise margin, and small static

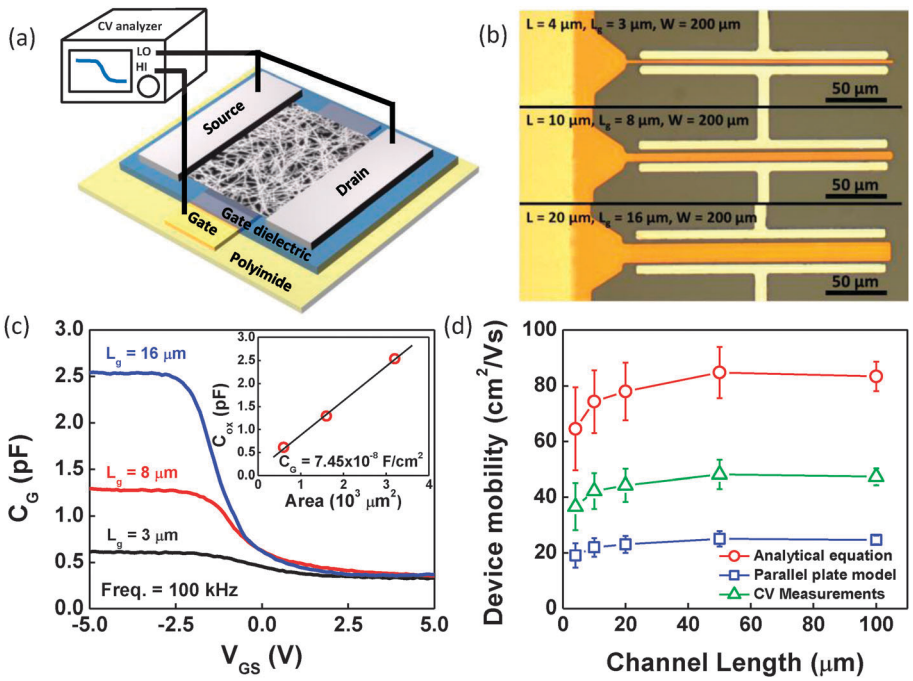

Fig. 8 (a) C–V measurement setup used to extract the gate capacitance of nanotube TFTs. (b) Optical microscope images of the underlapped gated devices used for the C–V measurements and C_{ox} extraction. (c) C–V characteristics of the nanotube TFTs measured at 100 kHz. Inset: C_{ox} as a function of the channel area. (d) Field-effect mobility of the semiconducting nanotube TFT as a function of the channel length. Reproduced with permission from ref. 63 (Copyright 2012 American Chemical Society).

power consumption. The CMOS operation requires a pull-up network consisting of p-type transistors and a pull-down network consisting of n-type transistors. Such circuit configuration ensures that the pull-up and pull-down networks cannot be turned on simultaneously, thereby preventing direct current flow from power supply to ground and reducing the static power consumption. Although the CMOS design is widely adopted in silicon-based technologies, it is not straightforward to realize in the SWNT-based platform. As-fabricated nanotube transistors typically exhibit p-type behavior in ambient environments due to the lower Schottky barrier heights for holes at the nanotube/metal interfaces for most air-stable metal contacts. In order to convert the nanotube FETs into n-type, many approaches have been reported in the literature including thermal or electrical annealing in vacuum to desorb O_2 from the metal contacts and thereby lower their work function,[14,15] surface chemical doping,[74–76] electrostatic gating,[77] and metal contact engineering.[78–80] In order to down-select the most practical n-doping method for SWNT TFT integrated circuits, major factors to be considered include air-stability, and process reliability and uniformity. Although promising methods such as using low work function metal contacts (Sc, Y, or Gd) have been reported for obtaining air-stable n-type SWNT FETs, such methods have not yet been proven to be effective for TFTs with random networks of SWNTs, especially when high device uniformity over large area is required.

Fig. 9 illustrates two air-stable methods used to obtain high-performance n-type carbon nanotube TFTs. In ref. 81, passivation of the nanotube TFTs with high-κ dielectric layer such as HfO_2 deposited by atomic layer deposition (ALD) was proposed (Fig. 9a) to convert the devices into n-type. The n-type devices obtained using this approach exhibit symmetric electrical performance compared with their p-type counterparts in terms of on-current, on/off ratio, and device mobility (Fig. 9b). The mechanism of the carrier type conversion has been attributed to the desorption of moisture and oxygen from the metal contacts during the vacuum baking process in the ALD chamber as well as the deficiency of oxygen atoms in the HfO_2 layer deposited at elevated temperatures. This introduces positive fixed charges into the high-κ oxide layer and efficiently shifts the I_{DS}–V_{GS} characteristics of the device from p- to n-type. Chemical doping was also used to demonstrate air-stable nanotube TFTs.[82] In this method, viologen was deposited onto the nanotube networks in the channel using inkjet printing (Fig. 9c) and TFTs with n-type transfer characteristics were achieved. Using both methods, CMOS inverters with high gain have been demonstrated.

It should be noted that despite the success, the reproducibility and uniformity of the n-FETs are still not as good as their p-type counterparts. Therefore, further study is needed to develop n-type TFT platforms with industry standard reproducibility for complex CMOS applications.

2.5 Frequency response

Due to the extremely high carrier mobility[6,7] and ballistic transport,[5] carbon nanotubes hold great potential for applications in RF electronics.[83–87] The frequency response of transistors using networks of high-purity semiconducting nanotubes

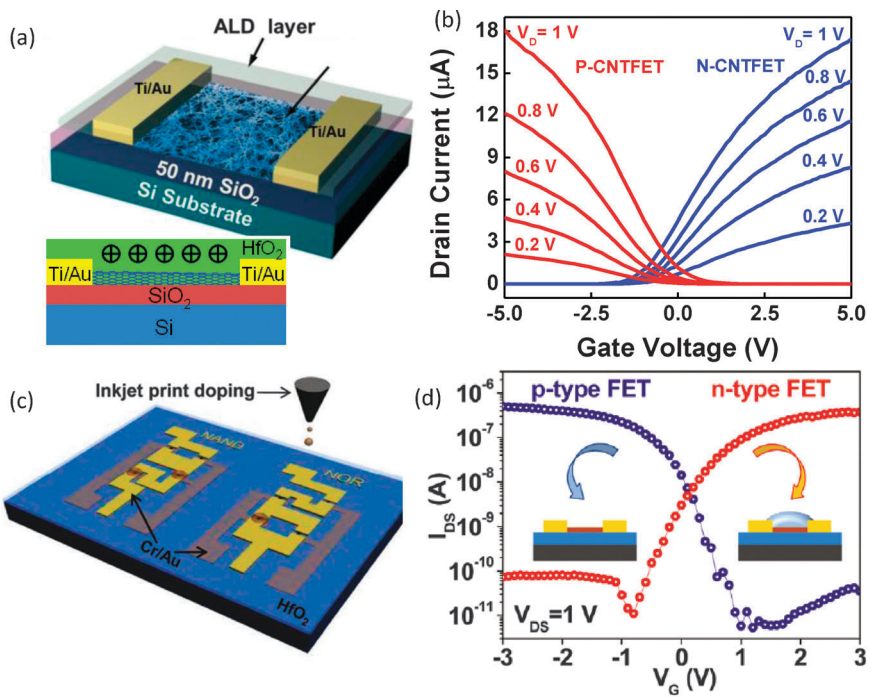

Fig. 9 (a) Air-stable n-type semiconducting nanotube TFTs obtained using ALD HfO_2 passivation. (b) Symmetric I_{DS}–V_{GS} characteristics have been achieved for the n- and p-type TFTs using the ALD passivation technique. Reproduced with permission from ref. 81 (Copyright 2011 American Chemical Society). (c) Air-stable n-type semiconducting nanotube TFTs obtained using surface chemical doping (viologen). (d) I_{DS}–V_{GS} characteristics before and after the viologen doping. Reproduced with permission from ref. 82 (Copyright 2011 American Chemical Society).

have been characterized[63,87] for potential use in wireless communication applications.

The common figures of merit used to determine the maximum operating speed of a transistor technology include current gain cutoff frequency (f_t) and maximum oscillation frequency (f_{max}), which correspond to the highest frequencies that the transistors can operate with current gain or power gain greater than 1, respectively. In order to extract f_t and f_{max} of the transistors, microwave measurements have been performed using devices configured into the ground-signal-ground (GSG) coplanar waveguide structures (Fig. 10a and e).[63,87] According to the relation $f_t = g_m/(2\pi(C_{gs} + C_{gd}))$, higher g_m and smaller parasitic capacitances lead to better frequency response. For this reason, RF devices are typically designed to have slightly underlapped or self-aligned gate structures in order to minimize the parasitic capacitances.

I_{DS}–V_{GS} and I_{DS}–V_{DS} characteristics of representative RF nanotube transistors with a channel length of ~4 μm on a flexible substrate[63] are presented in Fig. 10a and b. The S-parameters, measured using a vector network analyzer (VNA) from 10 MHz to 1 GHz, are plotted in Fig. 10c. Using the measured S-parameters, the current gain (h_{21}) and maximum available gain (G_{max}) can be deduced as shown in Fig. 10d. The results are de-embedded using on-chip open and short structures in order to remove the parasitic effects from the probing pads. The f_t and f_{max}, which are defined as the frequency where the h_{21} and G_{max} become 0 dB, are found to be ~170 and 118 MHz for transistors with 4 μm channel length (Fig. 10d). This performance is impressive considering the relatively long channel length used and the fact that such devices are fabricated on a mechanically flexible substrate. Such performance is also significantly better than organic semiconductor TFTs whose operating speed typically lies in the range of kHz or lower.

By scaling down the channel length, even faster transistors can be obtained due to the improvement of g_m. RF transistors

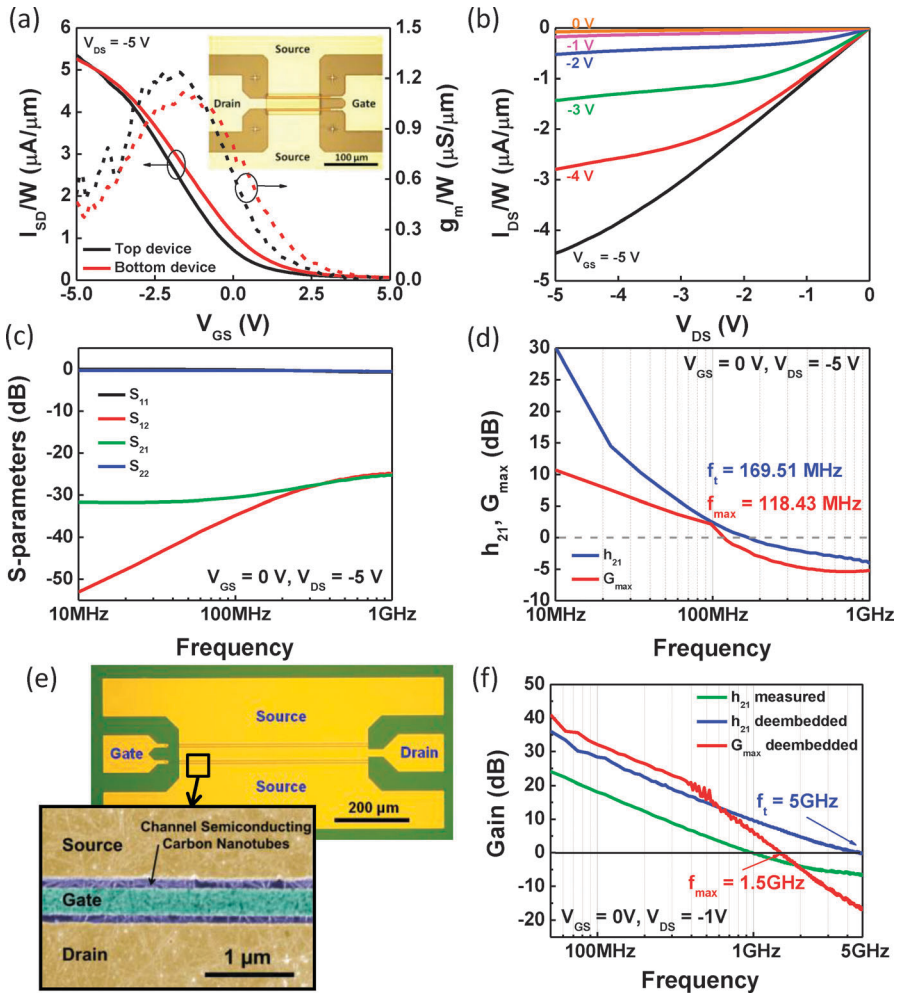

Fig. 10 (a) Transfer characteristics of a pair of nanotube RF transistors with L = 4 μm, L_g = 3 μm, and W = 100 μm, measured at V_{DS} = −5 V. Inset: Optical microscopy image of the corresponding device. (b) Output characteristics of the same device shown in panel (a). (c) Measured S-parameters for the flexible nanotube RF transistor from 10 MHz to 1 GHz. (d) De-embedded current gain h_{21} and maximum available gain G_{max} of a device showing a f_t of 170 MHz and a f_{max} of 118 MHz. Reproduced with permission from ref. 63 (Copyright 2012 American Chemical Society). (e) Optical micrograph and SEM image (inset) of a submicron nanotube RF transistor with L = 500 nm. (f) De-embedded h_{21} and G_{max} obtained from the measured S-parameters of the submicron nanotube RF transistor. The f_t is extracted to be 5 GHz at V_{DS} = −1 V. Reproduced with permission from ref. 87 (Copyright 2011 American Chemical Society).

using solution-processed semiconducting nanotube networks with channel lengths down to 500 nm (Fig. 10e) have been obtained on Si/SiO_2 substrates.[87] Impressive f_t of ~5 GHz was achieved at a low operating voltage (V_{DD}) of 1 V. This result highlights the practical use of SWNT TFTs for wireless applications.

3. Applications of solution-processed carbon nanotube TFTs

3.1 Integrated circuits

The solution-processed nanotube TFTs offer a wide range of potential applications such as bendable integrated circuits,[51,53,60,63] active-matrix backplanes for tactile sensors[62] and display electronics,[88] and conformal electronics.[62] First, we review the progress made on bendable integrated circuits made using nanotube TFTs. Because the p-FET platform is currently more mature with higher reliability and uniformity, a PMOS design with resistive load or diode-load is commonly adopted.

Mechanically flexible logic gates such as inverter, 2-input NAND, and NOR have been demonstrated using SWNT TFTs as shown in Fig. 11.[63] The voltage transfer characteristics (VTC) of a diode-loaded inverter are shown Fig. 11b. Respectable voltage gain of ~30 at V_{DD} = 5 V, symmetric input/output behavior (*i.e.* single V_{DD} operation), and rail-to-rail swing have been successfully achieved. The above characteristics enable cascading

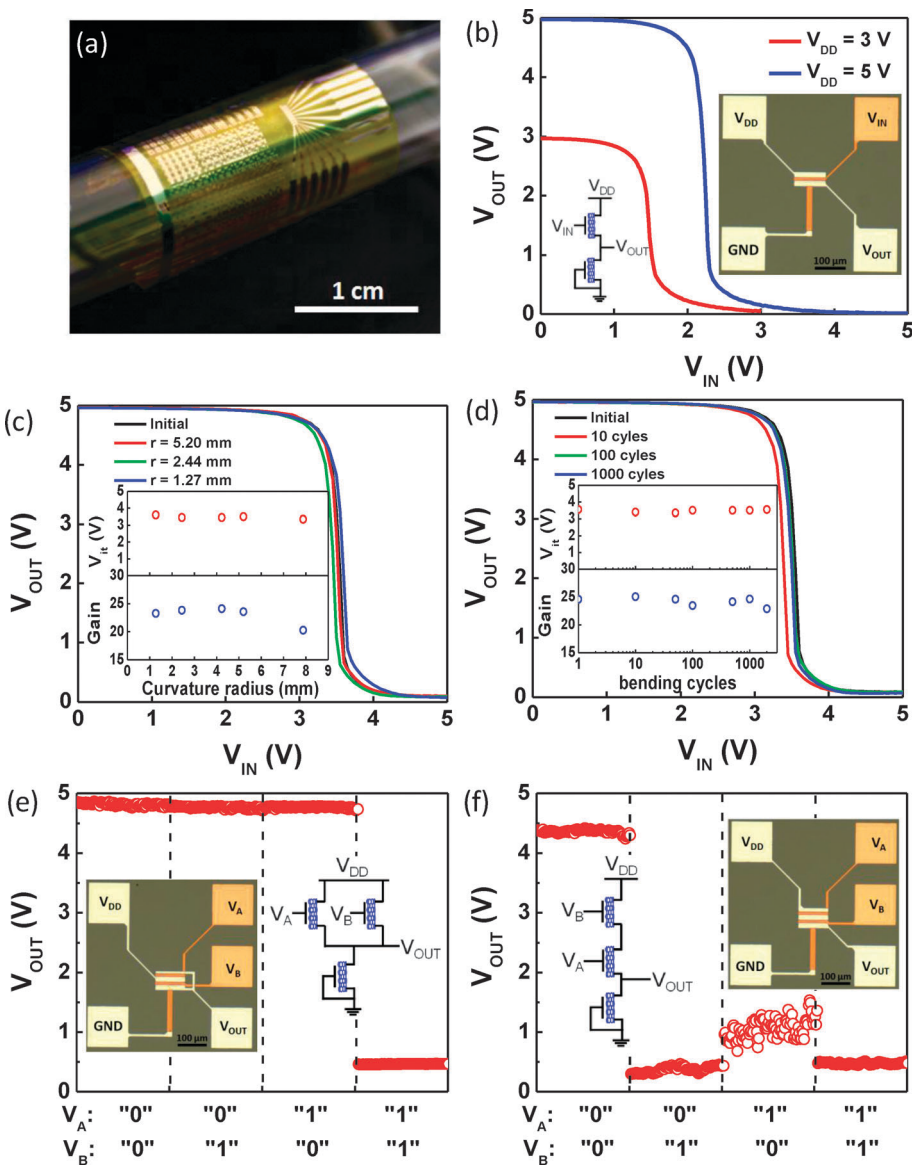

Fig. 11 (a) Photograph of a flexible integrated circuit made with semiconducting nanotube TFTs being wrapped on a test tube with a curvature radius of 5 mm. (b) VTC of a flexible nanotube inverter measured with V_{DD} of 3 or 5 V. (c) Inverter VTC measured at various curvature radii. Inset: Inverter threshold voltage and gain as a function of curvature radius, showing minimal performance change even when bent down to 1.27 mm radius. (d) The inverter VTC is measured after various numbers of bending cycles, indicating good reliability after 2000 cycles. (e, f) Output characteristics of the diode-loaded 2-input NAND (e) and NOR (f) logic gates. Reproduced with permission from ref. 63 (Copyright 2012 American Chemical Society).

multiple stages of logic blocks for larger scale integration, where the output of the preceding logic block needs to be able to drive the ensuing logic block directly. Moreover, owing to the excellent mechanical flexibility of the carbon nanotube networks, the fabricated inverter circuit is extremely bendable. The measured inverter VTC shows minimal performance change under various curvature radii (down to 1.27 mm) (Fig. 11c) and repeated bending tests (2000 cycles) (Fig. 11d). Similarly, 2-input NAND (Fig. 11e) and NOR (Fig. 11f) logic gates have also been demonstrated with diode load. Both circuits are operated with a V_{DD} of 5 V and input voltages of 5 and 0 V are treated as logic "1" and "0", respectively. For the NAND gate, the output is "1" when either one of the two inputs is "0", while for the NOR, the output is "0" when either one of the two inputs is "1". The measured output characteristics confirm the correct functioning of the circuits.

With the combination of the above-described basic logic blocks, more sophisticated integrated circuits, requiring cascading multiple stages of logic gates, can be readily constructed.[51,53] As an example, a 4-to-16 decoder consisting of 88 carbon nanotube TFTs has been demonstrated by Rogers *et al.*[51] This represents the first medium-scale integrated nanotube circuits. The photograph and optical micrograph of the nanotube decoder are shown in Fig. 12a. The 4-bit decoder works in a way that only one of the sixteen outputs are enabled at a time based on the sixteen possible input combinations,

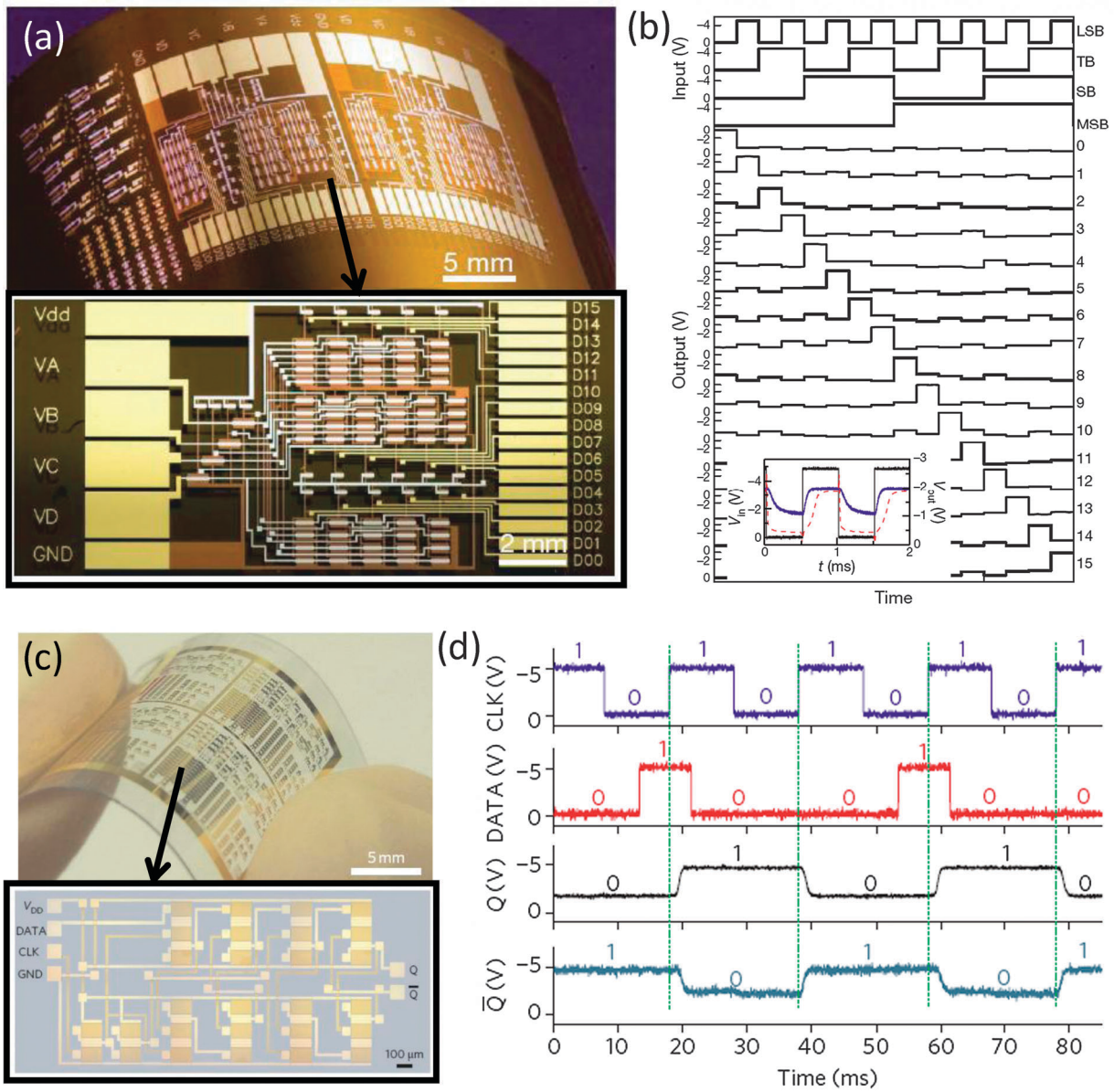

Fig. 12 (a) Photograph and optical micrograph of a 4-to-16 decoder made with nanotube TFTs. (b) Transient response of the decoder. Reproduced with permission from ref. 51 (Copyright 2008 Nature Publishing Group). (c) Photograph and optical micrograph of a D-flip-flop made with nanotube TFTs. (d) Transient response of the D-flip-flop. Reproduced with permission from ref. 53 (Copyright 2011 Nature Publishing Group).

as shown in the transient response of the decoder (Fig. 12b). Besides combinational logic, sequential logic such as synchronous D-flip-flop has also been used whose optical micrograph is shown in Fig. 12c.[53] As shown in the transient response of the D-flip-flop (Fig. 12d), the input (DATA) can be transmitted and stored at the output (Q) at each rising edge of the clock signal (CLK). In a word, significant progress has been made with the carbon nanotube integrated circuits. With the successful demonstration of both combinational and sequential logic blocks, complete system-level integration is possible and functional blocks such as arithmetic and logic unit (ALU) could be demonstrated in the future.

3.2 Conformal electronics

In recent years, flexible and stretchable electronics have been intensively explored for enabling new applications that are otherwise unachievable with the conventional rigid substrates. As discussed above, carbon nanotube TFTs have already been widely used in electronics fabricated on flexible substrates. Nevertheless, such flexible substrates can only be bent along one orientation and cannot be conformally wrapped over spherical surfaces. This limits the applications in wearable electronics where conformal coverage is required.

By cleverly engineering the substrate, a mechanically deformable and stretchable active-matrix backplane containing arrays of SWNT TFTs has been demonstrated.[62] The use of polyimide substrate and the basic fabrication process is the same as the previously-described flexible nanotube TFTs. However, by laser cutting a honeycomb mesh structure into the substrate, the otherwise non-stretchable polyimide substrate is made stretchable.

As shown in Fig. 13a, the enabled TFT backplane is used to conformally wrap around the surface of a baseball. Nanotube TFTs are strategically placed at each corner of the hexagons where the strain is minimal according to the mechanical simulations.[62] The stretching results of the TFTs are shown in Fig. 13b. The experiments show that the I_{DS}–V_{GS} characteristics of the devices show minimal performance change even when stretched up to 10%. This is the first demonstration of a novel type of carbon-nanotube-based backplane for stretchable/conformal electronics. Given the minimal thickness of the active channel (*i.e.*, nanotube network thickness), the high mechanical flexibility and stretchability of nanotube TFTs is expected. In future, the use of other stretchable support substrates (*e.g.*, PDMS) along with stretchable passive components (*e.g.*, electrodes and dielectrics) needs to be explored.

3.3 Artificial electronic skin

Artificial electronic skin (e-skin)[89] has been demonstrated previously, consisting of an array of tactile sensors capable of mapping touch. This is done by laminating a pressure-sensitive rubber (PSR) onto a flexible backplane containing arrays of carbon nanotube TFTs.[62] The e-skin is useful for mapping the applied pressure and could find wide range of applications in robotics, wearable electronics, and medical prostheses.

PSR has conducting carbon nanoparticles embedded inside. Upon pressing, the distance between the nanoparticles becomes smaller and the tunnelling probability becomes larger. This is reflected in the change of resistance under various applied pressures.[89] By connecting the PSR in series with a carbon nanotube TFT, one pixel of the active-matrix is formed (Fig. 14a).[62] By changing the applied pressure on the PSR, the output conductance of the pixel undergoes significant change as shown in Fig. 14b. The detection limit of such a configuration is around 1 kPa. As a practical example, the e-skin sensor is used to perform spatial and temporal mapping of the pressure applied on the surface as shown in Fig. 14c. In the experiment, an L-shaped

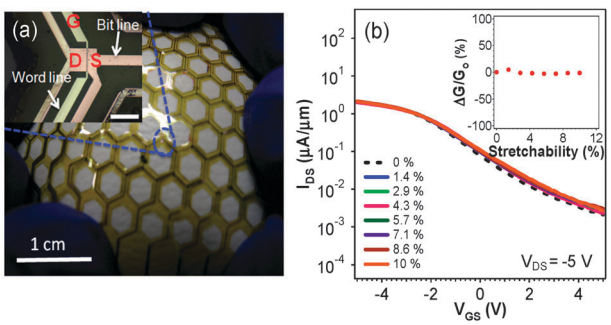

Fig. 13 (a) Photograph of a stretchable nanotube TFT array, which is conformally wrapped around a baseball. Inset: Optical micrograph showing a nanotube TFT placed at the corner of a hexagonal opening. (b) I_{DS}–V_{GS} characteristics of the device measured under various stretching conditions. Inset: Normalized on-state conductance as a function of stretchability. Reproduced with permission from ref. 62 (Copyright 2011 American Chemical Society).

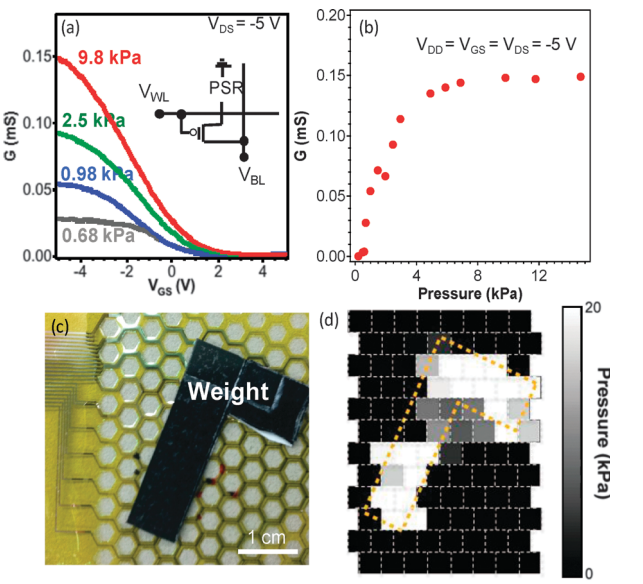

Fig. 14 (a) Pressure response of a pixel of an artificial electronic-skin, consisting of a nanotube TFTs active-matrix backplane and a pressure sensitive rubber. The I_{DS}–V_{GS} characteristics of a pixel are measured under various applied pressures. (b) Output conductance at V_{DD} = V_{GS} = V_{DS} = −5 V as a function of the applied normal pressure. (c) Photograph showing an electrical skin sensor with an L-shaped object placed on top. (d) The two-dimensional pressure mapping obtained from the L-shaped object in (c). Reproduced with permission from ref. 62 (Copyright 2011 American Chemical Society).

object is placed on the sensor, and upon electrically scanning through the pixels in the array, a two-dimensional pressure profile is obtained (Fig. 14d), which matches well with the shape of the object used.

3.4 Display electronics

The pixels in an active-matrix display are controlled by transistors that act as switches and are typically made from amorphous silicon[18] or polysilicon.[19] While amorphous Si suffers from performance limitations, poly-silicon deposition requires high temperature processing which is often incompatible with plastic substrates. As an alternative channel semiconducting material for TFT applications, solution processed carbon nanotubes offer high mobility, are optically transparent and mechanically flexible.

With the capability of large-area fabrication of high-quality nanotube TFTs with high uniformity, high on/off ratio and excellent mobility,[59,62,63] a monolithically integrated active-matrix organic light-emitting diode (AMOLED) display has been successfully demonstrated on glass substrates (Fig. 15).[88] As one of the most promising candidates for the next generation display technologies, OLEDs hold great advantages compared to liquid crystal displays (LCD) due to their high efficiency, superior color purity, low power consumption, large view angle, low temperature processing, and excellent flexibility.[90–94] The schematic diagram and optical micrograph of one pixel of the nanotube-based AMOLED display are shown in Fig. 15a and b, respectively. Each pixel consists of two semiconducting nanotube TFTs, one capacitor, and one OLED. The two-transistors, one-capacitor (2T1C) design (Fig. 15c inset) is necessary for output retention in line-by-line scan for displaying dynamic videos. The OLED fabrication involves the sputtering of transparent indium tin oxide (ITO) as the anode, evaporation of hole transporting layer 4-4′-bis[*N*-(1-naphthyl)-*N*-phenyl-amino]-biphenyl (NPD), emission layer tris(8-hydroxyquinoline) aluminum (Alq3), and LiF and aluminum cathode. As shown in Fig. 15c and d, the current flow through the OLED (I_{OLED}) (red line) and light output intensity (green line) can be modulated by more than 10^5 times by changing the voltages applied on the data line (V_{DATA}). The modulation of light output is visually seen in the photographs shown in Fig. 15d. Fig. 15e shows a glass substrate containing 7 AMOLED chips. Each chip contains 20 × 25 pixels driven by a total of 1000 nanotube TFTs. When all the pixels are turned on (V_{DATA} = −5 V, V_{SCAN} = −5 V, and V_{DD} = 8 V), a yield of ~70% was achieved (Fig. 15f), which is respectable for a proof-of-concept demonstration in the present laboratory-scale experiments. The use of 1000 nanotube TFTs also represents one of the highest degrees of integration to date for carbon-nanotube-based electronics. The demonstration shows carbon nanotubes' great potential as a competing technology alongside amorphous silicon, LTPS, organic semiconductor, and metal-oxide semiconductor as a low-cost and scalable backplane option.

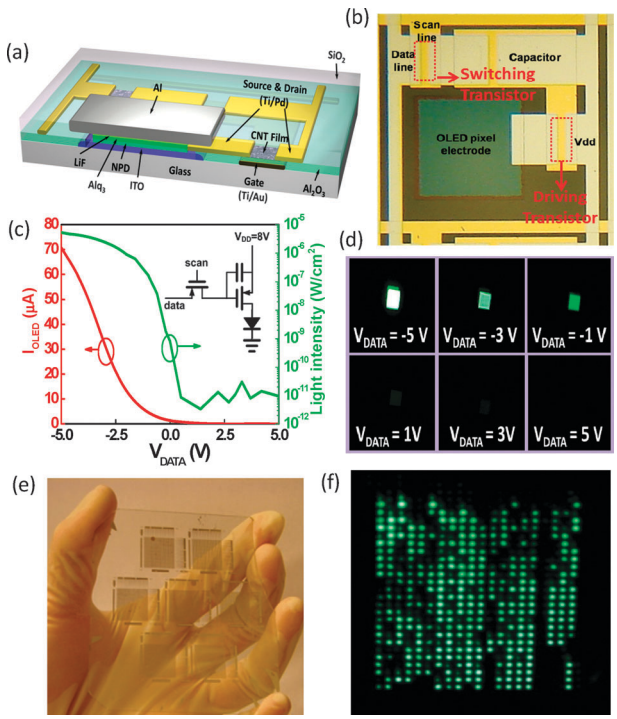

Fig. 15 (a) Schematic diagram showing a pixel of a monolithically integrated AMOLED. Each pixel consists of two semiconducting nanotube TFTs, one capacitor, and one OLED. (b) Optical micrograph of a AMOLED pixel. (c) OLED current (I_{OLED}) (red line) and light intensity (green line) as a function of the voltage on the data line (V_{DATA}). (d) Photographs showing OLED light output under various V_{DATA} voltages. (e) Photograph of 7 AMOLED chips fabricated on the glass substrate. Each chip contains 20 × 25 pixels with a total of 1000 nanotube TFTs. (f) Photograph of the AMOLED display with all pixels turned on. Reproduced with permission from ref. 88 (Copyright 2011 American Chemical Society).

4. Low-cost process scheme for flexible carbon nanotube electronics: printing

Another important feature of solution-processed nanotube TFTs is that they could potentially be fully printed. Printed electronics offer a cost-effective route to achieve mass production of large-area flexible electronic circuits at extremely low cost and high throughput without the need for special photolithography or vacuum-based processes. Numerous research efforts have been devoted in the past to develop a low-cost printed integrated circuit platform using nanotube TFTs. Conventionally, the lack of pure metallic or semiconducting carbon nanotube inks has hindered the fabrication of high performance printed nanotube devices. With the use of commercially available high purity semiconducting nanotube inks, high mobility and high on/off ratio carbon nanotube thin-film transistors have been demonstrated using an aerosol-jet printing process.[64] In this process, the gate, source and drain electrodes are first defined using conventional photolithography and lift-off processes. The channel semiconducting nanotube network, ion-gel dielectric, and PEDOT:PSS gate are subsequently defined using the aerosol-jet printing process (Fig. 16a). Using this method, high-performance transistors, inverters, NAND gates, and ring oscillators have been demonstrated (Fig. 16b).

Fully-printed transistors and integrated single-pixel OLED control circuits have also been demonstrated by using inks containing silver nanoparticles for the printed electrodes and interconnections.[65] It should be noted that ionic gel has been used in both publications as the gate dielectric for a simplified fabrication process. However, due to the unique operating principle of the ionic gel, the devices exhibit ambipolar behavior and the operating speed of the transistors is expected to be slow, limited by the movement of the ions. These problems require further improvements in the future.

For larger scale applications and mass production, gravure (roll-to-roll or R2R) printing can be used.[66–68] This represents a more cost-effective approach. In this method, the gate, dielectric, source/drain, and carbon nanotube layers are sequentially printed onto a roll of polyethylene terephthalate (PET) film (Fig. 16b). Ink formulation and viscosity control are critical in this case in order to achieve uniform printing at large scales. Fully-printed carbon nanotube logic gates, half adder, D-flip-flop, and one-bit radio-frequency identification (RFID) tags have been successfully produced.[66–68]

Despite the tremendous success in carbon nanotube printed electronics, it should be pointed out that the printing approach is useful for making cost-effective large scale nanotube circuits requiring only moderate performance because the resolution that is currently achieved using printing processes is limited (typically ten μm or more). For applications where high performance is required and cost is not a major concern, conventional photolithography and metalization is still preferred, primarily adopting the conventional processes utilized for LCD manufacturing, but with a thin layer of polymer cured on the glass handling substrate.

5. Conclusions and outlook

As a conclusion, this paper reviews the recent progress made on the use of carbon nanotubes TFTs for scalable, practical, and high performance macroelectronics. To overcome the challenges of nanotube assembly, minimizing the device-to-device performance variation, and making the fabrication process scalable and compatible with industry standards, methods have been developed to deposit thin-films of high-purity semiconducting carbon nanotubes at large-scales. This excellent material platform has enabled fabrication of high-performance TFTs on both rigid and flexible substrates with superb carrier

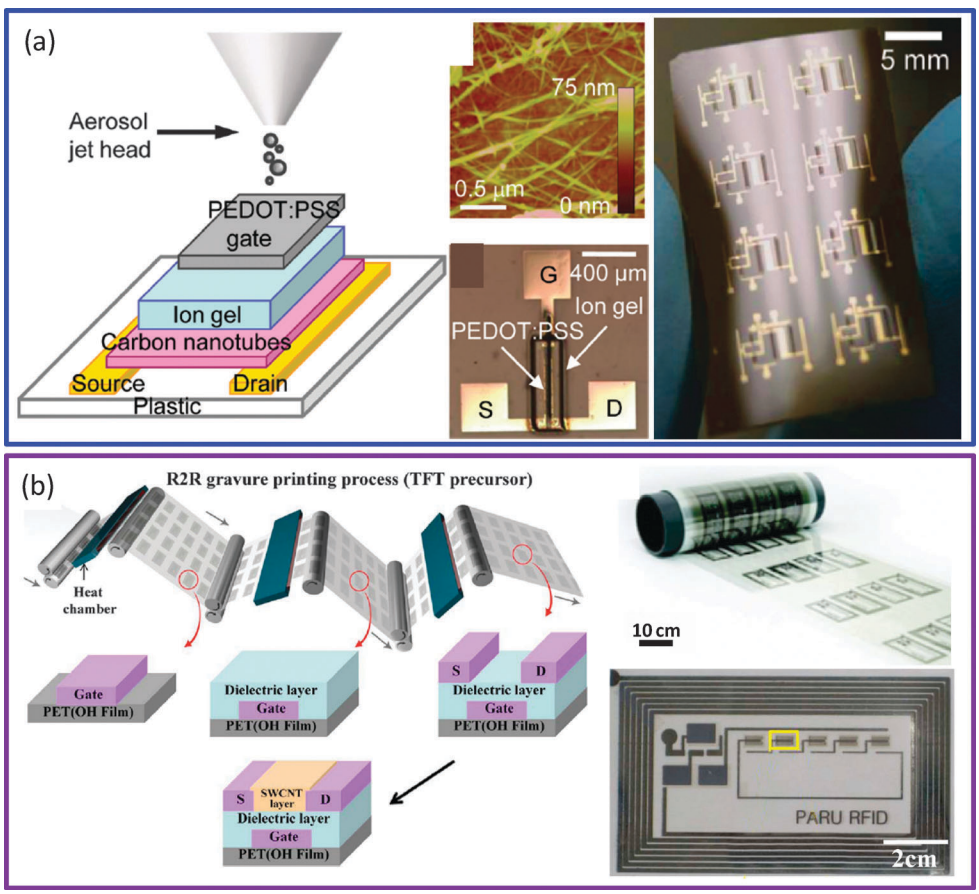

Fig. 16 (a) Nanotube TFTs fabricated using aerosol jet printing where the channel nanotube network, ion-gel dielectric, and PEDOT:PSS gate are defined using a printing process. Left: Schematic of the printing process. Center: AFM image and optical micrograph of the printed TFT. Right: Photograph of an array of printed NAND logic gates. Reproduced with permission from ref. 64 (Copyright 2010 American Chemical Society). (b) Left: Schematic illustration showing the fabrication process of fully-printed nanotube TFTs made using the roll-to-roll gravure printing process. Right: Fully-printed nanotube RFIDs. Reproduced with permission from ref. 66 and 67 (Copyright 2011 IEEE).

mobilities of ~ 50 cm^2 V^{-1} s^{-1} and high $I_{on}/I_{off} > 10^4$. On the basis of the above achievements, various kinds of electronic applications including conformal integrated circuits, active-matrix display electronics, and artificial electronic skin have been explored. The successful demonstrations show carbon nanotubes' immense promise for high performance thin-film electronics.

For the future research in this field, predictable and highly uniform device performance is indispensable for more sophisticated nanotube integrated circuits. For instance, precise control of the transistor threshold voltage and subthreshold characteristics is required. As a result, it is important to control not only the electronic type (metal *vs.* semiconducting) but also ultimately the chirality of the carbon nanotubes. Since chirality-specific nanotube separation has already been achieved,[71,72] a higher degree of control on the electrical characteristics is expected from TFTs made using such carbon nanotubes. In addition, further lowering of the I_{off}, without sacrificing I_{on}, is desirable, which can be obtained by increasing the semiconductor purity of the nanotube solutions as well as optimizing the deposition process to minimize the bundling of the assembled nanotubes. From application point of view, the next step is moving toward more sophisticated system-level integrated circuits. For the CMOS operation, platforms that are capable of providing n-type nanotube TFTs with reproducibility and uniformity comparable to their p-type counterparts need to be developed. As an example of the above-described system-level integration, a SWNT-based central processing unit (CPU) on a flexible substrate is worthy of investigation. One can envision that the demonstration of a flexible CPU would be a truly remarkable milestone in nanotube electronics, and could find tremendous applications in future low-cost, high-performance wearable electronics, and flexible user-interactive displays.

Acknowledgements

This work was partially funded by NSF COINS, NSF CAREER Award, and DARPA/DSO Maximum Mobility and Manipulation. A.J. acknowledges support from the World Class University program at Sunchon National University and a Sloan Fellowship.

Notes and references

1 *Carbon Nanotubes – Synthesis, Structure, Properties, and Applications*, ed. M. S. Dresselhaus, G. Dresselhaus and Ph. Avouris, Springer, 2001.
2 *Carbon Nanotube Electronics*, ed. A. Javey and J. Kong, Springer, 2009.
3 J. Wildoer, L. Venema, A. Rinzler, R. Smalley and C. Dekker, *Nature*, 1998, **391**, 59–62.
4 T. Odom, J. Huang, P. Kim and C. Lieber, *Nature*, 1998, **391**, 62–64.
5 A. Javey, J. Guo, Q. Wang, M. Lundstrom and H. Dai, *Nature*, 2003, **424**, 654–657.
6 T. Durkop, S. A. Getty, E. Cobas and M. S. Fuhrer, *Nano Lett.*, 2004, **4**, 35–39.
7 X. Zhou, J. Y. Park, S. Huang, J. Liu and P. L. McEuen, *Phys. Rev. Lett.*, 2005, **95**, 146805.
8 S. Tans, A. Verschueren and C. Dekker, *Nature*, 1998, **393**, 49–52.
9 R. Martel, T. Schmidt, H. R. Shea, T. Hertel and Ph. Avouris, *Appl. Phys. Lett.*, 1998, **73**, 2447–2449.
10 A. Javey, J. Guo, D. Farmer, Q. Wang, D. Wang, R. Gordon, M. Lundstrom and H. Dai, *Nano Lett.*, 2004, **4**, 447–450.
11 A. Javey, J. Guo, D. Farmer, Q. Wang, E. Yenilmez, R. Gordon, M. Lundstrom and H. Dai, *Nano Lett.*, 2004, **4**, 1319–1322.
12 A. D. Franklin, M. Luisier, S.-J. Han, G. Tulevski, C. M. Breslin, L. Gignac, M. S. Lundstrom and W. Haensch, *Nano Lett.*, 2012, **12**, 758–762.
13 A. Bachtold, P. Hadley, T. Nakanishi and C. Dekker, *Science*, 2001, **294**, 1317–1320.
14 V. Derycke, R. Martel, J. Appenzeller and Ph. Avouris, *Nano Lett.*, 2001, **1**, 453–456.
15 A. Javey, Q. Wang, A. Ural, Y. Li and H. Dai, *Nano Lett.*, 2002, **2**, 929–932.
16 Z. Chen, J. Appenzeller, Y. Lin, J. S. Oakley, A. G. Rinzler, J. Tang, S. J. Wind, P. M. Solomon and Ph. Avouris, *Science*, 2006, **311**, 1735.
17 L. Ding, Z. Zhang, S. Liang, T. Pei, S. Wang, Y. Li, W. Zhou, J. Liu and L.-M. Peng, *Nat. Commun.*, 2012, **3**, 667.
18 *Technology and Applications of Amorphous Silicon*, ed. R. A. Street, Springer, 2000.
19 S. Ucjikoga, *MRS Bull.*, 2002, **27**, 881–886.
20 A. J. Snell, K. D. Mackenzie, W. E. Spear, P. G. LeComber and A. J. Hughes, *Appl. Phys. A: Solid Surf.*, 1981, **24**, 357–362.
21 C. D. Dimitrakopoulos and D. J. Mascaro, *IBM J. Res. Dev.*, 2001, **45**, 11–27.
22 S. R. Forrest, *Nature*, 2004, **428**, 911–918.
23 G. H. Gelinck, H. Edzer, A. Huitema, E. Van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. Van Der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B.-H. Hiusman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. Van Rens and D. M. De Leeuw, *Nat. Mater.*, 2004, **3**, 106–110.
24 T. Sekitani, U. Zschieschang, H. Klauk and T. Someya, *Nat. Mater.*, 2010, **9**, 1015–1022.
25 T. Sekitani and T. Someya, *Adv. Mater.*, 2010, **22**, 1–19.
26 A. Ismach, L. Segev, E. Wachtel and E. Joselevich, *Angew. Chem., Int. Ed.*, 2004, **43**, 6140–6143.
27 A. Ismach, D. Kantorovich and E. Joselevich, *J. Am. Chem. Soc.*, 2005, **127**, 11554–11555.
28 S. Han, X. Liu and C. Zhou, *J. Am. Chem. Soc.*, 2005, **127**, 5294–5295.
29 C. Kocabas, S. Hur, A. Gaur, M. Meitl, M. Shim and J. A. Rogers, *Small*, 2005, **1**, 1110–1116.
30 L. Ding, D. Yuan and J. Liu, *J. Am. Chem. Soc.*, 2008, **130**, 5428–5429.
31 N. Patil, A. Lin, E. R. Myers, K. Ryu, A. Badmaev, C. Zhou, H.-S. P. Wong and S. Mitra, *IEEE Trans. Nanotechnol.*, 2009, **8**, 498–504.

32 L. Ding, A. Tselev, J. Wang, D. Yuan, H. Chu, T. P. McNicholas, Y. Li and J. Liu, *Nano Lett.*, 2009, **9**, 800–805.
33 S. W. Hong, T. Banks and J. A. Rogers, *Adv. Mater.*, 2010, **22**, 1826–1830.
34 C. Wang, K. M. Ryu, L. Gomez, A. Badmaev, J. Zhang, X. Lin, Y. Che and C. Zhou, *Nano Res.*, 2010, **3**, 831–842.
35 X. Liu, S. Han and C. Zhou, *Nano Lett.*, 2006, **6**, 34–39.
36 S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin and J. A. Rogers, *Nat. Nanotechnol.*, 2007, **2**, 230–236.
37 S. J. Kang, C. Kocabas, H. S. Kim, Q. Cao, M. A. Meitl, D. Y. Khang and J. Rogers, *Nano Lett.*, 2007, **7**, 3343–3348.
38 L. Jiao, B. Fan, X. Xian, Z. Wu, J. Zhang and Z. Liu, *J. Am. Chem. Soc.*, 2008, **130**, 12612–12613.
39 C. Wang, K. Ryu, A. Badmaev, N. Patil, A. Lin, S. Mitra, H.-S. P. Wong and C. Zhou, *Appl. Phys. Lett.*, 2008, **93**, 033101.
40 K. Ryu, A. Badmaev, C. Wang, A. Lin, N. Patil, L. Gomez, A. Kumar, S. Mitra, H.-S. P. Wong and C. Zhou, *Nano Lett.*, 2009, **9**, 189–197.
41 F. Ishikawa, H. Chang, K. Ryu, P. Chen, A. Badmaev, L. De Arco Gomez, G. Shen and C. Zhou, *ACS Nano*, 2009, **3**, 73–79.
42 A. Lin, N. Patil, K. Ryu, A. Badmaev, L. De Arco Gomez, C. Zhou, S. Mitra and H.-S. P. Wong, *IEEE Trans. Nanotechnol.*, 2009, **8**, 4–9.
43 P. G. Collins, M. S. Arnold and Ph. Avouris, *Science*, 2001, **292**, 706–709.
44 G. Hong, B. Zhang, B. Peng, J. Zhang, W. M. Choi, J.-Y. Choi, J. M. Kim and Z. Liu, *J. Am. Chem. Soc.*, 2009, **131**, 14642–14643.
45 Y. Che, C. Wang, J. Liu, B. Liu, X. Lin, J. Parker, C. Beasley, H.-S. P. Wong and C. Zhou, *ACS Nano*, 2012, **6**, 7454–7462.
46 Q. Cao and J. A. Rogers, *Nano Res.*, 2008, **1**, 259–272.
47 Q. Cao and J. A. Rogers, *Adv. Mater.*, 2009, **21**, 29–53.
48 N. Rouhi, D. Jain and P. J. Burke, *ACS Nano*, 2011, **5**, 8471–8487.
49 C. Kocabas, N. Pimparkar, O. Yesilyurt, S. J. Kang, M. A. Alam and J. A. Rogers, *Nano Lett.*, 2007, **7**, 1195–1202.
50 N. Pimparkar, C. Kocabas, S. J. Kang, J. Rogers and M. A. Alam, *IEEE Electron Device Lett.*, 2007, **28**, 593–595.
51 Q. Cao, H. S. Kim, N. Pimparkar, J. P. Kulkarni, C. Wang, M. Shim, K. Roy, M. A. Alam and J. A. Rogers, *Nature*, 2008, **454**, 495–500.
52 E. S. Snow, J. P. Novak, P. M. Campbell and D. Park, *Appl. Phys. Lett.*, 2003, **82**, 2145–2147.
53 D. Sun, M. Y. Timmermans, Y. Tian, A. G. Nasibulin, E. I. Kauppinen, S. Kishimoto, T. Mizutani and Y. Ohno, *Nat. Nanotechnol.*, 2011, **6**, 156–161.
54 M. Engel, J. P. Small, M. Steiner, M. Freitag, A. A. Green, M. C. Hersam and Ph. Avouris, *ACS Nano*, 2008, **2**, 2445–2452.
55 M. A. Meitl, Y. X. Zhou, A. Gaur, S. Jeon, M. L. Usrey, M. S. Strano and J. A. Rogers, *Nano Lett.*, 2004, **4**, 1643–1647.
56 M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim and Z. Bao, *Science*, 2008, **321**, 101–104.
57 M. Vosgueritchain, M. C. LeMieux, D. Dodge and Z. Bao, *ACS Nano*, 2010, **4**, 6137–6145.
58 E. S. Snow, P. M. Campbell, M. G. Ancona and J. P. Novak, *Appl. Phys. Lett.*, 2005, **86**, 033105.
59 C. Wang, J. Zhang, K. Ryu, A. Badmaev, L. Gomez and C. Zhou, *Nano Lett.*, 2009, **9**, 4285–4291.
60 C. Wang, J. Zhang and C. Zhou, *ACS Nano*, 2010, **4**, 7123–7132.
61 N. Rouhi, D. Jain, K. Zand and P. J. Burke, *Adv. Mater.*, 2011, **23**, 94–99.
62 T. Takahashi, K. Takei, A. G. Gillies, R. S. Fearing and A. Javey, *Nano Lett.*, 2011, **11**, 5408–5413.
63 C. Wang, J.-C. Chien, K. Takei, T. Takahashi, J. Nah, A. M. Niknejad and A. Javey, *Nano Lett.*, 2012, **12**, 1527–1533.
64 M. Ha, Y. Xia, A. A. Green, W. Zhang, M. J. Renn, C. H. Kim, M. C. Hersam and C. D. Frisbie, *ACS Nano*, 2010, **4**, 4388–4395.
65 P. Chen, Y. Fu, R. Aminirad, C. Wang, J. Zhang, K. Wang, K. Galatsis and C. Zhou, *Nano Lett.*, 2011, **11**, 5301–5308.
66 M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, J. M. Tour and G. Cho, *IEEE Trans. Electron Devices*, 2010, **57**, 571–580.
67 J. Noh, M. Jung, K. Jung, G. Lee, J. Kim, S. Lim, D. Kim, Y. Choi, Y. Kim, V. Subramanian and G. Cho, *IEEE Electron Device Lett.*, 2011, **32**, 638–640.
68 J. Noh, S. Kim, K. Jung, J. Kim, S. Cho and G. Cho, *IEEE Electron Device Lett.*, 2011, **32**, 1555–1557.
69 M. S. Arnold, S. I. Stupp and M. C. Hersam, *Nano Lett.*, 2005, **5**, 713–718.
70 M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp and M. C. Hersam, *Nat. Nanotechnol.*, 2006, **1**, 60–65.
71 A. A. Green and M. C. Hersam, *Adv. Mater.*, 2011, **23**, 2185–2190.
72 X. Tu, S. Manohar, A. Jagota and M. Zheng, *Nature*, 2009, **460**, 250–253.
73 Q. Cao, M. Xia, C. Kocabas, M. Shim, J. A. Rogers and S. V. Rotkin, *Appl. Phys. Lett.*, 2007, **90**, 023516.
74 X. Liu, C. Lee, J. Han and C. Zhou, *Appl. Phys. Lett.*, 2001, **79**, 3329–3331.
75 M. Shim, A. Javey, N. W. S. Kam and H. Dai, *J. Am. Chem. Soc.*, 2001, **123**, 11512–11513.
76 C. Klinke, J. Chen, A. Afzali and Ph. Avouris, *Nano Lett.*, 2005, **5**, 555–558.
77 Y. Lin, J. Appenzeller, J. Knoch and Ph. Avouris, *IEEE Trans. Nanotechnol.*, 2005, **4**, 481–489.
78 Z. Zhang, X. Liang, S. Wang, K. Yao, Y. Hu, Y. Zhu, Q. Chen, W. Zhou, Y. Li, Y. Yao, J. Zhang and L. M. Peng, *Nano Lett.*, 2007, **7**, 3603–3607.
79 L. Ding, S. Wang, Z. Zhang, Q. Zeng, Z. Wang, T. Pei, L. Yang, X. Liang, J. Shen, Q. Chen, R. Cui, Y. Li and L. M. Peng, *Nano Lett.*, 2009, **9**, 4209–4214.
80 C. Wang, K. Ryu, A. Badmaev, J. Zhang and C. Zhou, *ACS Nano*, 2011, **5**, 1147–1153.
81 J. Zhang, C. Wang, Y. Fu, Y. Che and C. Zhou, *ACS Nano*, 2011, **5**, 3284–3292.
82 S. Y. Lee, S. W. Lee, S. M. Kim, W. J. Yu, Y. W. Jo and Y. H. Lee, *ACS Nano*, 2011, **5**, 2369–2375.
83 C. Rutherglen, D. Jain and P. Burke, *Nat. Nanotechnol.*, 2009, **4**, 811–819.
84 C. Kocabas, H. Kim, T. Banks, J. Rogers, A. Pesetski, J. Baumgardner, S. Krishnaswamy and H. Zhang, *Proc. Natl. Acad. Sci. U. S. A.*, 2008, **105**, 1405–1409.

85 L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J.-P. Bourgoin, A. A. Green and M. C. Hersam, *Appl. Phys. Lett.*, 2009, **94**, 243505.
86 N. Chimot, V. Derycke, M. F. Goffman, J. P. Bourgoin, H. Happy and G. Dambrine, *Appl. Phys. Lett.*, 2007, **91**, 153111.
87 C. Wang, A. Badmaev, A. Jooyaie, M. Bao, K. L. Wang, K. Galatsis and C. Zhou, *ACS Nano*, 2011, **5**, 4169–4176.
88 J. Zhang, Y. Fu, C. Wang, P. Chen, Z. Liu, W. Wei, C. Wu, M. E. Thompson and C. Zhou, *Nano Lett.*, 2011, **11**, 4852–4858.
89 K. Takei, T. Takahashi, J. C. Ho, H. Ko, A. G. Gillies, P. W. Leu, R. S. Fearing and A. Javey, *Nat. Mater.*, 2010, **9**, 821–826.
90 S. Forrest, P. Burrows and M. Thompson, *Laser Focus World*, 1995, **31**, 99–101.
91 J. Sheats, H. Antoniadis, M. Hueschen, W. Leonard, J. Miller, R. Moon, D. Roitman and A. Stocking, *Science*, 1996, **273**, 884–888.
92 C. Tang, *Dig. Tech. Pap.- Soc. Inf. Disp. Int. Symp.*, 1996, **27**, 181–184.
93 P. Burrows, S. Forrest and M. Thompson, *Curr. Opin. Solid State Mater. Sci.*, 1997, **2**, 236–243.
94 G. Gu and S. Forrest, *IEEE J. Sel. Top. Quantum Electron.*, 1998, **4**, 83.