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Room Temperature Oxide Deposition Approach to Fully Transparent, All-Oxide Thin-Film Transistors

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Transparent and flexible electronics represent two emerging fields that have much traction for future technological applications.[1–3] Traditional thin-film transistors (TFTs) fabricated from polysilicon and amorphous silicon, and later from organic semiconductors and carbon nanotubes, enabled the realization of large-scale flexible circuits for display and sensor applications.[4–11] More recently, the family of semiconducting post-transition metal oxides (ZnO, In_2O_3, InZnO, InGaZnO, etc.) offers an additional platform with wide energy bandgaps for optical transparency over the full visible range, room temperature deposition (both solution-based and physical vapor deposition techniques) for plastic compatibility, and electrical properties suitable for TFTs for transparent, flexible, and biorelated applications.[12–17]

However, many existing fabrication techniques for these oxide TFTs, while they are being deposited at room temperature, require higher temperature annealing steps to prime the oxide (i.e., improve crystallinity, improve stoichiometry, or calcination of solutions) for TFT use or to improve the device performance to an acceptable level.[17–21] Unfortunately, the use of higher temperatures for processing and device improvement can severely limit substrate compatibility and present challenges for integration with other components. In order to retain a wide range of substrate choices without sacrificing device performance, a low-temperature fabrication scheme is needed. In this work, we demonstrate fully transparent all-oxide based ZnO TFTs with low operational voltages fabricated using a room temperature deposition method with no post-processing annealing and a maximum device processing temperature of 110 °C.

The schematic process flow for the fabrication of top-gated ZnO TFTs is shown in **Figure 1**a. ZnO TFTs are fabricated on three different substrates: (i) a reference silicon wafer substrate with a 50 nm thick thermal oxide (Figure 1b), (ii) transparent alkali-free borosilicate glass (Figure 1c), and (iii) flexible polyimide foil (Figure 1d).

Substrates are cleaned with acetone and isopropyl alcohol and blown dry with nitrogen. Substrates are then loaded into a cathodic arc vacuum deposition chamber and pumped down to $\approx 5 \times 10^{-6}$ Torr for ZnO deposition. The filtered cathodic arc deposition for zinc oxide has originally been developed for the deposition of transparent conducting oxide films.[22] It has been shown that this deposition technology is similar to pulsed laser deposition (PLD) as it produced a flux of energetic ions. The typical Zn ion energy is 36 eV[23] which leads to local heating right at the film growth region without imposing a large heat load to the substrate. Additionally, in contrast to magnetron sputtering, negative oxygen ions are not accelerated to very high energies of several 100 eV because the arc operates at low arc voltage (the potential difference between anode and cathode is less than 40 V).

The arc deposition system can be described as follows. Cathodic arc deposition (**Figure 2**a) uses a relatively low DC voltage to trigger and sustain a metal arc plasma, where the discharge current of about 50 A is concentrated in non-stationary cathode spots.[24] In contrast to the former work on AZO,[22] here we use a pure (undoped) zinc (99.99%) cathode. It is surrounded by an annular grounded anode body. A permanent ring magnet is placed at the bottom part of the cathode cone: its purpose is to steer the moving arc spots around the cathode, enabling efficient material use and spreading of the heat load on the cathode. The zinc plasma generated at cathode spots streams away from the cathode into the curved macroparticle filter coil. The purpose of the coil is to guide the plasma to the substrate, which is not in line of sight with the cathode. In doing so, the plasma particles (electrons and ions) are separated from the microscopic but relatively massive zinc droplets, also known as "macroparticles." The coil is made of hollow, water-cooled copper tubing. It operates at a constant current of 400 A, producing a magnetic field of the order of 100 mT (more details on plasma guiding and macroparticle removal can be found in ref. [24]). Zn ions react with oxygen dosed into the deposition chamber via a mass flow controller to form a ZnO film on the near-room-temperature substrate surface. 30 nm of ZnO is deposited as the active TFT channel material onto the substrates placed 12.5 cm away from the exit of the plasma macroparticle filter coil in a 5 mTorr O_2/Ar ambient (O_2 60 sccm, Ar 20 sccm unless otherwise stated).

Photolithography is used to define patterns for the source and drain electrodes via lift-off. Source and drain pads consist of 40 nm thick degenerately doped ZnO deposited at lower O_2 partial pressure than the TFT channel ZnO (5 mTorr, O_2 20 sccm, Ar 20 sccm, room temperature), followed by 30 nm

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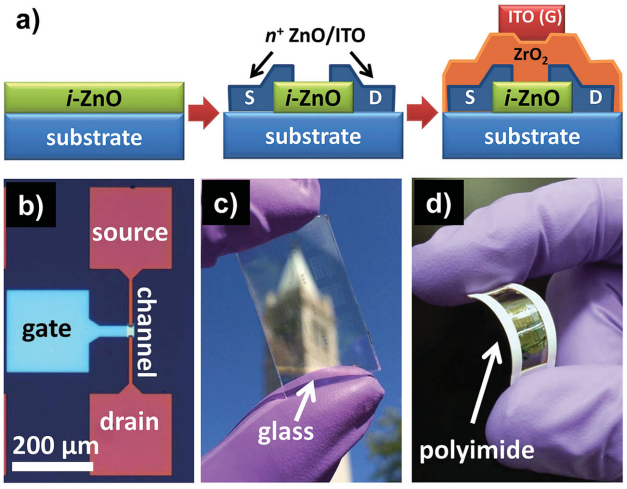

Figure 1. a) Process schematics of ZnO TFT fabrication. b) Optical microscope image of finished device on silicon. c) Photograph of finished device array on glass slide. d) Photograph of finished devices on freestanding polyimide foil bent between fingers.

of indium tin oxide (ITO) sputtered in a 7 mTorr Ar ambient also at room temperature. A second photolithography step is performed to define the ZnO channel region of the transistors by etching in hydrochloric acid (HCl 1% for 1 s). In this process, the top ITO film on the source and drain serves as an etch stop barrier for the underlying ZnO, as the etch rate for ITO in HCl is much lower than that of ZnO.[25] A 20 nm thick ZrO_2 top gate oxide is deposited by atomic layer deposition (ALD) at a maximum temperature of 110 °C and subsequently patterned by photolithography. The same ITO sputtering and lift-off process is then used to define the top gate contact. Figure 1b–d shows optical images of the devices completed on silicon, alkali-free glass, and freestanding polyimide foils, respectively.

We first explore the material properties of ZnO thin films deposited by cathodic arc. X-ray diffraction spectra (XRD) of the ZnO films as a function of O_2 flow rate are shown in Figure 2b. All films exhibit a polycrystalline hexagonal Wurtzite structure and {0002} texture in agreement with literature.[26] The *c*-axis lattice constant extracted from the 0002 peak at 34.8° is 5.2 Å in good agreement with values for sputtered ZnO films.[27] No peaks corresponding to metallic Zn inclusions are detected. Estimating the grain size from the 0002 peak positions 2Θ and full-width half-maximum widths β using the Scherrer equation, $D(2\Theta) = K\cdot\lambda/\beta\cdot\cos 2\Theta$, assuming a crystallite shape factor $K = 0.9$ and substituting $\lambda = 0.154$ nm for Cu Kα radiation, yield grain sizes between ≈17 and 23 nm.[28]

For transistor application, it is important to precisely control the conductivity of the ZnO channel to enable gate control. The carrier concentration in the ZnO film can be tuned by adjusting the O_2 flow rate during deposition as the carrier concentration of intrinsic ZnO films directly correlates with the number of oxygen vacancies.[26,29] We choose to keep the Ar flow rate and the total deposition pressure constant (20 sccm and 5 mTorr, respectively) and vary the O_2 flow rate from 10 to 35 sccm to modulate the electron concentration in the ZnO. As the O_2 flow rate is increased from 15 to 35 sccm, the electron concentration drops from the mid 10^{19} cm^{-3} to the low 10^{18} cm^{-3} (Figure 2c), while the Hall mobility (second panel in Figure 2c) essentially remains constant between 17.3 and 21.2 cm^2 V^{-1} s^{-1}, with the highest recorded mobility of 21.2 cm^2 V^{-1} s^{-1} being deposited at an O_2 flow rate of 15 sccm. For the higher O_2 flow rates above 35 sccm, the resistivity of the films (third panel in Figure 2c) increases rapidly, rendering Hall measurements unreliable on our setup. However, the ZnO mobilities reported here appear to be some of the highest Hall mobilities for room-temperature-deposited thin-film oxides for TFTs reported in the literature, showing that cathodic arc deposition is reliable for producing high-quality ZnO films.[13–15,17,30,31]

Figure 2d shows the optical absorption of the ZnO films as a function of wavelength and O_2 flow rate. As the O_2 flow rate increases from 10 to 30 sccm, the sub-bandgap absorption at wavelengths longer than 400 nm decreases significantly. This is caused by metallic Zn clusters becoming embedded in the film. Too low of an O_2 flow rate prevents present Zn particles from reacting with the ambient oxygen, causing Zn particles to remain and provide trap states that increase the absorption. Increasing the O_2 flow rate reduces the number of unreacted Zn particles, thus reducing the number of trap states and decreasing the absorption. The absorbance of 30 nm ZnO films in this spectral range drops below 2%. In parallel, the absorption edge at wavelengths shorter than 400 nm shifts to longer wavelengths for increasing O_2 flow rates due to the decreasing electron concentration. This effect is attributed to the reduction of the Burstein–Moss shift, which decreases the optical bandgap as the Fermi level lowers with decreasing electron concentration. These findings are consistent with our Hall measurement results. Absorbance data at 60 sccm O_2, which is the O_2 flow rate used for the ZnO TFT channel, is practically identical to the data at 40 sccm although film resistivity further increases.

We now focus on ZnO TFT device performance. The TFT device architecture implemented is a top gate structure consisting entirely of transparent oxides. We fabricated the all-oxide fully transparent devices on alkali-free glass substrates. **Figure 3**a shows the drain to source (DS) and gate to source (GS) I_{DS}–V_{GS} transfer curves of a TFT device on alkali-free glass with channel width and length of 100 µm, operated at $V_{GS} = \pm 3$ V and $V_{DS} = 3$ V, resulting in an on/off current ratio of ≈10^5. The subthreshold slope (SS) is calculated from a linear fit (dotted line) to be SS = 204 mV dec^{-1}. The threshold voltage of $V_t = 0.36$ V was extracted from a linear fit of $I_{DS}^{1/2}$ versus V_{GS}. The saturation mobility was determined to be μ_{sat} = 4.5 cm^2 V^{-1} s^{-1}, calculated using the peak value of the slope of the $I_{DS}^{1/2}$ versus V_{GS} plot under $V_{DS} = 3$ V saturation operation and a capacitance–voltage (CV) extracted gate oxide capacitance of $C_{ox} = 597$ nF cm^{-2}. Figure 3b shows the I_{DS}–V_{DS} characteristic of the device, exhibiting typical square-law behavior and reaching an on-current of almost 40 nA μm^{-1}. These values compare well with the best reported oxide low-temperature TFTs in literature with SS typically in the range of one hundred to a few hundreds of mV dec^{-1} and V_t less than 1 V.[21,32–37] It should be noted that alkali-free glass is chosen due to impurities in other glasses, such as microscopy slides. We found that charged ions in the glass were causing a threshold voltage shift of our devices, so alkali-free glass was used to avoid this issue.

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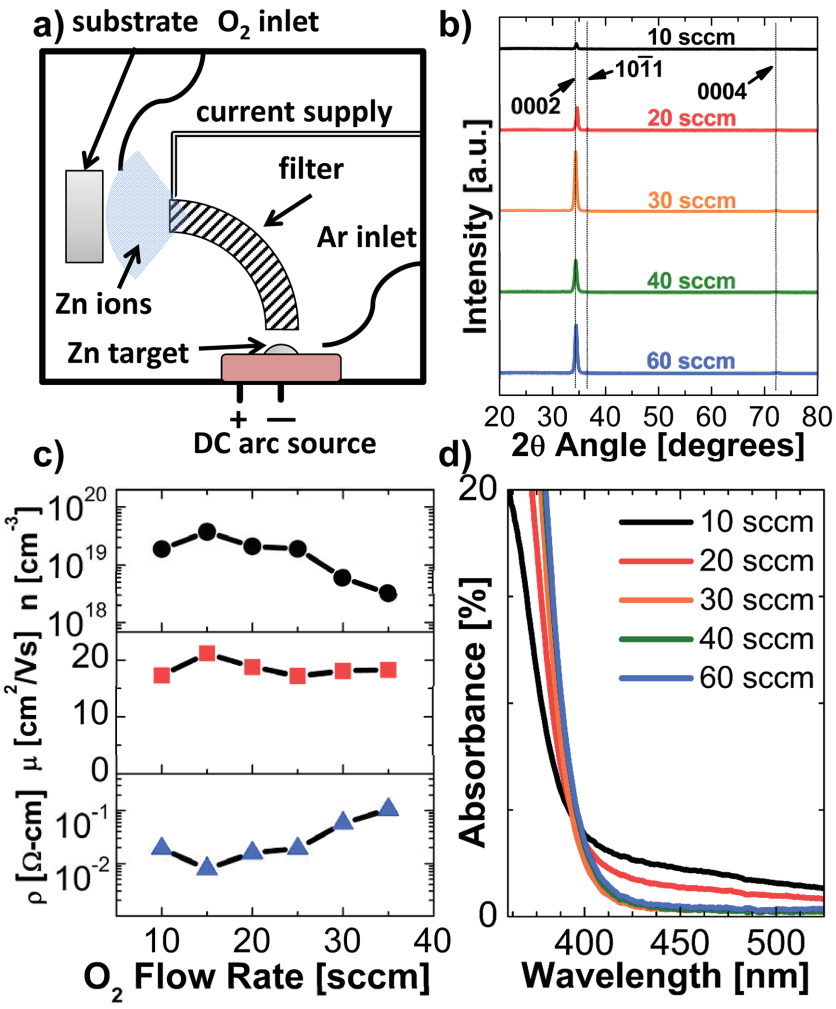

Figure 2. a) Schematic of cathodic arc deposition chamber. The permanent magnet is denoted in red. b) XRD spectra for ZnO films deposited at different O_2 flow rates. c) Electron concentration (n), Hall mobility (μ), and resistivity (ρ) as a function of O_2 flow rate. d) Dependence of optical absorption with O_2 flow rate.

Additionally, the off-current of our devices is comparable to those reported in literature, showing that the room temperature process is able to produce devices with just as low of an off-current as compared to those with higher temperature processes. In terms of the saturation mobility, our lower values as compared to literature can be associated with interface states between the ZrO_2 gate oxide and ZnO channel overlap capacitances between the gate and source/drain, which would cause some of the applied gate field to contribute to state filling and source/drain charges rather than channel inversion, as well as contact resistance effects. These effects can be combated by annealing or plasma treatments for the oxide interfaces and improved alignment during fabrication for the overlap capacitances. Again, seeing that we are avoiding any higher temperature or postannealing to improve the gate–channel interface, our future work will look into plasma treatment to enhance the ZrO_2–ZnO interface.

The process was then ported to flexible polyimide foils. Polyimide resin was spun on a temporary silicon handling wafer and cured at 300 °C for an hour before device fabrication. Figure 3c shows the I_{DS}–V_{GS} transfer curve of the ZnO TFT on polyimide with channel width and length of 100 μm operated at $V_{GS} = \pm 3$ V, exhibiting an on/off current ratio of almost 10^5, with extracted SS, threshold voltage, and saturation mobility of SS = 251 mV dec^{-1}, V_t = 1.2 V, and $\mu_{sat} = 4.8$ cm^2 V^{-1} s^{-1}, respectively. Figure 3d shows the I_{DS}–V_{DS} curves indicating expected square-law behavior with an on-current of again almost 40 nA μm^{-1}, thus reaching identical performance characteristics to the device on glass and with those reported in literature.

For each of the I_{DS}–V_{GS} curves on the two substrates, the increase in off-current at low V_{GS} operation can be attributed to gate leakage resulting from both the thin 20 nm gate oxide and the source/drain to gate overlap. The value of the SS can also be restricted by trap states in the channel–oxide interface, energy band tail states of the ZnO, and series resistance effects from our ITO contacts to our ZnO channel. The on/off ratio is 10^5 at 3 V operation, whereas other studies report ratios as high as 10^8.[32,33] Since the focus of this project is for low voltage operation for digital circuits, we are unable to directly compare the low voltage operation performance of some of the referenced TFTs with higher on/off ratios at higher operation voltages. This is because the referenced devices are being operated at voltages of V_{GS} and $V_{DS} \geq 10$ V, while ours are run at a V_{GS} and $V_{DS} = 3$ V. Overall, the devices made on glass and polyimide show consistent, transferable and reproducible behavior, suggesting this method to be a universally applicable technique for creating fully transparent ZnO TFTs on a variety of substrates. **Table 1** summarizes our results for the ZnO TFT on polyimide and compares this device to other high-performance oxide TFTs reported in literature.

With the focus of these TFTs being on applications in flexible electronics, bending studies are performed to get an idea of the mechanical robustness and its effect on the electrical performance of the device. To remove the polyimide from the handle wafer, the polyimide was cut around the edges and then submerged into DI water for 20 min. Putting the sample in water promotes self-delamination of the polymer from the substrate. This process prevents the polyimide from needing to be manually peeled off, which induces strain on the polymer, potentially cracking the fabricated devices. Once the polyimide has delaminated, the polyimide foil is laid flat, and the devices are measured to quantify possible effects from internal strain relaxation during delamination. Bending tests are then performed by wrapping the polyimide around a test tube with $r = 8$ mm and measuring the device performance while bent.

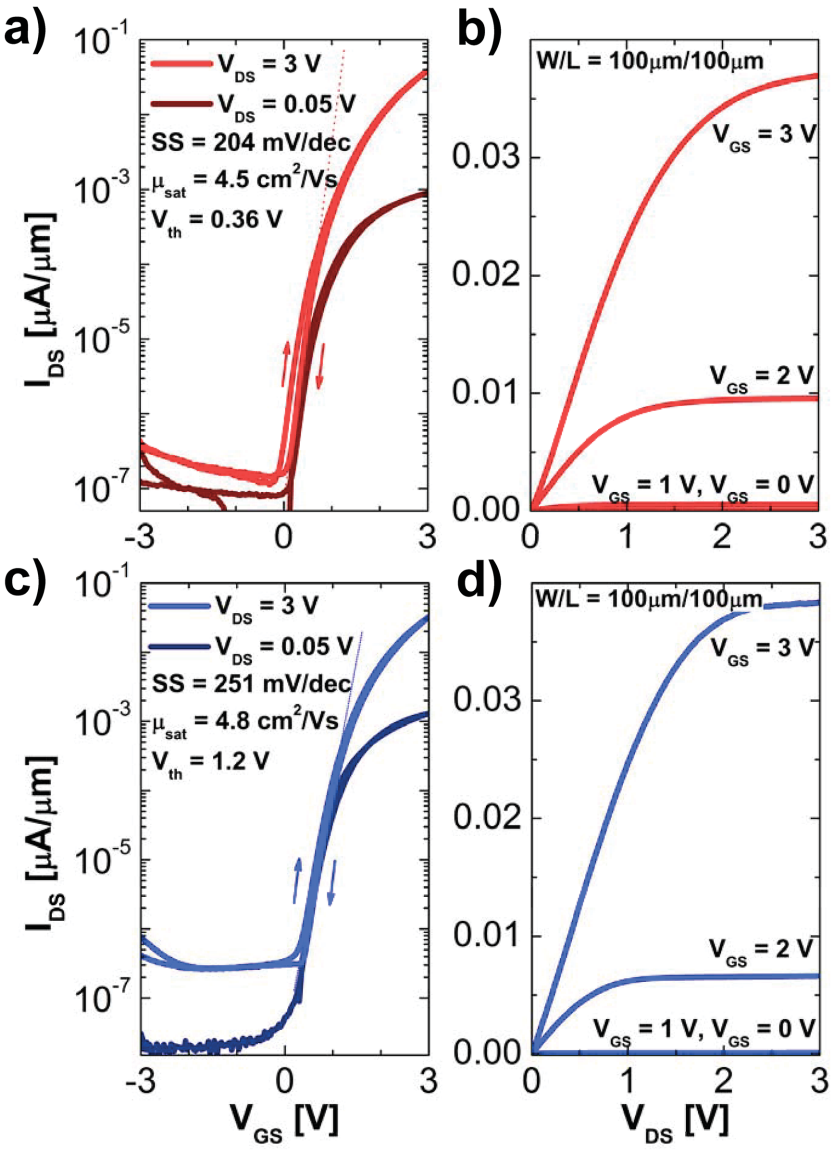

Figure 3. I_{DS}–V_{GS} and I_{DS}–V_{GS} curves for W/L = 100 μm/100 μm device on a,b) alkali-free glass and c,d) polyimide. The arrows on the transfer curves indicate the direction of the double sweep measurement.

inverter gate. Due to these devices being solely NMOS, the inverter was constructed with a depletion-mode transistor load rather than a PMOS device or resistor. Henceforth, the transistor in which the input (V_{IN}) is passed is referred to as the "switching transistor," whereas the depletion-mode transistor, whose gate terminal is connected to the inverter output node (V_{OUT}), is referred to as the "load transistor." The switching voltage of the inverter only depends on the V_t of the switching transistor since the load transistor is acting as the resistive load, so the supply voltage to the inverter (V_{DD}) was chosen to maximize the inverter noise margin. At an input voltage of V_{IN} = 0 V, the switching transistor is off and has a much greater resistance than the load transistor. Thus, V_{OUT} tends toward V_{DD}, logic 1. Upon the onset of inversion, the switching transistor changes from the off-state to the on-state. As the switching transistor turns on, the resistance of the switching transistor becomes comparable to and then much less than that of the load transistor, causing V_{OUT} to be pulled to ground, logic 0. **Figure 5** shows the transfer characteristics of the inverter at V_{DD} = 2 V as well as an optical image and circuit schematic of the device. The contact pads have been labeled for convenience. It should be noted that the V_{TUNE} pad is available for V_t tuning of the load transistor but was not needed and therefore unused in this device.

Also plotted is the DC gain of the inverter, defined as $|\partial V_{OUT}/\partial V_{IN}|$, which is shown to be ≈8. Additionally, the noise margins of the inverter were extracted from the transfer curve by taking the maximum low input voltage (V_{LI}) and the minimum high input voltage (V_{HI}), corresponding to the input voltages at unity gain, and the corresponding output values of those inputs, V_{HO} and V_{LO}, respectively. The high and low input noise margins are then defined as $NM_H = V_{HO}–V_{HI}$ and $NM_L = V_{LO}–V_{LI}$, respectively. The noise margin values were calculated as NM_H = 0.36 V_{DD} and NM_L = 0.33 V_{DD}.

Figure 4 shows the I_{DS}–V_{GS} and I_{DS}–V_{DS} curves for the W/L = 200 μm/25 μm device after peeling off the handle wafer before bending and while bent. This device geometry is chosen for its higher output current values. The on-current of the device drops almost one order of magnitude during delamination, which may be attributed to defects created in the device during strain relaxation of the polyimide film upon delamination. However, while bent at r = 8 mm, there is minimal change in device performance, proving that our ZnO TFT process is not only universally applicable to various substrates but also mechanically robust for flexible electronics.

Furthermore, to demonstrate the applicability of this process to integrated logic systems, we have fabricated an

In conclusion, a filtered cathodic arc deposition technique is demonstrated for room temperature deposition of intrinsic ZnO with electrical and optical quality suitable for transparent transistor applications. Additionally, this method of ZnO deposition has been shown to be usable in the fabrication of all-oxide fully transparent transistors on alkalki-free glass and polyimide with comparable or better electrical performance to alternative TFT platforms and existing oxide TFTs. Bending studies were performed to show the mechanical robustness of the device structure to confirm its potential use on flexible substrates. Additionally, further processing shows the material from cathodic arc deposition can be used for digital logic by

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Table 1. Comparison of this work (denoted with *) to previous ZnO and IGZO TFTs. V_{op} and W/L denote the operation voltage and size of the published device, respectively. Max T refers to the maximum temperature used during device processing, excluding substrate preparations. V_{op} refers to the gate voltage range in which the device was reported, with the accompanying V_{DS} voltage being the highest of the reported V_{op} value. It should be noted that transparency is defined as all components of the transistor, including the gate, source/drain contacts, and the substrate altogether be transparent.

Material	ZnO*	ZnO[21]	ZnO[35]	ZnO[36]	ZnO[37]	IGZO[32]	IGZO[33]	IGZO[34]
Dep. method	CAD	PLD	Sol–gel	Sputtering	Solution	Sputtering	Sol–gel	Sputtering
On/off ratio	10^5	$>10^4$	10^4	$>10^4$	$>10^4$	$<10^7$	10^8	$<10^8$
V_{op} [V]	±3	−1–4	0–3	±1.5	−1–3	±20	±10	±3
SS [mV dec^{-1}]	251	250	≈300 (est.)	180	250	200	95.8	60
V_t [V]	1.2	2	0.7	0.1	0.1	2	2.7	0.5
μ_{sat} [cm^2 V^{-1} s^{-1}]	3.1	0.024	3.4	0.45	22.1	11	<10.5	10
W/L	100/100	2000/50	1500/100	500/50	N/A	400/100	100/10	1000/5
Max T [°C]	110	200	280	200	150	RT	150	325
Transparent?	Yes	Yes	No	No	No	Yes	No	No
Flexible?	Yes	No	Yes	Yes	No	No	Yes	No

creating a working inverter gate entirely out of oxides. Overall, this work demonstrates a low-temperature fabrication process for ZnO TFTs enabling use in both fully transparent and flexible electronic applications.

In future work, such a process could be ported to other flexible plastics with much lower thermal budget than polyimide, such as PET or PEN. Device performance improvements can be achieved by creating better channel–oxide interfaces and decrease series resistance issues, which will help with the gate control of the device and boost device mobility and on/off ratio. Additionally, lower temperature gate oxides via ALD or solution processing will be explored to lower the processing temperature to its lowest limit of 90 °C, as determined by photolithography. Previous research by colleagues should be noted for the development of an e-skin platform based on carbon nanotubes,[10,38,39] which requires uniform TFTs for pixel backplane addressing as well as large-scale digital circuits for on-chip pixel addressing and simple data manipulation. Continued development of this ZnO device platform will enable use in future e-skin applications as an emerging flexible, large-scale circuit system for backplanes and circuits on various flexible substrates.

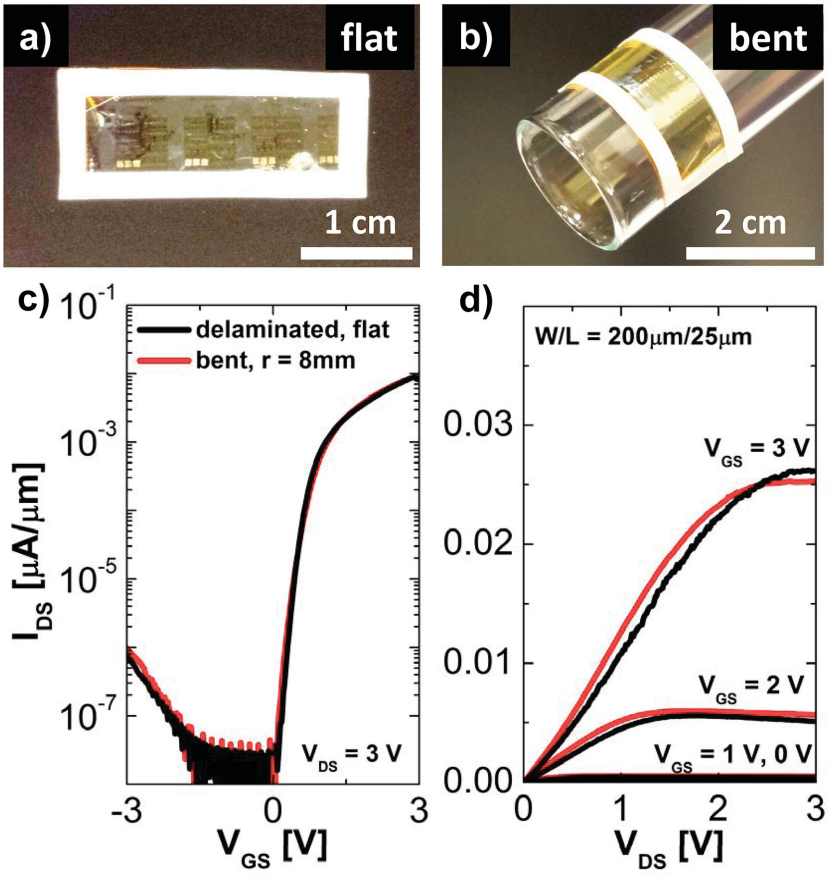

Figure 4. Photographs of the substrate while a) flat and b) bent around a test tube with r = 8 mm. c) I_{DS}–V_{GS} and d) I_{DS}–V_{DS} curves for W/L = 200 μm/25 μm device on freestanding polyimide (black) and bent at r = 8 mm (red).

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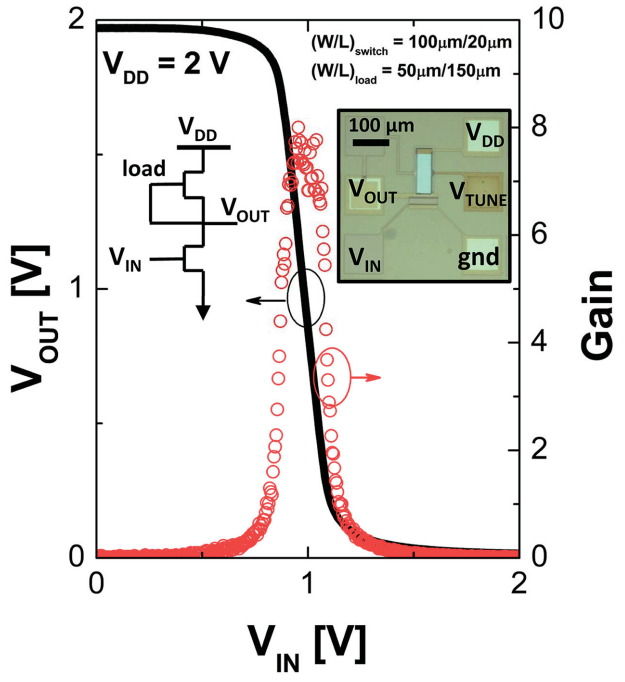

Figure 5. Voltage transfer curve (V_{OUT} vs V_{IN}) and DC gain ($|\partial V_{OUT}/\partial V_{IN}|$) of the all-oxide NMOS inverter on polyimide under an operation voltage V_{DD} = 2 V. The switching transistor has a W/L = 100 μm/20 μm, and the depletion-mode load transistor has a W/L = 50 μm/150 μm. Inset is a schematic representing the device layout as well as the corresponding optical image of the device with labeled contacts.

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