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ABSTRACT

Tellurium (Te) has recently been rediscovered as an attractive semiconducting material for a wide range of electronic and optoelectronic applications. However, thermal instability of Te-based devices has not been investigated and introduces major drawbacks for their practical applications. Toward this goal, this work explores the influence of annealing temperatures on Te transistors and their two failure mechanisms, related to the sublimation of the Te channel and the degradation of the contacts. To overcome these challenges, we fabricated a Te device that is graphene-contacted and SiO_x-encapsulated such that the Te channel and the contacts remain intact and stable at high temperatures. The device exhibits an effective mobility of $\sim$50 cm^2 V^{-1} s^{-1}, which is comparable to traditional metal-contacted Te transistors. The traditional Te devices have performance degradation with increasing temperature and failure at 200 °C. Through the graphene contact and SiO_x encapsulation, our device shows improved thermal stability despite the repeated annealing processes for temperatures up to 250 °C, making it suitable for practical use.

Tellurium has a one-dimensional crystal structure with hexagonally packed helical atomic chains bonded via van der Waals force.[1,2] It is a p-type semiconductor with a thickness-dependent bandgap, which varies from 0.31 eV to 1.04 eV for bulk to monolayer.[2–4] It can provide high hole mobility with low processing temperature and wafer-scale production; therefore, it has been demonstrated as a promising candidate for flexible/transparent electronics and three-dimensional integration circuits.[3] Although various properties and applications of Te have been reported,[3–9] a detailed study of the thermal stability of Te-based devices, which is a major concern for their practical use, is still lacking. Te-based transistors suffer from device degradation after exposure to high temperatures because (1) the high vapor pressure of Te induces sublimation of the channel,[10,11] and (2) interdiffusion/reactivity between the Te and the electrodes causes contact degradation. This can critically limit its practical utility. Thus, a method to mitigate such an effect on Te-based devices is necessary.

In this study, we investigated the effect of temperature on the evaporated Te-based devices and demonstrated a graphene-contacted and SiO_x-encapsulated Te transistor with improved thermal stability. Our device suppresses the sublimation of the Te channel by applying an encapsulation layer such that the Te film remains intact for hours at temperatures up to 250 °C in an N_2 environment. The integration of graphene as a contact with Te also eliminates the interdiffusion/reactivity between Te and the electrodes even after repeated annealing at 250 °C in N_2. Our Te transistor showed a device performance with a hole mobility of $\sim$50 cm^2 V^{-1} s^{-1} after contact annealing, which was similar to a Ni-contacted Te device with the same channel thickness. While typical metal-contacted Te devices show performance degradation with increasing temperatures and failure at temperatures >200 °C, our device can maintain its electrical performance under repeated annealing processes at temperatures up to 250 °C.

The vapor pressure of Te is $\sim10^{-7}$ Torr at 200 °C and reaches $\sim10^{-5}$ Torr at 250 °C.[10] The high vapor pressure results in sublimation of the Te film when it is exposed to a high-temperature environment, significantly deteriorating the electrical properties of Te. Encapsulation is an effective method to stabilize the chemically or thermally sensitive materials such as organic semiconductors and black phosphorus.[12–14] Therefore, we first investigated the effect of the encapsulation layer on the thermal stability of Te films. Patterned crystalline Te films with a thickness of 6 nm were prepared on the cold SiO_2/Si substrates (−80 °C) by thermal evaporation as reported previously[3] [Figs. 1(a) and 1(b)], the average grain size of which was $\sim$25 μm^2. 30 nm SiO_x was subsequently deposited on the substrates by e-beam evaporation to fully encapsulate the Te films on the bottom [Figs. 1(c) and 1(d)]. The Te films with and without the SiO_x encapsulation layer were annealed at 250 °C in an N_2 atmosphere for 1 h to

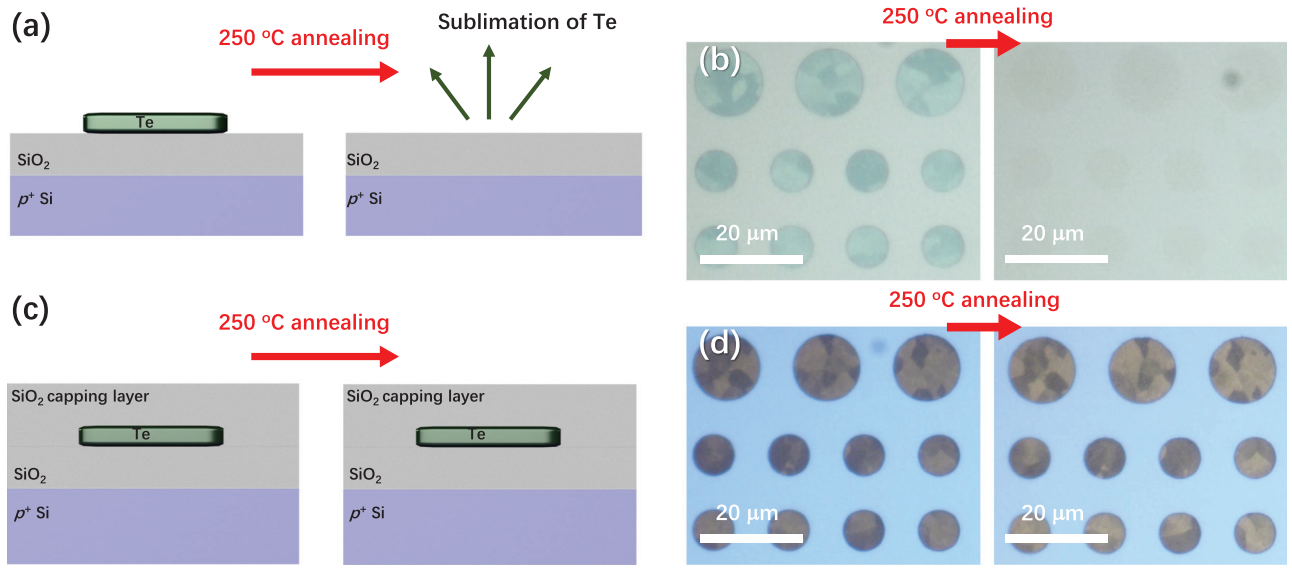

FIG. 1. (a) and (b) Schematic diagram (a) and optical microscopy images (b) of the Te films before (left) and after (right) annealing in the N_2 atmosphere. (c) and (d) Schematic diagram (c) and optical microscopy images (d) of the SiO_x encapsulated Te films before (left) and after (right) annealing in the N_2 atmosphere. The thickness for Te films is ~6 nm, and the thickness for the SiO_x capping layer is ~30 nm. Each annealing process mentioned above lasts for 1 h.

assess their thermal stability. For the uncapped sample, the Te films fully sublimed after the annealing process as shown in Fig. 1(b). In contrast, the encapsulated films did not show surface morphology changes, including the sublimation or the movement of grain boundaries after annealing at 250 °C [Fig. 1(d)]. When the annealing temperature was further increased to 300 °C, re-evaporation of Te was observed on the encapsulated sample (supplementary material Fig. S1). The voids observed on the encapsulated Te films are likely caused by the pinholes or cracks in the evaporated SiO_x capping layer, which are formed or enlarged during the high-temperature annealing process.

Next, field-effect transistors (FETs) were fabricated to further examine the thermal stability of Te at the device level. Te FETs with different metal contacts (Pd, Ni, and Au) were fabricated on the SiO_2 (50 nm)/p^+ Si substrates, which serve as a dielectric layer and a global back gate, respectively [Fig. 2(a)]. These devices were annealed at 250 °C in an N_2 atmosphere for 30 min. For the Pd-contacted FET, a significant change in the channel region was observed after annealing due to the diffusion of Pd atoms into the Te channel [supplementary material Figs. S2(a) and S2(b)]. The diffused Pd metalized the Te channel, which was confirmed by the I_d–V_g transfer curves for the Pd-contacted FET (supplementary material Fig. S3). A similar behavior between Au and Te was also observed after annealing [supplementary material Figs. S2(c) and S2(d)]. These interactions between the metal contact and the Te channel lead to the device deterioration. Among the investigated metal contacts, the Ni contact was considered most stable [supplementary material Figs. S2(e) and S2(f)]. Therefore, we further fabricated Ni-contacted and SiO_x-encapsulated Te devices [Figs. 2(a) and 2(b)] to evaluate their thermal stability. The device was annealed in the N_2 atmosphere repeatedly with annealing temperature increasing from 100 °C to 250 °C [Figs. 2(b)–2(f)]. Each annealing process lasted an hour, and the electrical measurements were performed on the device immediately after each annealing process. Figure 2(g) shows the I_d–V_g transfer curves for the device before and after annealing. The effective mobility, which was extracted from the I_d–V_g transfer curves, decreases slightly from 57 $cm^2\ V^{-1}\ s^{-1}$ to 38 $cm^2\ V^{-1}\ s^{-1}$ as the annealing temperature increases to 150 °C. When the annealing temperature was further raised to 200 °C, the device performance drops dramatically with ~3 orders of magnitude lower effective mobility (~0.05 $cm^2\ V^{-1}\ s^{-1}$) and subthreshold swing increases from 2.3 V dec^{-1} (as-fabricated) to 8.6 V dec^{-1}. The device becomes an open circuit after annealing at 250 °C. We also measured the device performance of encapsulated Ni-contacted Te devices, which contain random lattice orientation along the channel, after annealing at different temperatures (supplementary material Fig. S4). The effective mobility decreases from $26.1 \pm 8.6\ cm^2/V\,s$ to $11.8 \pm 1.8\ cm^2/V\,s$ as the annealing temperature increases to 150 °C. When the annealing temperature reached 200 °C, half of the devices became open circuits, and the rest showed a low effective mobility of ~0.1 $cm^2\ V^{-1}\ s^{-1}$. The degradation in performance above 150 °C is mainly related to the loss of Te around the contact regions. At these locations, re-evaporation/diffusion of Te is easy because the shadowing effect causes poor step coverage and Te and the contact metal can possibly react with each other.[15,16] This explanation is supported by the observable disconnection around the contact regions after annealing at 250 °C [Fig. 2(f)].

To address these challenges, we applied a thin and chemically inert contact material to replace the thick and active metal such that the thermal stability of Te devices can be enhanced. Graphene is considered to be a promising candidate owing to the following reasons. First, the electrical conductivity of graphene is sufficiently high.[17,18] Second, graphene is chemically inert due to large delocalized π electrons, circumventing the interdiffusion/reaction at the interface of the contact at high temperatures.[19,20] In addition, the atomically thin

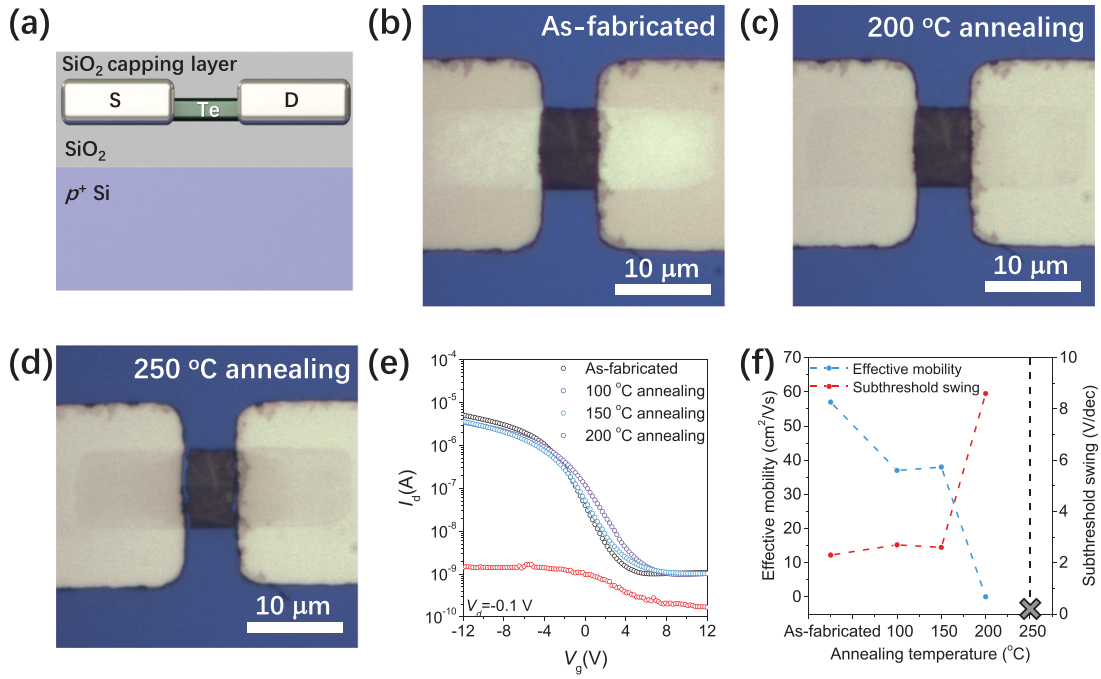

FIG. 2. (a) Schematic diagram of the device structure for a metal-contacted Te device encapsulated with the evaporated SiO_x layer. (b)–(d) A Ni-contacted SiO_x-encapsulated Te device before (b) and after (c) and (d) annealing in the N_2 atmosphere at different temperatures. (e) I_d–V_g transfer curves change for the Ni-contacted SiO_x-encapsulated Te device before and after annealing processes. (f) Effective mobility change extracted from (e). Effective mobility is calculated using $\mu_{eff} = \frac{dI_d}{dV_d}\frac{L}{WC_{ox}(V_g - V_t)}$, where C_{ox} is the gate oxide capacitance, L is the channel length, W is the device width, and V_t is the threshold voltage. The thickness for the Te channel is ~7 nm, and the thickness for the SiO_x-capping layer is ~30 nm. Each annealing process mentioned above lasts for 1 h.

graphene electrodes eliminate the shadowing effect during the capping layer deposition,[14] hence fully encapsulating the Te device to prevent the sublimation.

Graphene-contacted and SiO_x-encapsulated Te FETs were fabricated as shown in Figs. 3(a) and 3(b). The chemical vapor deposition (CVD)-grown bilayer graphene film was transferred onto the SiO_2 (50 nm)/p^+ Si substrate through a wet transfer method,[21] followed by lithography and O_2 plasma etching processes to define the electrodes. The Te film was deposited as a channel connecting the source and drain graphene electrodes. The metal Ni probe pad was deposited far away from the source/drain contact regions. Fabrication was completed by capping the whole device with a 30 nm evaporated SiO_x layer and opening windows on top of Ni pads for probing. The as-fabricated graphene-contacted and SiO_x-encapsulated Te device shows a poor electrical performance [Fig. 3(c)] with the effective mobility of 3.5 $cm^2\ V^{-1}\ s^{-1}$, which is much lower than the effective mobility of the Ni-contacted devices (57 $cm^2\ V^{-1}\ s^{-1}$). Post-annealing has a significant effect on the electrical performance of the graphene-contacted Te device [Figs. 3(c)–3(e)] because the high temperature treatment facilitates removal of residues at the interface and adhesion between Te and graphene,[22,23] yielding an improved contact. The highest contact annealing temperature was 250 °C since the Te device may deteriorate due to the degradation of the encapsulation layer at higher temperatures (>250 °C). As shown in Fig. 3(e), the effective mobility is enhanced from 3.5 $cm^2\ V^{-1}\ s^{-1}$ to 15.1 $cm^2\ V^{-1}\ s^{-1}$ after the contact annealing at 200 °C in N_2. The mobility further increases to 50.4 $cm^2\ V^{-1}\ s^{-1}$ when the annealing temperature is raised to 250 °C. The ON-current level is enhanced by over an order of magnitude after the 250 °C annealing process as shown in the I_d–V_g transfer curves [Fig. 3(c)]. The electrical performance of the annealed graphene-contacted and SiO_x encapsulated Te device is comparable to that of the Ni-contacted device without annealing. It needs to be noted that the annealing temperature (250 °C) for the graphene-contacted devices is even higher than the failure temperature for the metal-contacted ones, demonstrating the advantages of the ultrathin and chemically inert electrodes. We believe that the thermal stability of Te-based devices could be further improved by a more suitable encapsulation layer or a more optimized deposition technique such as low temperature atomic layered deposition or sputtering.

We further investigated the thermal stability of the graphene-contacted and SiO_x encapsulated Te device by tracking its changes in electrical performance after repeated high-temperature annealing processes. The as-fabricated graphene-contacted Te device was first annealed at 250 °C for an hour and was cooled down to room temperature, followed by the electrical measurements. The same annealing procedures and the measurement were performed on the same sample two more times at annealing temperatures of 200 °C and 250 °C. Each annealing process mentioned above lasts for 1 h. As shown in Fig. 4(a), no prominent morphology changes were observed on the device after the repeated high-temperature annealing processes. The semi-log and liner I_d–V_g transfer curves measured after each annealing process are exhibited in Figs. 4(b) and 4(c). No significant device

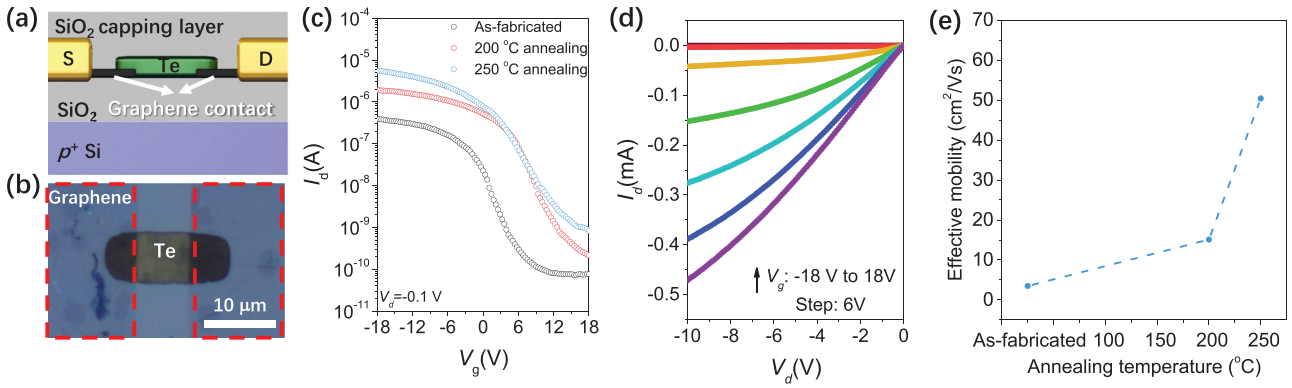

FIG. 3. (a) Schematic diagram of the device structure for a graphene-contacted Te device encapsulated with the evaporated SiO_x layer. (b) Optical image of a typical graphene-contacted encapsulated Te device. (c) I_d–V_g transfer curves of a graphene-contacted SiO_x-encapsulated Te device before and after contact annealing at different temperatures in the N_2 atmosphere. (d) I_d–V_d output characteristics of the graphene-contacted SiO_x-encapsulated Te device after a contact annealing at 250 °C in the N_2 atmosphere. (e) Effective mobility change extracted from (b). The thickness for the Te channel is ~7 nm, and the thickness for the SiO_x capping layer is ~30 nm. Each annealing process mentioned above lasts for 1 h.

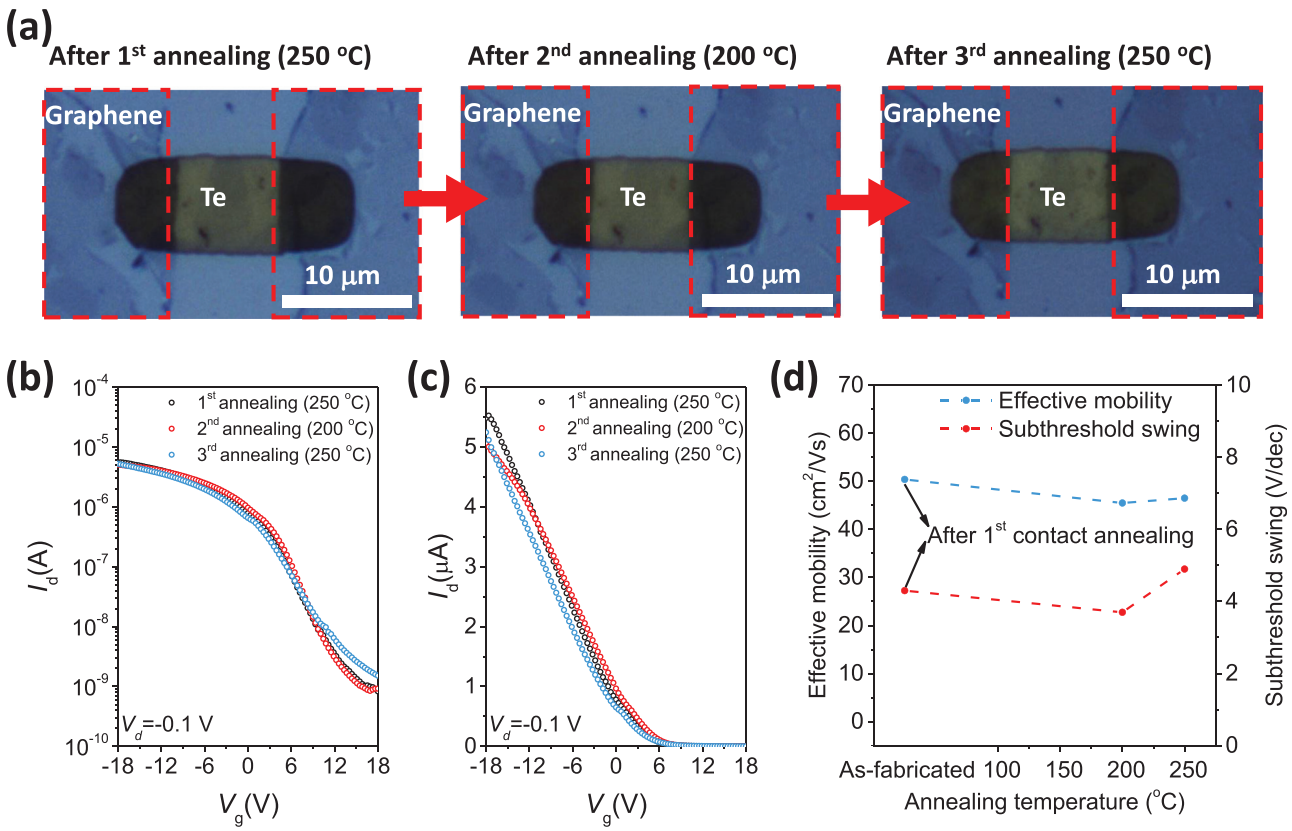

FIG. 4. (a) Optical microscopy images of a graphene-contacted SiO_x-encapsulated Te device after repeated annealing processes. (b) and (c) Semi-log (b) and linear (c) I_d–V_g transfer curves of a graphene-contacted SiO_x-encapsulated Te device after repeated high temperature annealing processes in the N_2 atmosphere. (d) Effective mobility and subthreshold swing change [extracted from (b)] after repeated high temperature annealing processes in the N_2 atmosphere. The thickness for the Te channel is ~7 nm, and the thickness for the SiO_x capping layer is ~30 nm. Each annealing process mentioned above lasts for 1 h.

performance degradation was observed. As apparent from these figures, the device shows a similar I_d–V_g curve after each annealing process. The OFF-current slightly increases from 0.83 nA to 1.5 nA, which is probably due to the quenched-in defects,[24] as Te devices were rapidly cooled from annealing temperatures to room temperature. The subthreshold swing increase from 4.3 V dec^{-1} to 4.9 V dec^{-1} and a small fluctuation in threshold voltage is observed after annealing. The effective mobility of the graphene-contacted and SiO_x-encapsulated Te device remains approximately constant at ~47 cm^2 V^{-1} s^{-1} after repeated thermal treatments with the highest annealing temperature of 250 °C [Fig. 4(d)]. The changes in subthreshold swing and threshold voltage are likely caused by the charges trapped inside the oxide layer or at the interface,[25,26] which could also induce an OFF-current increase. The changes of defects or trapped charges in the Te devices must be small; otherwise, an obvious mobility drop would take place due to the scattering. Supplementary material Fig. S5 shows the effective mobility of 10 individual devices with random lattice orientation along the channel on the same chip after repeated annealing procedures. The devices exhibited an average effective mobility of 48.1 ± 9.7 cm^2/V s. The sustained excellent electrical performance and the long-term thermal stability demonstrate the potential of the graphene-contacted and SiO_x-encapsulated Te device.

In conclusion, this work explores the thermal stability of Te films and devices. To address the thermal instability of Te, we fabricated a graphene-contacted and SiO_x-encapsulated device. The chemically inert graphene provides a thermally stable interface with Te, and the ultrathin nature of graphene allows a fully sealed encapsulation layer on the Te channel. Such a device structure increases the temperature tolerance of the Te-based devices to up to 250 °C. Further enhancement in thermal stability may be possible by improving the encapsulation layer through providing a conformal coating, suppressing pinhole or crack formation, and matching the thermal expansion coefficients between the encapsulation layer and the Te film. Exploration of a proper electrode, which is inert to tellurium at high temperature and compatible to the conventional fabrication process, is needed.

See the supplementary material for optical images of SiO_x-encapsulated Te films and metal-contacted Te devices and I_d–V_g transfer curves for the Pd-contacted Te device before and after annealing.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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