High-gain monolithic 3D CMOS inverter using layered semiconductors

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We experimentally demonstrate a monolithic 3D integrated complementary metal oxide semiconductor (CMOS) inverter using layered transition metal dichalcogenide semiconductor N-channel (NMOS) and P-channel (PMOS) MOSFETs, which are sequentially integrated on two levels. The two devices share a common gate. Molybdenum disulphide and tungsten diselenide are used as channel materials for NMOS and PMOS, respectively, with an ON-to-OFF current ratio (I_{ON}/I_{OFF}) greater than 10^6 and electron and hole mobilities of 37 and 236 cm^2/Vs, respectively. The voltage gain of the monolithic 3D inverter is about 45 V/V at a supply voltage of 1.5 V and a gate length of 1 μm. This is the highest reported gain at the smallest gate length and the lowest supply voltage for any 3D integrated CMOS inverter using any layered semiconductor. *Published by AIP Publishing.*
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Device scaling has been essential to increase integration density in semiconductor circuits and systems with the accompanied benefits of higher speed and lower power dissipation.[1] With scaling, several second order effects such as variability, parasitic resistance, and parasitic device and interconnect capacitance are limiting the performance of the devices, circuits, and systems.[2] Monolithic 3-dimensional (3D) integration in which active device layers are sequentially fabricated can improve the circuit and system performance by reducing the average interconnect length and capacitance, thereby increasing the circuit speed and decreasing power dissipation.[3] 3D integration also enables the integration of heterogeneous active materials. To this effect, monolithic 3D integration of logic circuits, memory, and sensors was demonstrated. Layered transition metal dichalcogenides (TMDs) such as molybdenum disulphide (MoS_2), tungsten diselenide (WSe_2), and so on show promising electronic and optoelectronic properties.[4] TMDs allow precise thickness control down to a monolayer thickness (less than a nanometer), which could potentially solve an important problem in scaled devices, i.e., variation in the channel thickness in ultra-thin body devices.[5] Many of the TMD materials such as MoS_2 and WSe_2 have a lower dielectric constant, which can reduce the drain-to-channel coupling and hence improve the short-channel performance of highly scaled devices.[6] The relative dielectric constant is ~10.7 for the bulk and reduces to ~3.4 for the monolayer thickness of MoS_2. The in-plane and out-of-plane dielectric constants of bulk MoS_2 are 7.43 and 15.4, respectively, and for monolayer MoS_2, they are 1.63 and 7.36, respectively.[7] Transistors using MoS_2 and WSe_2 have shown low mobility degradation with a gate-to-channel electric field even at monolayer channel thickness.[8–10] A field-effect hole mobility as high as 300 cm^2/Vs was reported for monolayer WSe_2 MOSFET.[10] Hence, monolithic 3D integration using TMDs is interesting for further scaling.

In the planar complementary metal oxide semiconductor (CMOS) static logic gates, the N-channel (NMOS) and the P-channel (PMOS) transistors are placed on the same plane. The gate, source, and drain electrodes are connected appropriately to form the inverter circuit as shown in Fig. 1(a). It can be seen that a pair of NMOS and PMOS devices are present in the circuit, and electrically, they share the same gate electrode. A typical layout for the inverter is shown in Fig. 1(b). The NMOS and the PMOS share the gate electrode. In many circuits such as NAND, NOR, XOR, and XNOR, the source and drain electrodes cannot always be shared and must be electrically isolated as shown in the generalized device structure [Fig. 1(c)]. This type of shared gate 3D architecture was explored for silicon MOSFETs and FinFETs and TMDs.[11,12] To date, the only monolithic 3D integration using TMDs showed a CMOS inverter voltage

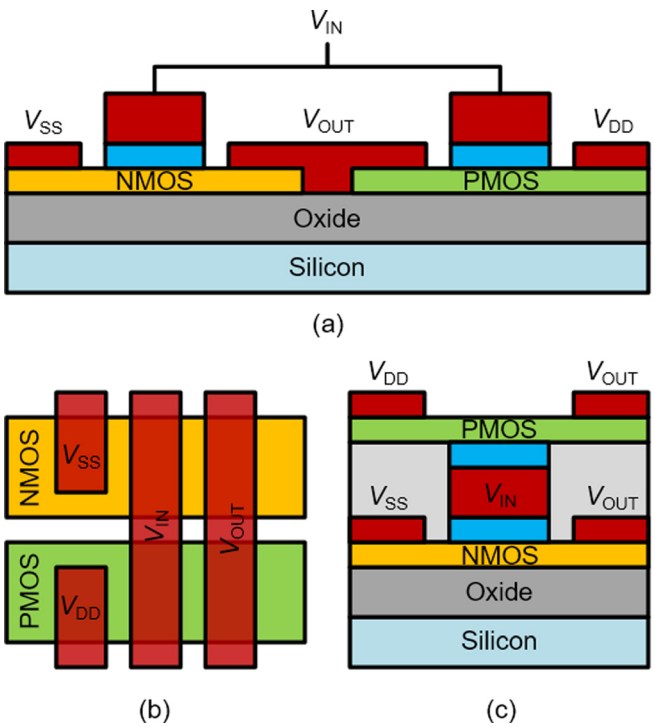

FIG. 1. (a) Planar implementation of the CMOS inverter. (b) Layout of a planar CMOS inverter. (c) Monolithic 3D CMOS inverter with the common gate and electrically isolated source/drain electrodes.

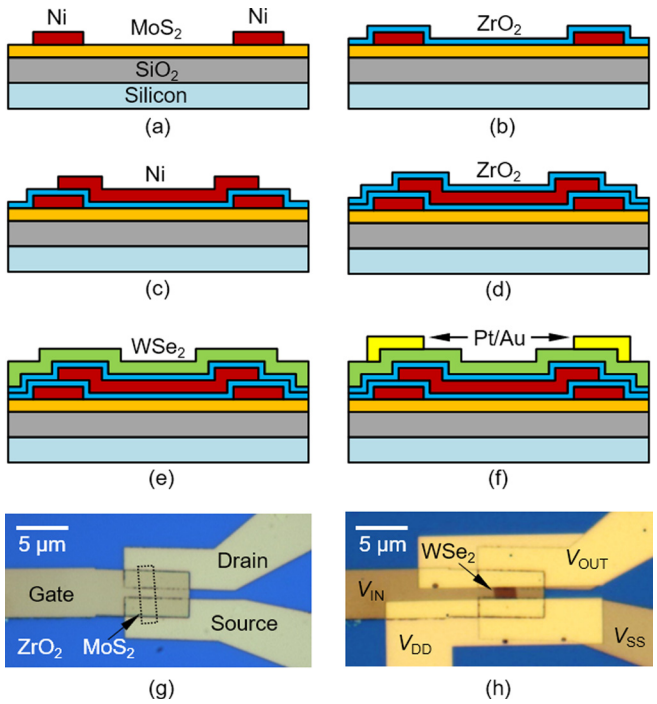

FIG. 2. Device fabrication flow: (a) MoS_2 flake (thickness = 3.5 nm) on the Si/SiO_2 substrate after source/drain Ni contacts; (b) after ZrO_2 deposition using ALD; (c) Ni top gate is formed; (d) ZrO_2 is deposited using ALD; (e) WSe_2 flake (thickness = 2.8 nm) is placed on the gate stack using dry transfer; and (f) Pt/Au contacts are formed on WSe_2. Optical image of the device after (g) S/D contacts and gate formation to MoS_2; and (h) Pt/Au S/D formation on WSe_2. WSe_2 MOSFET is fabricated right on top of the MoS_2 MOSFET. The gate length for NMOS and PMOS is 1 μm.

gain ($\Delta V_{OUT}/\Delta V_{IN}$) of about 10 V/V at a supply voltage (V_{DD}) of 3 V.[11] In comparison to Ref. 11, in this work, we have added forming gas anneal, which is used as a cleaning step after the transfer of WSe_2. Forming gas anneal was used to reduce the output conductance of the WSe_2 PMOS device and hence improve the voltage gain of the CMOS inverter. In this work, we report a high-gain monolithic 3D integrated common-gate CMOS inverter using MoS_2 as NMOS and WSe_2 as PMOS with a peak switching gain of about 45 V/V at $V_{DD} = 1.5$ V, which is the highest reported gain at the smallest gate length and the lowest supply voltage for any reported 3D integrated CMOS inverter using any channel material.

Device fabrication was carried out on a p+ doped silicon substrate with 260 nm of silicon dioxide (SiO_2). MoS_2 and WSe_2 flakes were transferred onto the substrate using the mechanical exfoliation method. Flakes with 3 nm to 6 nm thickness were chosen for further device fabrication. The chosen MoS_2 flakes were etched into rectangular shapes using xenon difluoride (XeF_2) gas.[13] 40 nm of nickel (Ni) was evaporated and lifted-off to form the source/drain contacts to MoS_2 [Fig. 2(a)]. 1 nm of SiO_x was evaporated as the seeding layer, and 20 nm zirconium dioxide (ZrO_2) deposited using atomic layer deposition (ALD) at 110 °C acts as the high-κ gate oxide [Fig. 2(b)]. Figure 2(c) shows the first layer MoS_2 MOSFET with a 40 nm Ni metal common gate for the MoS_2 N-MOSFET in the first layer and the WSe_2 P-MOSFET that will be formed on top of the first layer. Next, 20 nm of ZrO_2 was deposited at 110 °C using ALD [Fig. 2(d)]. WSe_2 flake was transferred on top of the gate dielectric using a pick-and-place transfer method [Fig. 2(e)].[8] The flake was etched into a rectangular shape using XeF_2 gas. At this stage, forming gas anneal was performed at 120 °C for 30 min. Forming gas anneal is known to remove organic residues.[14] Forming gas anneal helps to clean the surface of WSe_2. 10 nm of platinum (Pt) and 30 nm of gold (Au) were evaporated and lifted-off to form the S/D contacts to WSe_2. Figure 2(g) shows the device after the gate metal formation. Figure 2(h) shows the final device after S/D contacts are formed on WSe_2.

Figures 3 and 4 show the $I_D - V_G$ and $I_D - V_D$ characteristics of representative MoS_2 NMOS and WSe_2 PMOS devices, respectively. The threshold voltage (V_T) was extracted using the constant current method with a current reference of 10^{-7} A/μm. For the MoS_2 NMOS, V_T was extracted to be −0.56 V. The drain current at $V_D = 1$ V and $V_G - V_T = 1$ V is about 10 μA/μm. The I_{ON}/I_{OFF} ratio is over 10^6. For the WSe_2 PMOS, V_T, drain current at $V_D = -1$ V and $|V_G - V_T| = 1$ V, and I_{ON}/I_{OFF} ratio are about −1.48 V, 50 μA/μm, and 10^7, respectively. The electron field-effect mobility for MoS_2 was extracted to be 37 cm^2/Vs, and the hole field-effect mobility for WSe_2 was 236 cm^2/Vs, which are commensurate with those reported in the literature.[8–10,15] The contact resistance of MoS_2 MOSFET is 1.45 kΩ μm and that of WSe_2 MOSFET is 1.04 kΩ μm on each side. The peak transconductance (g_m) for MoS_2 and WSe_2 MOSFETs is about 15 μS/μm and 42 μS/μm, respectively. The devices show excellent output saturation. The output conductance (g_{ds}) at $|V_G - V_T| = 1$ V for MoS_2 and WSe_2 MOSFETs is less than 1 nS/μm each. In Ref. 11, the output conductance

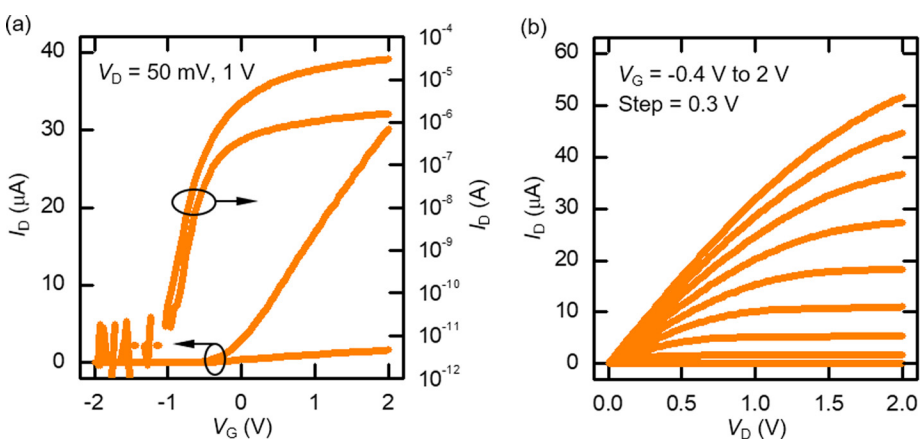

FIG. 3. $I_D - V_G$ and $I_D - V_D$ characteristics of MoS_2 N-MOSFET.

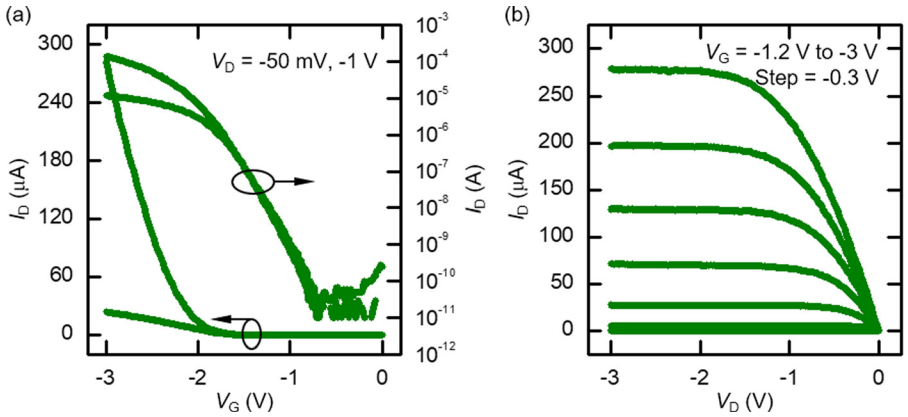

FIG. 4. $I_D - V_G$ and $I_D - V_D$ characteristics of WSe_2 P-MOSFET.

of the reported WSe_2 PMOS device was about 5 μS/μm. The forming gas anneal step that was added after the transfer of WSe_2 helped to obtain a cleaner surface and improved the output conductance. The voltage gain for a CMOS inverter is $(g_{mn} + g_{mp})/(r_{on}||r_{op})$, where r_o is the output resistance of the device and the subscripts n and p refer to the NMOS and PMOS devices, respectively.[16] High g_m and r_o $(=1/g_{ds})$ are required to achieve high switching voltage gain in a CMOS inverter. Figure 5 shows the voltage transfer characteristics and peak gain of a representative monolithic 3D integrated CMOS inverter. The highest peak gain of about 45 V/V is observed at $V_{DD} = 1.5$ V and gate length $L_G = 1$ μm, which is the highest gain reported at the smallest gate length and the lowest supply voltage for a monolithic 3D CMOS inverter using any channel material. To use an inverter in a circuit,

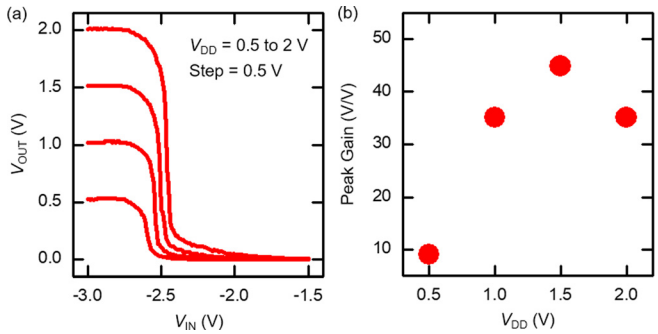

FIG. 5. (a) Voltage transfer characteristics of the monolithic 3D CMOS inverter and (b) peak voltage gain as a function of supply voltage.

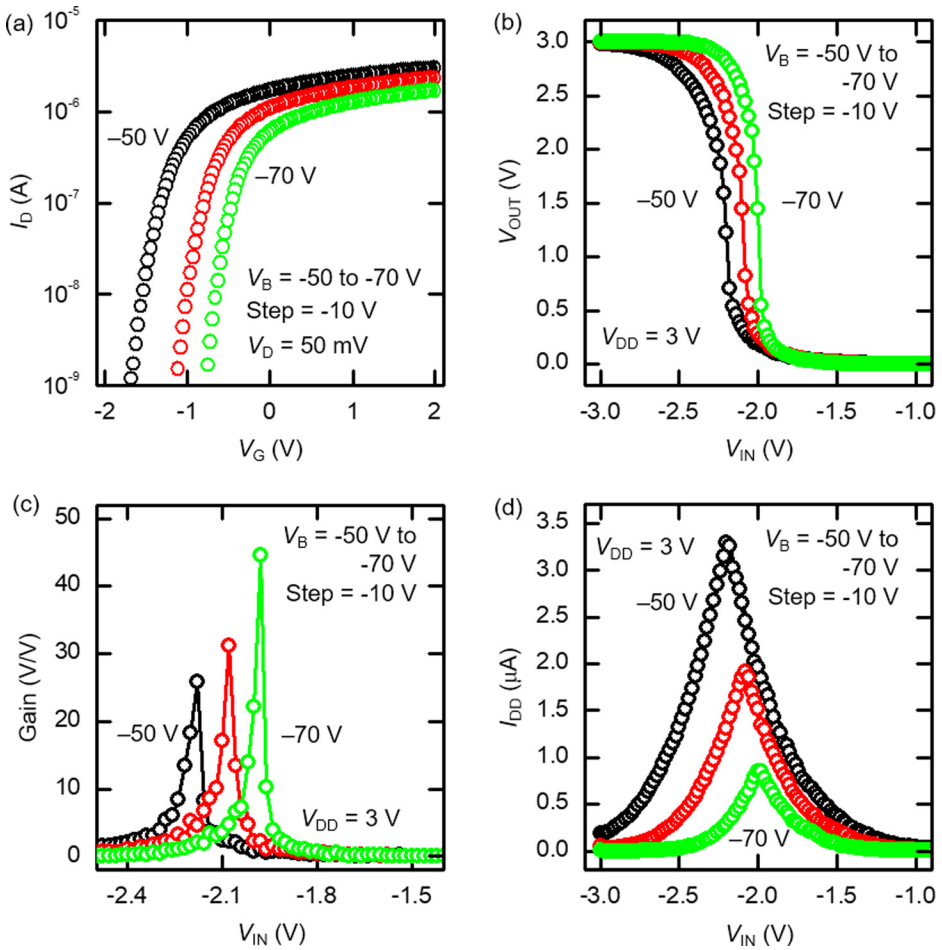

FIG. 6. (a) $I_D - V_G$ characteristics as a function of V_B. (b) Voltage transfer characteristics of a monolithic 3D CMOS inverter as a function of V_B. (c) Voltage gain of the monolithic 3D CMOS inverter as a function of V_B. (d) Current drawn from the supply voltage as a function of V_{IN}.

switching must be achieved between 0 and V_{DD}, preferably at around $V_{DD}/2$. The inverter shown in Fig. 5 does not switch between 0 and V_{DD} as the V_T of NMOS is negative. Hence, the noise margins for the inverter cannot be calculated. Methods such as gate work function engineering,[17] channel doping,[9,16,18] and local back biasing[11,19] can be used to achieve the correct V_T for NMOS. Figure 6 shows the impact of substrate back-biasing (V_B) on the performance of MoS_2 NMOS and inverter. By applying a more negative back bias, the V_T of the MoS_2 NMOS increases and becomes less negative. The V_T changes from -1.32 V to -0.45 V when the back bias is changed from -50 V to -70 V, respectively. The back-bias-coefficient ($\gamma = \delta V_T/\delta V_B = C_{oxb}/C_{oxf} = t_{oxf}/t_{oxb}$) is about 44 mV/V, where the subscripts *oxf* and *oxb* refer to the front and back oxides, respectively.[20] The low γ is due to the thick SiO_2 layer and can be increased by decreasing the thickness of the SiO_2 layer. Substrate back bias shifts the switching point (V_{IN} at $V_{OUT} = V_{DD}/2$) of the inverter to more positive values of V_{IN} as the V_T of NMOS increases [Fig. 6(b)]. The switching point shifts by about 200 mV positive when the back bias changes from -50 V to -70 V. Voltage gain increases with the increase in RBB [Fig. 6(c)]. The voltage gains are 26 V/V, 31 V/V, and 45 V/V at $V_B = -50$ V, -60 V, and -70 V, respectively. This shows that MoS_2 NMOS with positive V_T can further improve the voltage gain of the monolithic 3D CMOS inverter. The inverter voltage gain is benchmarked against the other reported implementations of planar and 3D CMOS inverters.[11,15,16,19,21,22] Among all the reported monolithic 3D CMOS inverters using any channel materials, this work shows the highest voltage gain of 45 V/V, obtained at $V_{DD} = 1.5$ V and $L_G = 1\ \mu$m (Fig. 7). Previously reported implementation of the MoS_2-WSe_2 monolithic 3D CMOS inverter showed a voltage gain of 10 V/V at $V_{DD} = 3$ V.[11] The monolithic 3D CMOS inverter using InAs (NMOS)/Ge (PMOS) showed a voltage gain of 45 V/V at $V_{DD} = 4$ V and $L_G = 1.5\ \mu$m.[23] The carbon nanotube (CNT)-based 3D CMOS inverter showed a gain of about 8 V/V at $V_{DD} = 5$ V.[22] The gain of the inverter increases with the smaller channel length modulation parameter, λ, which is inversely proportional to the gate length (L_G). CMOS inverters with longer L_G will show higher gain. Hence, this work shows the highest gain at the smallest gate length for a 3D CMOS inverter using any channel material.

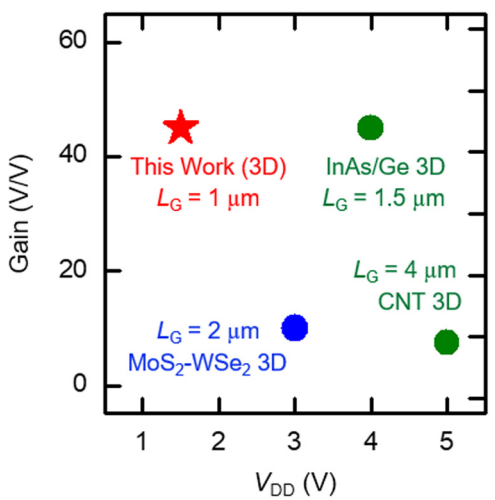

FIG. 7. Benchmarking of our TMD monolithic 3D CMOS inverter against other reported 3D CMOS inverters. MoS_2-WSe_2 3D,[11] InAs/Ge 3D,[23] and CNT 3D.[22]

Monolithic 3D integration is essential to increase the integration density accompanied by higher speed and lower power dissipation. We demonstrate a monolithic 3D integrated CMOS inverter using layered transition metal dichalcogenides. For a monolithic 3D CMOS inverter using any layered semiconductor, we report the highest voltage gain of about 45 V/V, which is achieved at a supply voltage of 1.5 V and a gate length of 1 μm.

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