Comparative study of solution-processed carbon nanotube network transistors

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Carbon nanotube networks in thin-film type transistors were studied experimentally, comparing the use of pre-separated semiconducting enriched nanotubes (90% and 99% purity) to examine how topology affects the properties of the devices. Measurements are reported for two deposition methods used for network formation: random and spin-aligned deposition methods. The results show that the thin-film transistors fabricated via spin-aligned deposition demonstrate better electrical uniformity and performance than those produced by the random network deposition method. Our results imply that coverage and alignment are strongly correlated with the properties of the devices and should therefore be simultaneously optimized for improved electrical uniformity and performance. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4752006]

Networks of single-walled carbon nanotubes (SWNTs) represent a class of electronic materials that can serve as high-performance channel layers in thin-film field effect transistors (TFTs) and other devices.[1–5] The favorable properties of such films may provide a route to practical nanotube-based electronic systems by eliminating the need for precise control over the properties or positions of individual SWNTs. Although single-tube devices can potentially achieve the intrinsic mobility of a semiconducting SWNT,[6] single-tube assembly methods are extremely challenging to scale up and are not yet technologically practical for large-area applications. Therefore, thin films of SWNTs consisting of either random or well-aligned networks represent a promising path to scalable device manufacturing.[7,8] However, such films may have a lower mobility than single-tube devices because tube-tube crossings limit the current flow from source to drain when the channel length is greater than the nanotube length.[9,10] Increasing the network density can increase the current but can also lead to a shorted TFTs[11] resulting from a detrimental increase in the probability of having a percolation path dominated by metallic species.

The problem of the co-existence of metallic and semiconducting SWNTs can be addressed by using pre-purified semiconducting enriched SWNTs produced, for example, by density gradient ultracentrifugation.[12] However, limitations are also imposed in this process because cost-effective, 100% pure semiconducting nanotubes are not available. Therefore, all commercially available enriched solutions contain some amount of metallic nanotubes, which may negatively impact semiconducting device properties. To date, there has been progressive research based on highly pre-enriched semiconducting nanotubes (i.e., over 95% semiconducting nanotubes).[13,14] Nevertheless, many interesting issues remain to be studied. Open questions include whether improved performance can be achieved with separated nanotubes of lower enrichment (<95%) and how does network topology affect the transport and uniformity properties.[15] Here, we present the results of experimental studies designed to address these questions by evaluating the transport and uniformity properties of transistors fabricated from 90% semiconducting nanotubes with varying degrees of alignment and coverage, using transistors fabricated from 99% semiconducting nanotubes for comparison. Two representative deposition methods were studied for the formation of nanotube networks in this analysis: (i) random and (ii) spin-aligned deposition methods.

Prior to the formation of nanotube networks, a silicon substrate with a 55-nm oxide layer (Si/SiO_2) was cleaned by O_2 plasma treatment to make it hydrophilic. Next, the cleaned substrate was immersed in a poly-L-lysine solution (0.1% w/v in water; Sigma Aldrich), to form an amine-terminated adhesion layer followed by a deionized (DI) water rinse.[7,8] Subsequently, the samples were immersed in a commercially available solution (0.01 mg/ml) of semiconducting nanotubes (Nano Integris Inc.) for 1 min, 3 min, or 7 min for the random network deposition method, followed by DI water and isopropanol rinses, and then blow-dried in nitrogen. For the spin-aligned deposition method, 200 μl of the semiconducting nanotube solution was dropped by pipette near the center of the surface of the poly-L-lysine-modified substrate at spin speeds of 3000 rpm or 7000 rpm (Headway Research). Subsequently, DI water and isopropanol rinses were similarly applied after 3 min of reaction time. After the formation of the networks, 30-nm Pd source-drain electrodes were deposited using e-beam evaporation followed by a lift-off process. Finally, because the nanotube thin films covered the entire chips, one more step of photolithography and O_2 plasma was used to define the channel widths and to remove unwanted paths. In all of the devices, the gate width and length were fixed at 3 μm and 4 μm, respectively. We fabricated 144 devices for each network-formation condition. Although the transistors exhibited some hysteresis, as is typical for devices of this type,[16] the current values and on/off ratios, the central focus of this study remained robust and independent of the directional history of the voltages applied to the gate. Electrical tests on the network transistors were performed in air and at room temperature, with no further passivation or annealing treatments.

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Figure 1 displays the measurements of the devices fabricated from the random network deposition method using the 99% semiconducting nanotube solution. Evidently, the nanotube density on the poly-L-lysine-modified SiO_2 strongly depends on the deposition time (Figure 1(a)). For a deposition time of 1 min, network percolation was not fully achieved due to short nanotube lengths, resulting in low yields (data not shown). For the 90% semiconducting nanotube solution, however, network percolation was observed with the 1-min deposition time, as will be discussed in more detail below. The use of higher semiconducting enriched nanotubes, e.g., a 99% semiconducting nanotube solution, helps to achieve a sufficient on/off ratio with a smaller channel length and thus a smaller device area. On the other hand, higher enrichment of semiconducting nanotubes requires more ultracentrifugation, resulting in a relatively shorter nanotube length that inhibits network formation.[17]

The transfer characteristics of the devices fabricated via the random network deposition method under two conditions are shown in Figure 1(b), measured at $V_D = 0.5$ V. As the nanotube deposition time was increased from 3 min to 7 min, the average on-state current, I_{ON}, defined at $V_G = -10$ V and $V_D = 0.5$ V, increased from 74 nA/μm to 283 nA/μm. In contrast, the on/off ratio, I_{ON}/I_{OFF} (the off-state current, I_{OFF}, is defined at $V_G = 0$ V and $V_D = 0.5$ V), shows the opposite trend, decreasing with increasing nanotube density, as illustrated in Figure 1(c), and this trend is consistent with prior reports.[7,18] Given that 1% of SWNTs in the solution are still metallic, the most straightforward explanation for this observation is that the probability of a metallic interconnection between the source and drain electrodes increased at higher nanotube density. Therefore, it should be noted that the random network deposition method entails an inherent tradeoff between high I_{ON} (with a corresponding high mobility) and I_{ON}/I_{OFF} values.

Next, we evaluated the 90% semiconducting nanotube solution with the random network deposition method, with results shown in Figure 2. With a deposition time of 1 min, a percolation transport pathway in the 90% semiconducting nanotubes was effectively created due to the relatively long nanotube length, as noted above (Figure 2(a)). Importantly, previous reports regarding the random network deposition method have only demonstrated on/off ratios of factor of 2–3 for a relatively short gate length of 4 μm, even with a 95% semiconducting nanotube solution.[17] In this work, however, we obtained an average on/off ratio of almost 10^6 with a 90% semiconducting nanotube solution due to the narrow gate width of 3 μm (Figure 2(b)). In a transistor with a tube density greater than the network percolation threshold, there are many parallel paths, i.e., metallic nanotube paths, carrying current from the source to the drain electrodes. In our

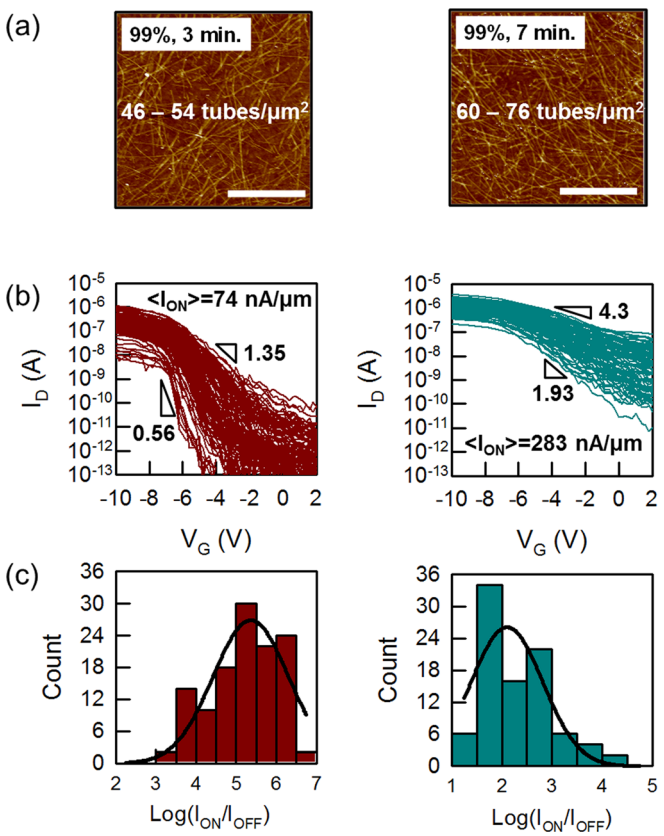

FIG. 1. (a) Resulting AFM images (2.5 μm × 2.5 μm, z-scale is 10 nm) of the networks created from the random deposition method using the 99% semiconducting nanotube solution under the different conditions of 3 min and 7 min. Scale bar, 1 μm. (b) Transfer characteristics (I_D-V_G) for each conditions of 3 min and 7 min at $V_D = 0.5$ V. The subthreshold swing value is inserted in the graph (unit: V/dec). (c) Histograms compiled from the transfer characteristics showing on/off ratios.

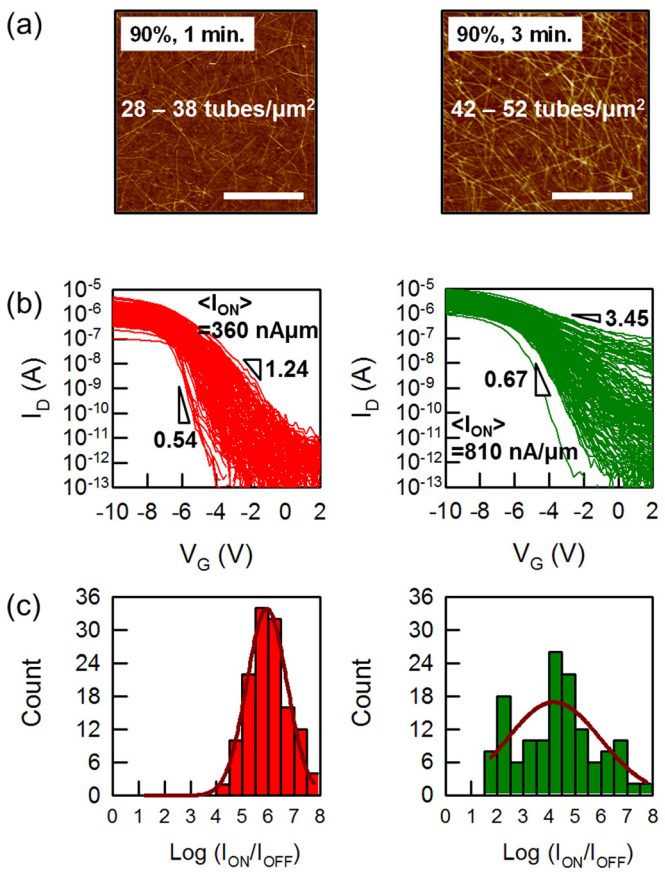

FIG. 2. (a) Resulting AFM images (2.5 μm × 2.5 μm, z-scale is 10 nm) of the networks created from the random deposition method using the 90% semiconducting nanotube solution under the different conditions of 1 min and 3 min. Scale bar, 1 μm. (b) Transfer characteristics (I_D-V_G) for each conditions of 1 min and 3 min at $V_D = 0.5$ V. The subthreshold swing value is inserted in the graph (unit: V/dec). (c) Histograms compiled from the transfer characteristics showing on/off ratios.

device, however, these paths may be broken due to the narrow gate width, resulting in a high on/off ratio.[19] Note that, compared with the results for the 99% semiconducting nanotubes with a 3-min deposition time, the I_{ON} for 90% semiconducting nanotubes with a 1-min deposition time is improved by a factor of ~5, although the 1-min deposition time resulted in a lower nanotube density in the networks. This result is mainly attributed to the fact that the use of long (but still shorter than L_G) and low-density nanotubes leads to fewer nanotube-nanotube junctions and consequently better performance. This finding implies that the use of long as well as high semiconducting enriched nanotube solutions is the optimal way to achieve high-performance devices, i.e., with high I_{ON} and I_{ON}/I_{OFF} values. However, the on/off ratios of the devices fabricated from 90% semiconducting nanotubes with the longer 3-min deposition time still varied over a range of roughly 6 orders of magnitude and the yields of the devices with high on/off ratios were lower than those of the devices fabricated with a 1-min deposition time (Figure 2(c)). Therefore, a trade-off between the on/off ratio and I_{ON} is unavoidable in devices fabricated using the random network deposition method, even with a narrow gate width.

We also evaluated the spin-aligned deposition technique for the formation of networks of partially aligned nanotubes using a solution of 90% semiconducting nanotubes. It has been reported that the spin-aligned method can be used to increase the nanotube density without significantly increasing the number of junction points;[20] however, a certain level of misalignment is also required for percolation, and it is well known that density and alignment directly influence device behavior.[21] Although such progressive devices fabricated using the spin-aligned technique have been reported in the literature, direct comparisons with the random network deposition method are lacking. Here, to investigate the manner in which the topology affects electronic properties and uniformities, we coated the substrate at two spin speeds, 3000 rpm and 7000 rpm, while maintaining the same volume (200 μl) of 90% semiconducting nanotubes. Figure 3 illustrates the results for the spin-aligned deposition method. Note that for the devices fabricated via the spin-aligned technique, the I_{ON} values are higher than those for the random network deposition method (Figure 3(b)). We compared the devices fabricated from 90% semiconducting nanotubes with 3-min random network deposition time and those from 3000-rpm spin-aligned deposition. Although the density of nanotubes with 3000-rpm spin-on deposition was much lower than that with the 3-min random network deposition method, the I_{ON} value is higher by a factor of 1.5–2, most likely due to the high level of misalignment with the random network deposition method, leading to more tube/tube contacts and causing increased channel resistance. However, the on/off ratio still fluctuated over roughly 6 orders of magnitude at a spin speed of 3000 rpm because this speed is inefficient for the formation of highly aligned nanotubes; instead, a large amount of nanotubes adsorb nonspecifically to the existing network, in a manner similar to random network deposition.

Upon comparing AFM results for the fabrications at different spin speeds using the same volume of nanotube solution, the importance of higher spin speed becomes clear (Figure 3(a)). The higher fluidic shear force leads to

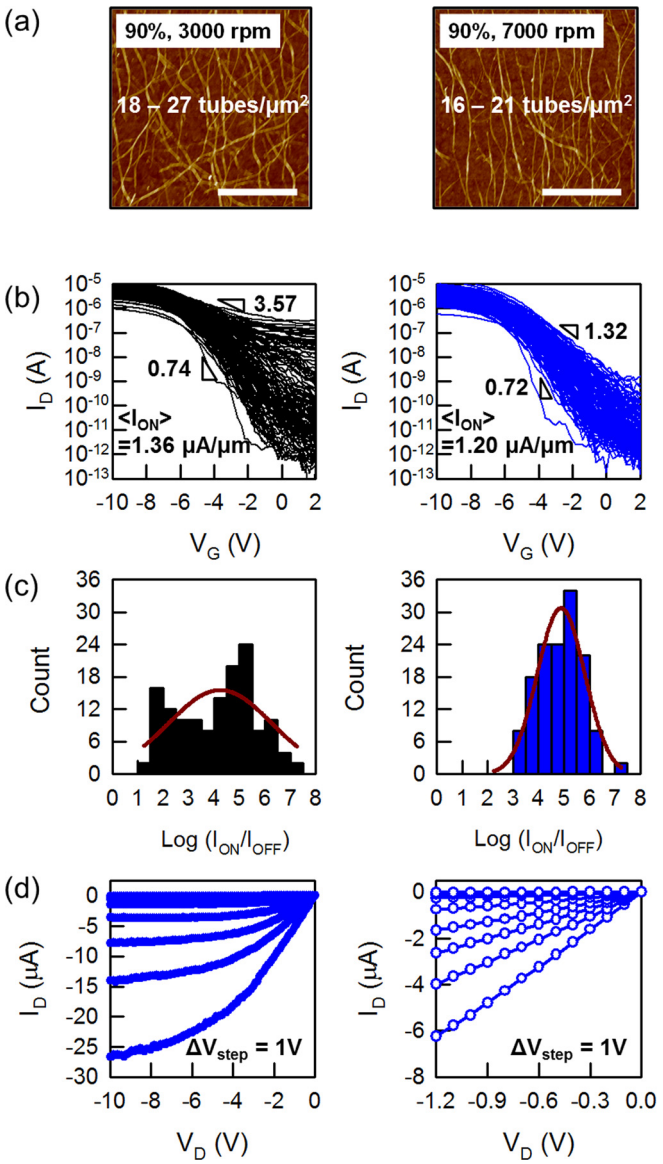

FIG. 3. (a) Resulting AFM images (2.5 μm × 2.5 μm, z-scale is 10 nm) of the networks created from the spin-aligned deposition method using the 90% semiconducting nanotube solution under the different spin speeds of 3000 rpm and 7000 rpm. Scale bar, 1 μm. Because the spin-aligned method results in the radial alignment from the center of the substrate, only upper parts of the chip showing the same direction of the alignment were used for the fabrication of the chip. (b) Transfer characteristics (I_D-V_G) for each conditions of 3000 rpm and 7000 rpm at $V_D = 0.5$ V. The subthreshold swing value is inserted in the graph (unit: V/dec). (c) Histograms compiled from the transfer characteristics showing on/off ratios. (d) Output characteristics (I_D-V_D) of the devices from the spin-aligned method (7000 rpm) for different gate voltages ranging from −10 V to 1 V in 1 V steps.

enhanced alignment, consistent with previous reports.[20] The uniformity of the on/off ratio thus improved significantly at the spin speed of 7000 rpm (Figure 3(c)). Of these device, the highest normalized I_{ON} value obtained, with an on/off ratio of almost 10^5, represent some of the best nanotube network devices, compared to previously reported nanotube network devices. The uniform distribution of on/off ratios is likely because the enhanced alignment effectively reduced the percolation of metallic nanotubes. Therefore, our reproducible results suggest that the spin-aligned technique can be further optimized to extend beyond the random network deposition technique. Figure 3(d) illustrates the output

characteristics (I_D-V_D) of the representative device from the spin-aligned deposition method (7000 rpm) measured in the triode region and saturation region. The I_D-V_D curves appear to be very linear for V_D between 0 and -1.2 V, indicating that ohmic contacts are formed between the electrodes and the nanotubes. Under more negative V_D, the device clearly exhibits saturation behavior. It is worth noting that at faster spin deposition speeds (greater than 9000 rpm with the same volume of nanotubes), the electronic performance did not improve because the nanotube alignment was even more dramatically enhanced, resulting in a failure to form networks (data not shown).

In summary, we experimentally investigated the manner in which network topology affects the electrical properties of thin-film transistors. The results demonstrate that the use of only high semiconducting enriched nanotube solutions is not optimal, as the networks formed actually carry less current than those observed in thin-film transistor consisting of moderate semiconducting enriched nanotube solutions. Moreover, we demonstrated that the fabrication of such transistors via the spin-aligned method can lead to higher current drivability arising from reduced tube/tube contact and can enhance network uniformity, alleviating contamination by metallic tubes.

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[1]E. S. Snow, J. P. Novak, P. M. Campbell, and D. Park, Appl. Phys. Lett. **82**, 2145 (2003).
[2]Y. Zhou, A. Gaur, S. Hur, C. Kocabas, M. A. Meitl, M. Shim, and J. A. Rogers, Nano Lett. **4**, 2031 (2004).
[3]C. Kocabas, M. Meitl, A. Gaur, M. Shim, and J. A. Rogers, Nano Lett. **4**, 2421 (2004).
[4]L. Hu, D. S. Hecht, and G. Gruner, Nano Lett. **4**, 2513 (2004).
[5]S. Kumar, J. Y. Murthy, and M. A. Alam, Phys. Rev. Lett. **95**, 066802 (2005).
[6]A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, Nature **424**, 654 (2003).
[7]T. Takahashi, K. Takei, A. G. Gillies, R. S. Fearing, and A. Javey, Nano Lett. **11**, 5408 (2011).
[8]C. Wang, J.-C. Chien, K. Takei, T. Takahashi, J. Nah, A. M. Niknejad, and A. Javey, Nano Lett. **12**, 1527 (2012).
[9]Q. Cao and J. A. Rogers, Adv. Mater. (Weinheim, Ger.) **21**, 29 (2009).
[10]C. Rutherglen, D. Jain, and P. Burke, Nat. Nanotechnol. **4**, 811 (2009).
[11]S. Kumar, N. Pimparkar, J. Y. Murthy, and M. A. Alam, Appl. Phys. Lett. **88**, 123505 (2006).
[12]M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, Nat. Nanotechnol. **1**, 60 (2006).
[13]M. Engel, J. P. Small, M. Steiner, M. Freitag, A. A. Green, M. C. Hersam, and Ph. Avouris, ACS Nano **2**, 2445 (2008).
[14]C. Wang, J. Zhang, K. Ryu, A. Badmaev, L. G. De Arco, and C. Zhou, Nano Lett. **9**, 4285 (2009).
[15]M. Y. Timmermans, D. Estrada, A. G. Nasibulin, J. D. Wood, A. Behnam, D.-M. Sun, Y. Ohno, J. W. Lyding, E. Pop, and E. I. Kauppinen, Nano Res. **5**, 307 (2012).
[16]W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li, and H. Dai, Nano Lett. **3**, 193 (2003).
[17]C. Wang, J. Zhang, and C. Zhou, ACS Nano **4**, 7123 (2010).
[18]N. Rouhi, D. Jain, K. Zand, and P. Burke, Adv. Mater. **23**, 94 (2011).
[19]Q. Cao, H. Kim, N. Pimparkar, J. P. Kulkarni, C. Wang, M. Shim, K. Roy, M. A. Alam, and J. A. Rogers, Nature (London) **454**, 495 (2008).
[20]M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. Bao, Science **321**, 101 (2008).
[21]C. Kocabas, N. Pimparkar, O. Yesilyurt, S. J. Kang, M. A. Alam, and J. A. Rogers, Nano Lett. **7**, 1195 (2007).