Germanium nanowire field-effect transistors with SiO_2 and high-κ HfO_2 gate dielectrics

Dunwei Wang, Qian Wang, Ali Javey, Ryan Tu, and Hongjie Dai[a)]
Department of Chemistry, Stanford University, California 94305

Hyoungsub Kim and Paul C. McIntyre
Department of Materials Science and Engineering, Stanford University, California 94305

Tejas Krishnamohan and Krishna C. Saraswat
Department of Electrical Engineering, Stanford University, California 94305

(Received 27 May 2003; accepted 23 July 2003)

Single-crystal Ge nanowires are synthesized by a low-temperature (275 °C) chemical vapor deposition (CVD) method. Boron doped *p*-type GeNW field-effect transistors (FETs) with back-gates and thin SiO_2 (10 nm) gate insulators are constructed. Hole mobility higher than 600 $cm^2/V\,s$ is observed in these devices, suggesting high quality and excellent electrical properties of as-grown Ge wires. In addition, integration of high-κ HfO_2 (12 nm) gate dielectric into nanowire FETs with top-gates is accomplished with promising device characteristics obtained. The nanowire synthesis and device fabrication steps are all performed below 400 °C, opening a possibility of building three-dimensional electronics with CVD-derived Ge nanowires. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1611644]

Chemically derived nanotube and nanowire materials have attracted much attention as candidates for future electronic components including field-effect transistors (FETs).[1–6] Currently, for further device scaling and miniaturization, germanium is of renewed interest as an electronic material to complement silicon due to its higher carrier mobility and the trend in gate dielectrics evolution. This letter reports the fabrication of FETs based on Ge nanowires (GeNWs) synthesized by a recently developed low-temperature chemical vapor deposition (CVD) method. Back-gated and top-gated GeNW FETs are constructed, with SiO_2 and high-κ ($\sim$17) HfO_2 gate dielectrics, respectively. Promising device characteristics are obtained with these devices.

GeNWs were synthesized by CVD of germanium at 275 °C on Au nanocolloids (20 nm in diameter),[7] via the vapor–liquid–solid (VLS) growth mechanism.[7,8] To facilitate device integration, patterned growth of GeNWs was carried out using a technique previously developed for patterned growth of carbon nanotubes.[9,10] For synthesis of B-doped GeNWs, 10 ppm B_2H_6 in H_2 was used in the CVD. This simple low-temperature CVD method reliably yielded single-crystal GeNWs with average diameters $\sim$20 nm and lengths $\sim 10\mu$m (Fig. 1). After CVD, the substrate was heated in air at 400 °C for 2 h to activate B dopants in the GeNWs, followed by a HCl etch to remove the germanium oxide layer on the nanowires. GeNWs emanating from the patterned growth sites were then contacted by metal source (S) and drain (D) electrodes by lithography on a polymer resist, metal evaporation and liftoff.[10] Arrays of two terminal GeNWs were obtained on a single chip, with a yield of $\sim$30% for devices comprising of single wires bridging S and D determined by scanning electron microscopy imaging of the device array.

The first type of GeNW FETs used the back-gate configuration [Fig. 2(a)], with SiO_2 ($t_{ox}=10$ nm) as gate dielectric and Pd as the S/D contact metal. The Pd contacts were annealed in Ar at 250 °C for 1 h in order to obtain ohmic contact.[11] The S–D distances (channel lengths) are $L=5\ \mu$m [Fig. 2(b) inset]. Typical current versus gate voltage [I_{ds} versus V_{gs}, Fig. 2(b)] and current versus S–D bias voltage [I_{ds} versus V_{ds}, Fig. 2(c)] characteristics of the back-gated GeNW ($\sim$20 nm in diameter) FETs exhibit $I_{ON}/I_{OFF}=10^3$, linear resistances of 500 kΩ for the ON state, subthreshold slope of $S\sim 300$ mV/decade, transconductance in the linear triode region ($V_{ds}=-0.1$ V) $g_m=dI_{ds}/dV_{gs}=0.21\ \mu$S, and maximum ON state current on the order of $\sim 3\ \mu$A per GeNW. Devices made from GeNWs grown in the absence of B_2H_6 during CVD are highly insulating under a wide range of V_{gs}. This suggests that B-doping of GeNWs is effective when diborane is introduced to the CVD growth system.

To estimate the hole carrier mobility in the back-gated GeNW FETs, we first calculate the coupling capacitance be-

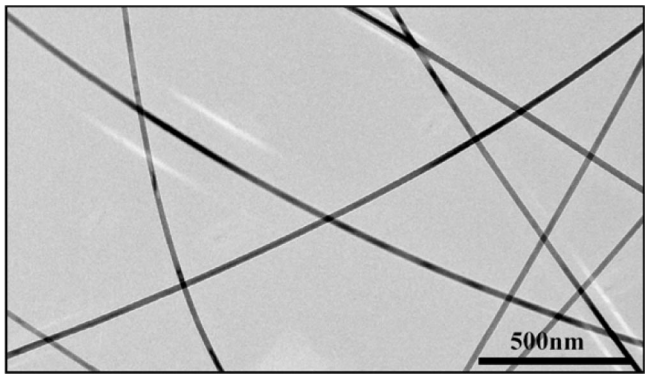

FIG. 1. Single-crystal GeNWs synthesized at 275 °C. A low-magnification transmission electron microscopy (TEM) image showing abundant $\sim$20-nm-diameter GeNWs grown from $\sim$20-nm Au colloids.

a)Electronic mail: hdai@stanford.edu

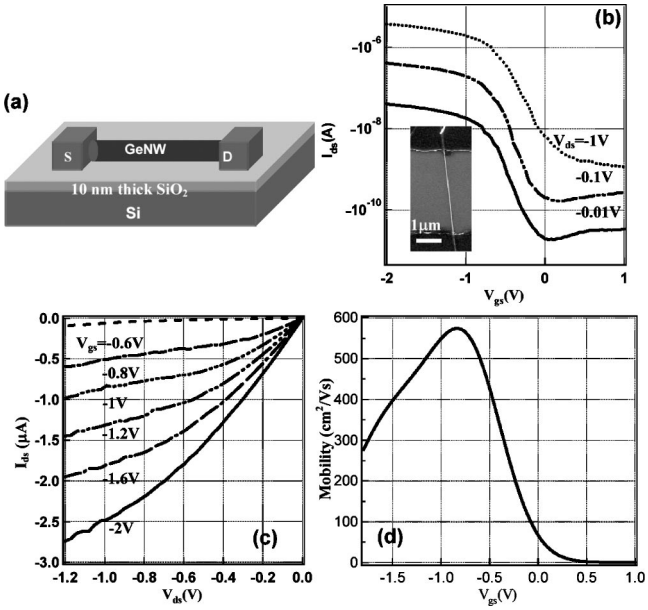

FIG. 2. GeNWs FETs with back-gates and 10-nm-thick SiO_2 as the gate insulator: (a) A schematic side view of the device. (b) I_{ds} vs V_{gs} curves. Inset: a top scanning electron microscope (SEM) view of a device, showing S/D electrodes and a single GeNW bridging the S/D. (c) I_{ds} vs V_{ds} characteristics for the device in (b). (d) Hole mobility vs gate voltage estimated from the transconductance of the device. Note that the $I_{ds}-V_{gs}$ curve in (b) was smoothed before the transconductance dI_{ds}/dV_{gs} was calculated.

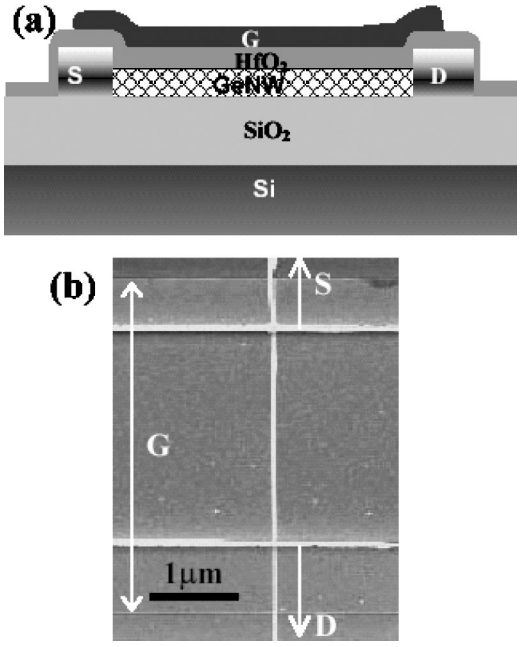

FIG. 3. Device structure of GeNWs FETs with top-gates and 12-nm-thick HfO_2 gate dielectric. (a) A schematic side view of the device. The gate electrode is at the very top of the surface in the image, overlapping with S and D by ~0.5 to 1 μm. (b) A top SEM view of a device.

tween the GeNW channel and the back-gate through the t_{ox} = 10-nm-thick SiO_2 gate dielectric. Within the cylinder-on-plate model, the capacitance is,[12]

$$C_{ox}=\frac{2\pi\varepsilon_0\varepsilon L}{\cosh^{-1}\left(\frac{r+t_{ox}}{r}\right)}, \tag{1}$$

where $\varepsilon\sim3.9$ is the dielectric constant of SiO_2, $L\sim5$ μm is the GeNW channel length, and $r=10$ nm is radius of the GeNW. The estimated gate capacitance is then $C_{ox}\sim0.82$ fF (0.16 fF per 1 μm of channel length). Next, we assume the metal-oxide semiconductor field-effect transistor (MOSFET) model[13] and use the $I_{ds}-V_{ds}$ characteristics of the GeNW FETs in the linear triode region to deduce the hole mobility via

$$\mu=\frac{dI_{ds}}{dV_{gs}}\times\frac{L^2}{C_{ox}}\times\frac{1}{V_{ds}}. \tag{2}$$

With this method, we extract a hole-mobility versus gate-voltage plot [Fig. 2(d)] that exhibits a shape similar to that expected for the universal mobility curve with a low field hole mobility of $\mu\sim600$ cm^2/V s.[14] We note, however, that hysteresis does exist in the current versus gate sweeps for these prepared devices from as-grown GeNWs without intentional surface passivation. Our transconductance and mobility estimate takes this factor into account and is conservative as it is based on data of the sweep direction that reveals the lower performance characteristics. As a comparative note, there has been no report on hole mobility in transistors built with chemically synthesized GeNWs thus far. In the literature, data on MOSFETs constructed with Ge wafers by the lithography method are scarce. The highest hole mobility reported for Ge MOSFETs is ~700 cm^2/V s.[11] Hole mobility in bulk single-crystal Ge is 1800 cm^2/V s.

The second type of GeNW FETs consisted of a top-gate and a 12-nm-thick high-κ ($\kappa\sim17$) HfO_2 gate insulator layer grown on top of the GeNWs by atomic layer deposition (ALD)(see Fig. 3).[15–17] The initial steps of device fabrication were nearly identical to those involved in making the back-gate devices, except that the SiO_2 thickness of the SiO_2/Si substrate used here was 500 nm, and Ti(30 nm)/W(3 nm) were used as S and D electrodes (S–D distance $L=3$ μm in this case). A 12-nm-thick HfO_2 was deposited on the devices at 300 °C using alternating surface-saturating reactions of $HfCl_4$ and H_2O.[16,17] The use of W as the top layer of the S and D electrodes afforded a conformal layer[17] of HfO_2 on the S/D and SiO_2 substrate. Following ALD, electron-beam lithography, metal (15 nm Ti) evaporation, and liftoff were used to fabricate the top-gate, with slight overlap with the S and D. The conformal coverage of HfO_2 on all surface structures on the substrate gave negligible leakage current (<10 pA) between the top-gate and S/D for $|V_{gs}|<3$ V.

Typical $I_{ds}-V_{gs}$ and $I_{ds}-V_{ds}$ characteristics of the top-gate HfO_2 GeNW FETs are shown in Fig. 4. The device exhibits $I_{ON}/I_{OFF}=10^3$, linear resistances ~500 kΩ for the ON state, subthreshold slope $S\sim750$ mV/decade, transconductance in the linear triode region $g_m=dI_{ds}/dV_{gs}=0.19$ μS and maximum ON state current on the order of ~3 μA per GeNW. We estimate the peak low-field hole mobility, for the top-gated GeNW FET with ALD HfO_2 as gate insulator, to be around 200 cm^2/V s from simulations using MEDICI (two-dimensional device simulator).[18]

The GeNW FET results obtained by the current work are interesting in several ways. First, hole mobility of 600 cm^2/V s is obtained with the back-gated GeNWs FETs. The mobility is close to the highest value ever reported for Ge MOSFETs[11] built on Ge wafers, and points to the high quality and excellent electrical properties of the as-grown GeNWs by our CVD method. Second, in the GeNW FETs with HfO_2 gate insulators, a high-κ gate dielectric is inte-

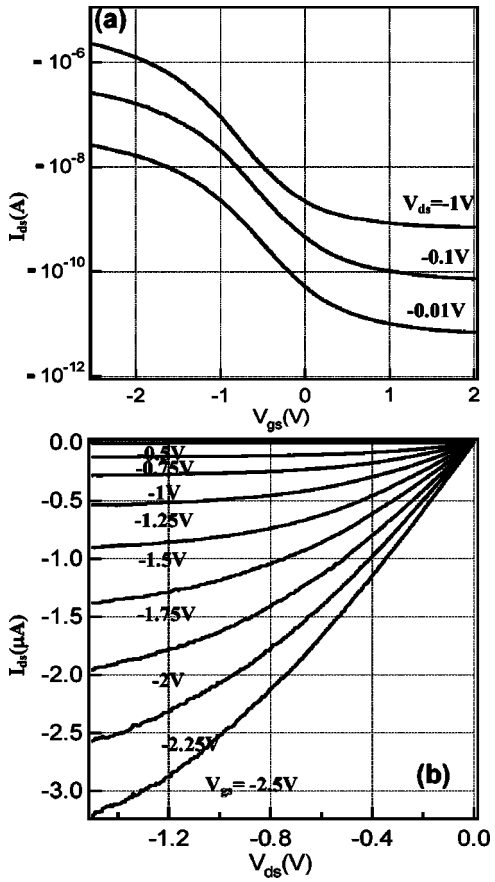

FIG. 4. Electrical properties of GeNWs FETs with HfO_2 gate dielectric: (a) I_{ds} vs V_{gs} curves for a device. (b) I_{ds} vs. V_{ds} recorded under various gate voltages for the device.

grated into nanowire-based transistors. This is a significant step towards channel length scaling of nanowire transistors. Third, the growth and processing for the GeNW FETs are all carried out below 400 °C, which raises the possibility of three-dimensional integration of electronic devices on any substrates. It is conceivable to build multiple layers (with proper insulation between layers) of GeNW devices (or GeNW electronics on a conventional Si-complementary MOS layer) at these temperatures without adversely affecting the devices in the underlying layers. The current GeNW device work, however, represents only a beginning of systematic research on GeNW FETs, and the devices are far from optimized. The back-gate structure does not require post-growth deposition of dielectric materials on the surfaces of GeNWs, which should retain most of the intrinsic properties of the nanowires, thus providing a model system for the investigation of electron transport in the as-grown wires. The device characteristics, however, are nonideal, as manifested by the relatively large subthreshold swings ($S \sim 300$ mV/decade) as opposed to the theoretical limit of ~60 mV/decade.[13] This problem and the existence of hysteresis are likely to be caused by surface states on the nonpassivated Ge wires or interface states between the GeNW and the underlying SiO_2 substrate. S and D metal contacts to the GeNWs may not be perfectly ohmic, which could give rise to a high parasitic resistance at the contacts.

The GeNW FETs with ALD HfO_2 gate insulators exhibit further reduced performance from the back-gated devices, with a higher S of ~750 mV/decade and lower mobility. This is attributed to interface states between the HfO_2 and GeNWs and increased carrier scattering in the nanowire, caused by the deposition of HfO_2. Such a problem is well known for Si and Ge MOSFETs caused by dielectric film deposition on Si and Ge channels.[19] Nevertheless, the GeNW FETs with high-κ gate dielectrics exhibit promising characteristics, and the performance is at least comparable to that of Ge MOSFETs with HfO_2 gate insulators[20] fabricated on Ge wafers by lithography. For optimization of the GeNW transistors, future work on ohmic contacts and surface and interface passivation is clearly required.

In summary, we have presented single crystalline GeNWs grown by a low-temperature CVD method for building nanowire-based FETs. The individual Ge nanowire devices exhibit promising electrical properties. Integration of high-κ dielectrics into nanowire transistors has been carried out. The device characteristics and low-temperature fabrication processes suggest that GeNWs are promising building blocks for advanced electronic devices.

One of the authors (H.D.) acknowledges support from MARCO/MSD, DARPA Moletronics and SRC/AMD. Other supports include a Mayfield Stanford Graduate Fellowship (H.K.), and an IBM Faculty Award (P.C.M.), a Packard Fellowship, and a Dreyfus Teacher-Scholar Award.

[1] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundsfrom, and H. Dai, Nature Materials **1**, 241 (2002).
[2] L. J. Lauhon, M. S. Gudiksen, D. Wang, and C. M. Lieber, Nature (London) **420**, 57 (2002).
[3] P. Yang, Y. Wu, and R. Fan, Int. J. Nanosci. **1**, 1 (2002).
[4] Yi Cui, Deli Wang, W. U. Wang, and C. M. Lieber, Nano Lett. **3**, 149 (2003).
[5] J.-Y. Yu, S.-W. Chung, and J. R. Heath, J. Phys. Chem. **104**, 11864 (2000).
[6] D. Zhang, C. Li, S. Han, X. Liu, T. Tang, W. Jin, and C. Zhou, Appl. Phys. Lett. **82**, 112 (2003).
[7] D. Wang and H. Dai, Angew. Chem., Int. Ed. Engl. **41**, 4783 (2002).
[8] Y. Wu and P. Yang, J. Am. Chem. Soc. **123**, 3165 (2001).
[9] J. Kong, H. Soh, A. Cassell, C. F. Quate, and H. Dai, Nature (London) **395**, 878 (1998).
[10] H. Soh, C. Quate, A. Morpurgo, C. M. Marcus, J. Kong, and H. Dai, Appl. Phys. Lett. **75**, 627 (1999).
[11] L. M. H. a. J. J. R. S. C. Martin, IEEE Electron Device Lett. **10**, 325 (1989).
[12] S. Ramo, J. R. Whinnery, and T. V. Duzer, *Fields and Waves in Communication Electronics* (Wiley, New York, 1994).
[13] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[14] K. Chen, H. Wann, P. Ko, and C. Hu, IEEE Electron Device Lett. **17**, 202 (1996).
[15] M. Leskela and M. Ritala, Thin Solid Films **409**, 138 (2002).
[16] H. Kim, P. C. McIntyre, and K. C. Saraswat, Appl. Phys. Lett. **82**, 106 (2003).
[17] S.-Y. Lee, H. Kim, P. C. McIntyre, K. C. Saraswat, and J. S. Byun, Appl. Phys. Lett. **82**, 2874 (2003).
[18] T. Krishnamohan, Z. Krivokapic, and K. Saraswat, in *IEEE Int. Conf. Simul. Semi. Proc. and Dev.*, 2003.
[19] S. B. Samavedam, H. H. Tseng, P. J. Tobin, J. Mogab, S. Dakshina-Murthy, L. B. La, J. Smith, J. Schaeffer, M. Zavala, R. Martin, B. Y. Nguyen, L. Hebert, O. Adetutu, V. Dhandapani, T. Y. Luo, R. Garcia, P. Abramowitz, M. Moosa, D. C. Gilmer, C. Hobbs, W. J. Taylor, J. M. Grant, R. Hegde, S. Bagchi, E. Luckowski, V. Arunachalam, M. Azrak, *VLSI Tecc. Dig. Tech. Papers 2002 Symp.*, p. 24.
[20] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, Tech. Dig. - Int. Electron Devices Meet. (in press).