

Mimicking the Human Brain and More: New Grand Challenge Initiatives

After President Obama announced the BRAIN Initiative,^{1,2} there was a call for suggestions of other grand challenges for which the great advances and investments in nanoscience and nanotechnology could be fruitfully applied.^{3–6} After considering over 100 responses, the White House recently announced “A Nanotechnology-Inspired Grand Challenge for Future Computing”.⁶ There may yet be more.

Since the discovery of the first solid-state electronic switch in 1947,⁷ transistor dimensions have been aggressively down-scaled to enhance their functionality, performance, and speed, while lowering the manufacturing cost. Today's 14-nm technology node⁸ utilizes Si that is patterned into “fins”⁹ with a minimum fin thickness of 8 nm (corresponding to ~15 Si atoms across), and a minimum gate length of 20 nm. One can argue that the transistors of today are already at the molecular scale. A typical 14-nm node processor has a die size of 80–130 mm² with 1.3–1.9 billion transistors. More than half of the die area is typically allocated to memory.

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Throughout this evolutionary path, the layout of the transistors and circuits has remained planar, meaning that the active components are laid out side-by-side (with only a few exceptions). Today's processors can perform computation at unprecedented speeds. For instance, complex mathematical problems that would have been considered nearly impossible to solve by a human can be readily computed using today's processors. Yet, when it comes down to data processing, for instance, of an image or a video, the human brain remains far superior despite the tremendous progress that has been made in the field of image processing. It is incredible how the human sensory nervous system can use data from multitude of senses, such as sight, hearing, taste, smell, and touch to form a concept of its environment instantaneously and to deliver a rapid response. Importantly, the brain uses minimal *energy* compared to state-of-the-art computer processors for handling such operations. Finally, unlike today's processors, the human brain has the ability to learn and to develop from daily experiences, which makes it even more efficient in processing sensory data. This effect exists throughout our lives but is most remarkably apparent in the early development stages.

The human brain consists of a complex three-dimensional (3D) network of ~100 billion neurons, with each neuron interconnected to as many as 10 000 other neurons. While the basic structure of the brain is known, the underlying mechanistic details of its operation are still not well understood. The BRAIN Initiative was announced by the White House in 2013 to facilitate research that would provide us with a better understanding of this complex and remarkable organ.^{1,2} It is understood that each neuron is not just a switch but rather a sophisticated circuit that takes positive and negative inputs from multiple other neurons to determine its outputs. The interconnection between different neurons evolves through learning and memory. In other words, the brain is a reconfigurable processor.

Developing a new class of computer processors that in some ways function like a human brain by more efficiently processing large data sets is of utmost interest. Given the low manufacturing cost of electronics, we have seen sensors being implemented all around us in a seamless fashion. Example sensors include outdoor/indoor temperature, air quality, home security, motion detectors for lighting or air control, location and navigation, pulse rate and health monitoring, and more. Make no mistake, this proliferation is just the beginning of exponential growth. It is projected that within the next 10 years, over a trillion electronic sensors will be wirelessly integrated that can supply us with a continuous wealth of information displayed on hand-held devices such as smart phones or smart watches. That corresponds to roughly a thousand sensors per person in the world. One challenge,

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however, is to develop processors powerful enough that can instantaneously process such large volumes of data and provide us with useful information about our health, security, and environment.

One approach to achieve the above objective is to use the third dimension in assembling active electronic switches to form monolithic 3D circuits (Figure 1).¹⁰ Doing so not only presents a new dimension for increasing the device density per unit area of a die but also enhances performance and functionality by enabling new architectures. For instance, in this design layout, logic and memory components can be vertically integrated with only tens of nanometers spacing as opposed to millimeter or more separation of today's proces-

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sors. A challenge with monolithic 3D integration, however, is layer-by-layer processing of high-quality semiconductors and devices. Development of electronic materials that can be processed at low temperatures, without damaging the underlying device layers, is a necessity. In this regard, the use of layered transferred thin films or directly grown one- or two-dimensional semiconductors is an attractive approach.¹¹ However, with 3D device integration, power consumption and heat dissipation need to be carefully addressed. Of particular importance is the development of a new electronic switch that can operate at significantly lower voltages (and thus power) than conventional metal oxide semiconductor field-effect transistors (MOSFETs). Heat dissipation is already a challenge for today's electronics where active switches are laid out in 2D. By stacking the devices in the third dimension, heat dissipation becomes even more challenging. Research in this area needs to be further expanded to explore a new switch capable of operating by a few millivolts (rather than hundreds of millivolts, which is the lower operating bound of MOSFETs). This advance would present a $\sim 10\,000\times$ reduction of power consumption per switch. Research directions toward this goal include tunneling transistors, which operate based on a different switching mechanism, and negative capacitance transistors, which provide an internal voltage up-converter. However, both directions have proven to be challenging. While the former looks promising in modeling and simulations, experimental results have been rather poor partly because of the materials' nonidealities, including defects. On the other hand, negative capacitance transistors have not yet been shown to exhibit significant advantages over traditional MOSFETs, with recent theoretical work showing only a 2–3 \times reduction in power; while impressive, it is not sufficiently large to meet the future needs. Improving materials quality at the atomic scale and exploring new material systems free of defects is critical for tunnel transistors. In fact, this materials demand is true for *any* future device architecture to ensure uniformity and performance. As noted above, today's transistors are already at the molecular (or macromolecular) scale. Chemists have for years developed synthetic approaches for producing molecules with perfect arrangements of atoms. Perhaps, concepts from synthetic chemistry can be applied to future semiconductor materials. Furthermore, the search for a new millivolt switch must be expanded in the future.

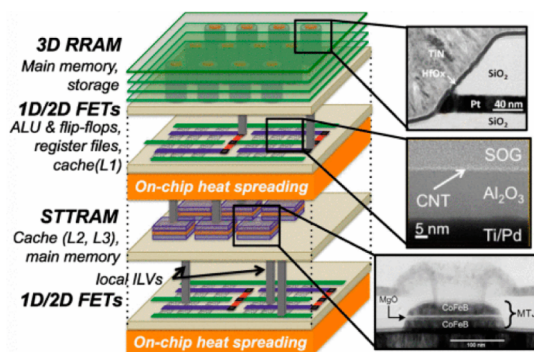


Figure 1. Example conception of monolithic 3D electronics. Reproduced with permission from ref 10. Copyright 2014 IEEE.

It is worth noting that heat dissipation is also an issue in the human brain. In fact, a large fraction of the human brain volume is allocated for heat dissipation and energy delivery.¹² Besides exploration of low-power devices, new schemes for heat management may prove necessary for future 3D electronics. Finally, reconfigurable circuit architectures may be an attractive path for the development of processors that can learn and evolve over time. In this regard, memristors could also play important roles as significant materials advances have been made in this field over the past several years.^{13,14}

It is an exciting time for the field of electronic materials and devices. The challenges are immense, and so are the opportunities and potential impact. To meet future needs, interdisciplinary approaches are needed; merging the expertise of chemists, chemical engineers, physicists, device engineers, and circuit and system designers. Chemists, chemical engineers, and physicists enabled and started the Si integrated circuit (IC) industry. They played critical roles in developing microfabrication process technologies and establishing the solid-state physics that has driven the engineering of today's electronic devices. They were also many of the founders of the major IC companies that now exist. Moving forward, the roles of chemists and nanoscientists will be equally important as we have reached device dimensions where atomic-scale control of composition is a necessity. Since its first issue, *ACS Nano* has promoted research in nanoscale electronic materials, advanced materials characterization techniques at the atomic scale, nanofabrication processes, and new device architectures that can serve as the building blocks for the "Nanotechnology-Inspired Grand Challenge for Future Computing" recently announced by the White House.⁶

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Ali Javey
Associate Editor



Paul S. Weiss
Editor-in-Chief

REFERENCES AND NOTES

- Weiss, P. S. President Obama Announces the BRAIN Initiative. *ACS Nano* **2013**, *7*, 2873–2874.
- Alivisatos, A. P.; Andrews, A. M.; Boyden, E. S.; Chun, M.; Church, G. M.; Deisseroth, K.; Donoghue, J. P.; Fraser, S. E.; Lippincott-Schwartz, J.; Looger, L. L.; *et al.* Nanotools for Neuroscience and Brain Activity Mapping. *ACS Nano* **2013**, *7*, 1850–1866.
- Wackler, T. Nanotechnology-Inspired Grand Challenges for the Next Decade. *Federal Register* **2015**, *80*, 34713–34715.
- Parak, W. J.; Nel, A. E.; Weiss, P. S. Grand Challenges for Nanoscience and Nanotechnology. *ACS Nano* **2015**, *9*, 6637–6640.
- Whitman, L.; Weiss, P. S.; Schmidt, D. G. Nanotechnology-Inspired Grand Challenges, <http://www.acs.org/content/acs/en/acs-webinars/grand-challenge.html> (accessed November 4, 2015).
- Whitman, L.; Bryant, R.; Kalil, T. A Nanotechnology-Inspired Grand Challenge for Future Computing, <https://www.whitehouse.gov/blog/2015/10/15/nanotechnology-inspired-grand-challenge-future-computing> (accessed November 4, 2015).
- Shockley, W. B.; Bardeen, J.; Brattain, W. H. The Nobel Prize in Physics, <http://www.nobelprize.org/nobelprizes/physics/laureates/1956>, 1956 (accessed November 15, 2015).
- Natarajan, S.; Agostinelli, M.; Akbar, S.; Bost, M.; Bowonder, A.; Chikarmane, V.; Chouksey, S.; Dasgupta, A.; Fischer, K.; Fu, Q.; *et al.* A 14 nm Logic Technology Featuring 2nd-Generation FinFET, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 μm^2 SRAM Cell Size. *Electron Devices Meeting (IEDM)* 2014, pp 3–7.

9. Hisamoto, D.; Lee, W.-C.; Kedzierski, J.; Takeuchi, H.; Asano, K.; Kuo, C.; Anderson, E.; King, T.-J.; Bokor, J.; Hu, C. FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm. *IEEE Trans. Electron Devices* **2000**, *47*, 2320–2325.
10. Ebrahimi, M. S.; Hills, G.; Sabry, M. M.; Shulaker, M. M.; Wei, H.; Wu, T. F.; Mitra, S.; Wong, H.-S. P. Monolithic 3D Integration Advances and Challenges: From Technology to System Levels. *SOI-3D-Subthreshold Microelectronics Technology Unified Conference* **2014**, 1–2.
11. Javey, A.; Nam, S.; Friedman, R. S.; Yan, H.; Lieber, C. M. Layer-by-Layer Assembly of Nanowires for Three-Dimensional, Multifunctional Electronics. *Nano Lett.* **2007**, *7*, 773–777.
12. Wang, H.; Wang, B.; Normoyle, K. P.; Jackson, K.; Spitler, K.; Sharrock, M. F.; Miller, C. M.; Best, C.; Llano, D.; Du, R. Brain Temperature and Its Fundamental Properties: A Review for Clinical Neuroscientists. *Front. Neurosci.* **2014**, *8*, 307.
13. Chang, T.; Jo, S.-H.; Lu, W. Short-Term Memory to Long-Term Memory Transition in a Nanoscale Memristor. *ACS Nano* **2011**, *5*, 7669–7676.
14. Xia, Q.; Robinett, W.; Cumbie, M. W.; Banerjee, N.; Cardinali, T. J.; Yang, J. J.; Wu, W.; Li, X.; Tong, W. M.; Strukov, D. B.; *et al.* Memristor—CMOS Hybrid Integrated Circuits for Reconfigurable Logic. *Nano Lett.* **2009**, *9*, 3640–3645.