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## **Field-Effect** Transistors Built from All **Two-Dimensional Material Components**

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We demonstrate field-effect transistors using heterogeneously stacked two-dimensional materials for all of the components, including the semiconductor, insulator, and metal layers. Specifically, MoS<sub>2</sub> is used as the active channel material, hexagonal-BN as the top-gate dielectric, and graphene as the source/ drain and the top-gate contacts. This transistor exhibits n-type behavior with an ON/OFF current ratio of  $>10^6$ , and an electron mobility of  $\sim$ 33 cm<sup>2</sup>/V·s. Uniquely, the mobility does not degrade at high gate voltages, presenting an important advantage over conventional Si transistors where enhanced surface roughness scattering severely reduces carrier mobilities at high gate-fields. A WSe2-MoS2 diode with graphene contacts is also demonstrated. The diode exhibits excellent rectification behavior and a low reverse bias current, suggesting high quality interfaces between the stacked layers. In this work, all interfaces are based on van der Waals bonding, presenting a unique device architecture where crystalline, layered materials with atomically uniform thicknesses are stacked on demand, without the lattice parameter constraints. The results demonstrate the promise of using an all-layered material system for future electronic applications.

KEYWORDS: layered materials · transition metal dichalcogenides · graphene · hexagonal boron nitride · MoS<sub>2</sub> · heterolayers

wo-dimensional (2-D) material systems have aroused immense interest in research due to the possibility of obtaining thickness uniformity down to a monolayer without surface dangling bonds. Graphene (Gr), as a two-dimensional semimetal has been studied extensively for the purpose of analog and digital applications. However, the absence of an intrinsic bandgap in Gr overshadows its attractive properties of small quantum capacitance and extremely high mobilities in scaled transistors.<sup>1–3</sup> Transition metal dichalcogenides (TMDC), with an inherent bandgap, tunable by composition and the number of layers, have ignited significant interest and promise over the past few years for both

electronic and optoelectronic applications.<sup>4–7</sup> For instance, MoS<sub>2</sub> and WSe<sub>2</sub> have been used to obtain excellent switching current ratios (up to 10<sup>8</sup>), and ideal subthreshold slope (60 mV/decade).<sup>8-12</sup> One of the primary advantages of layered materials is, in principle, the absence of dangling bonds, which rules out performance degradation due to interface states.<sup>13</sup> Uniquely, heterostructures using two-dimensional materials would not suffer from constraints of lattice mismatch. A layered material can be seamlessly transferred onto another, and bond by van der Waal's (vdW) forces, leaving the interface pristine. An ideal transistor structure would, therefore, be composed of a TMDC material as the channel, with a

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Figure 1. Schematics (not to scale) of the fabrication process steps (top) and the corresponding optical microscope images (bottom) of a representative all-2D FET. (i) Transfer of large-area CVD grown bilayer graphene onto a Si/SiO<sub>2</sub> substrate. (ii) Bilayer graphene patterning by O<sub>2</sub> plasma to define S/D contacts. (iii) Transfer of a few-layer MoS<sub>2</sub> flake on top of the patterned grahene S/D contacts. (iv) Transfer of a few-layer h-BN gate dielectric, overlapping the MoS<sub>2</sub> channel. (v) Transfer of a multilayer graphene top gate electrode. (vi) Optical microscope image of a fully fabricated all-2D transistor. Scale bar is 5  $\mu$ m for all images.

layered insulator as the gate dielectric, and layered metallic source/drain and gate contacts. Atomically thin p-n diodes have been reported, using MoS<sub>2</sub> and WSe<sub>2</sub> monolayers as the electron and hole conducting layers, respectively.<sup>14–16</sup> These vdW heterostructure diodes have exhibited excellent rectification behavior owing to the abruptness of the 2D-2D interface, with ideality factor of 1.2. MoS<sub>2</sub> transistors with graphene source/drain contacts have been used to fabricate flexible, transparent transistors.<sup>17</sup> Also, flexible and transparent MoS<sub>2</sub> transistors with graphene source/ drain contacts were fabricated with h-BN as back gate dielectric, demonstrating negligible hysteresis in transport characteristics.<sup>18</sup> Heterostructures with 2D materials have been used for memory applications and tunnel transistors. Gr/MoS2 heterostructures have been used for nonvolatile memory cells.<sup>19</sup> Tunnel transistors fabricated with Gr/hexagonal-BN (h-BN)/Gr and Gr/MoS<sub>2</sub>/Gr open the prospect of obtaining steep transistors with such an architecture.<sup>20</sup> Vertical Gr/h-BN/Gr heterostacks have also exhibited negative differential resistance, allowing the prospect of vdW heterostructures in analog electronics.<sup>21</sup> Gr/WS<sub>2</sub>/Gr heterostructures have demonstrated strong lightmatter interactions, leading to enhanced photon absorption and electron-hole creation.<sup>22</sup> This has opened the possibility of flexible photovoltaic devices with layered 2D materials. Heterobilayers of WSe<sub>2</sub> and MoS<sub>2</sub> have shown strong interlayer coupling with spatially direct absorption and spatially indirect emission, exhibiting yet another unique property of TMDC heterostructures. TMDC heterojunctions with III-V, Si, and carbon nanotubes have also been explored previously, demonstrating electrically active vdW interfaces built from highly dissimilar semiconductors.<sup>23–26</sup> However, a transistor made completely from twodimensional materials to leverage the absence of interface states with digitally controlled and atomically uniform thickness has not been reported so far. In this work, we use large area chemical vapor deposited

(CVD) Gr to contact few-layer MoS<sub>2</sub> crystals. We use exfoliated hexagonal boron nitride as the layered gate dielectric and exfoliated Gr as the top-gate contact. The resulting field-effect transistor (FET) made completely of layered materials exhibits a high ON/OFF current ratio of >10<sup>6</sup>, with a MoS<sub>2</sub> electron mobility of 33 cm<sup>2</sup>/V·s. We also demonstrate the rectification behavior of an all-2D diode, using MoS<sub>2</sub>–WSe<sub>2</sub> heterojunction contacted with Gr as the source/drain electrodes.

Figure 1 shows the fabrication steps and corresponding optical images of a representative all-2D FET. The details of the process are as follows. CVD grown bilayer or monolayer Gr on a Cu foil was coated with PMMA. The PMMA-coated substrate was treated with dilute HNO<sub>3</sub> and the Cu was etched by inserting the foil into an ammonium persulfate solution bath for 18 h. After the Cu foil was completely etched away, the floating PMMA coated Gr was scooped out of the bath and transferred onto a Si/SiO<sub>2</sub> (260 nm) substrate (Figure 1(i)). The sample was baked at 220 °C for 5 min to improve Gr adhesion on the SiO<sub>2</sub> surface followed by PMMA removal using acetone.<sup>27,28</sup> Ni/Au (30 nm/ 30 nm) bond pads were then formed by electron-beam (e-beam) lithography, evaporation and resist lift-off. Gr was subsequently patterned using e-beam lithography and oxygen plasma etching to define the S/D electrodes of the FET (Figure 1(ii)). MoS<sub>2</sub>, h-BN, and Gr multilayers as the active channel, gate dielectric, and the gate electrode, respectively, were sequentially stacked on the Gr S/D contacts using a pick and transfer process. Specifically, MoS<sub>2</sub>, h-BN and Gr multilayers were first exfoliated onto Si/SiO<sub>2</sub> process substrates. Flakes of interest were patterned into rectangular shapes with desired dimensions using electron-beam lithography and dry etching. MoS<sub>2</sub> and h-BN were etched using XeF<sub>2</sub>, and Gr was etched using O<sub>2</sub> plasma. The substrates were then spin coated with PMMA (6  $\mu$ m in thickness). PMMA was used as a carrier layer to pick the flake of interest off the substrate, and to

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Figure 2. Back-gated few-layer MoS<sub>2</sub> FET with monolayer graphene contacts. The  $p^+$  Si substrate is used as the back-gate. (a) Device schematic (not to scale). (b)  $I_D - V_G$  curves at different  $V_D$ . (c)  $I_D - V_D$  characteristics.

dry-transfer onto the device substrate. First, using an engraver, the PMMA slab around the patterned flake of interest was cut under an optical microscope. The slab was poked from all sides to release from the SiO<sub>2</sub> substrate. The PMMA slab with the flake was then picked with a needle under a microscope, and transferred onto the targeted area on the device substrate. The sample was subsequently annealed at 180 °C for 2 min after each transfer step to improve the adhesion of the transferred flakes to the substrate. The PMMA carrier layer was removed by immersion in dichloromethane after each transfer step. With this dry transfer method, a MoS<sub>2</sub> flake was transferred in between the prepatterned Gr S/D contacts (overlapping each Gr contact) to form the active channel (Figure 1(iii)). A h-BN flake was then dry-transferred onto the MoS<sub>2</sub> channel area to form the gate dielectric (Figure 1(iv)) followed by the transfer of a multilayer Gr flake to form the top-gate contact (Figure 1(v)). The device was annealed in forming gas (5% H<sub>2</sub>, 95% N<sub>2</sub>) for 3 h at 200 °C in order to improve the interface properties. An optical image of a fully fabricated FET is shown in Figure 1(vi). Note that the alignment accuracy for this manual pick and transfer process is  $\sim 2 \mu m$ . In fact, for the specific device shown in Figure 1, there is  $\sim 2 \,\mu m$ misalignment between the Gr gate and S/D electrodes. This results in a gate underlapped MoS<sub>2</sub> region which contributes to the parasitic resistance of the device, but otherwise does not restrict the switching behavior. In principle, the alignment accuracy and yield can be improved in the future by using an automated pick and transfer process. MoS<sub>2</sub>/WSe<sub>2</sub> heterojunction diodes with Gr contacts were also fabricated using a similar transfer approach, except that MoS<sub>2</sub> and WSe<sub>2</sub> layers were sequentially transferred such that each flake is in contact with only one prepatterned Gr electrode, with a MoS<sub>2</sub>/WSe<sub>2</sub> overlap region in the middle of the device. All electrical measurements were performed at room temperature, in ambient air.

#### **RESULTS AND DISCUSSION**

We first examine the properties of Gr contacted MoS<sub>2</sub> back-gated FETs (Figure 2a). Figure 2b,c shows the  $I_{\rm D}$ - $V_{\rm G}$ and  $I_{\rm D} - V_{\rm D}$  characteristics of a representative MoS<sub>2</sub> transistor with Gr S/D contacts. Here the p<sup>+</sup>Si/SiO<sub>2</sub>

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(260 nm) substrate is used as the back gate. The channel length, L, and width, W, are  $\sim$ 7  $\mu$ m and  $\sim$ 25  $\mu$ m, respectively. This MoS<sub>2</sub> transistor with vdW Gr contacts exhibits clear n-type characteristic with ON/OFF current ratio of  $\sim 10^6$ . Notably, the low  $V_{\rm DS}$  regime of the output characteristics (Figure 2b) is linear without an inflection point. This result suggests that Gr provides efficient contacts to the conduction band of MoS<sub>2</sub> for electron injection. This observation is similar to those previously reported for MoS<sub>2</sub> devices with elemental metal contacts, where the FETs exhibited n-type characteristics. We have also characterized Gr contacted WSe<sub>2</sub> multilayer devices. In contrast to MoS<sub>2</sub> devices, Gr contacted WSe<sub>2</sub> FETs exhibit a p-type characteristic with nonlinear  $I_{\rm D} - V_{\rm D}$  curves arising from a large Schottky barrier (SB) height to the valence band of WSe<sub>2</sub> at the Gr interface (Supporting Information, Figure S1). The results suggest that the workfunction of Gr, which is  $\sim$ 4.5 eV based on literature,<sup>29</sup> is low enough for contacting electrons in MoS<sub>2</sub>, but not high enough to form an ohmic contact to holes in WSe<sub>2</sub>. Given the ability to chemically dope Gr,<sup>30</sup> in the future, it should be possible to explore Gr with tuned work function to further improve the contact resistances to both MoS<sub>2</sub> and WSe<sub>2</sub>. This presents potentially a unique feature of Gr contacts over elemental metals.

Next we fabricated an all-2D transistor, where a  $MoS_2$  flake (thickness, ~10 nm) is contacted by bilayer Gr S/D, with h-BN (thickness, ~55 nm) as the top-gate dielectric and multilayer Gr (thickness, ~10 nm) as the top-gate electrode (Figure 3a). In this system, all interfaces are based on vdW bonding, presenting a unique device architecture where crystalline, layered materials are stacked on demand, without the lattice parameter constraints. The device has a channel length and width of  $\sim$ 3 and 2.7  $\mu$ m, respectively. Panels b and c of Figure 3 depict the transfer and output characteristics of this all 2-D FET, respectively. The device demonstrates clear n-type switching behavior, with ON/OFF current ratio of >10<sup>6</sup> (the OFF current being limited by the noise level of the system).

The contact resistance of TMDC devices is generally significant as compared to the channel resistance. Thus, in order to properly extract the device mobility, the contact resistances must be carefully taken into



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Figure 3. All-2D MoS<sub>2</sub> FET with few-layer h-BN gate dielectric, and bilayer graphene source/drain and multilayer graphene top-gate electrodes. (a) Device schematic (not to scale). (b)  $I_D - V_G$  characteristics at different  $V_D$ . (c)  $I_D - V_D$  characteristics. (d) Extracted mobility as a function of gate voltage,  $V_G - V_t$ . The inset shows the circuit model of the device used for mobility extraction. The substrate is grounded during all measurements.

account. To extract the mobility of the all-2D FET, we used a model described as follows. The potential from the source to the drain is assumed to drop across three resistors in series, as shown in the inset of Figure 3d: the source and drain contacts,  $R_c$ , and the active channel,  $R_{CH}$ . The drain current,  $I_D$  can be expressed as  $I_D = \mu C_{ox}$  $(W/L)(V_{G-i} - V_t)(V_{D-i})$ , where  $\mu$  is the mobility,  $C_{ox}$  is the capacitance of the gate oxide, W and L are the channel width and length, respectively, V<sub>t</sub> is the threshold voltage, and  $V_{G-i}$  and  $V_{D-i}$  are the intrinsic gate and drain voltages after subtracting the potential drops across the source and drain contact resistances. The channel resistance  $R_{CH}$  can be then defined as  $R_{CH}$  =  $V_{\rm D-1}/I_{\rm D} = L/(\mu C_{\rm ox} W(V_{\rm G-1} - V_{\rm t}))$ . The total resistance between the source and the drain is given by  $R_{total} =$  $R_{CH} + 2R_c = V_D/I_D = L/(\mu C_{ox}W(V_{G-i} - V_t)) + 2R_c$ . At high  $V_{G-i} - V_{t'}$  the channel resistance becomes negligible with the total resistance being dominated by the contacts. That is  $R_{\rm total} \approx 2R_{\rm c}$ . From the measured transfer curves at high  $V_{\rm G}$  and  $V_{\rm D}$  = 0.05 V, we extract  $R_{\rm c} \sim 15 \ {\rm k}\Omega$  (see Supporting Information for details).  $I_{\rm D}$ can be expressed as  $\mu C_{ox}(W/L)(V_G - V_t - I_D R_c)(V_D - V_c)$  $2I_DR_c$ ). Assuming h-BN has a dielectric constant of 4,  $C_{ox}$ is calculated to be  ${\sim}6.4 \times 10^{-8}~\text{F/cm}^2.$  The extracted electron mobility for our all-2D device is subsequently calculated as a function of  $V_{\rm G} - V_{\rm t}$  as shown in Figure 3d. The peak mobility is  $\sim$ 33 cm<sup>2</sup>/V · s which is consistent with the range of electron mobility values reported in the literature for MoS<sub>2</sub> FETs.<sup>8,31</sup> We also calculate the field-effect mobility  $\mu_{FE}$  using the expression  $\mu_{FE}$  =  $dI_D/dV_G(L/WC_{ox}V_{DS})$ , at  $V_{DS} = 0.05$  V. In this method,

the contact resistance is not corrected for, and the mobility is extracted to be  $26 \text{ cm}^2/\text{V} \cdot \text{s}$ , which is slightly lower than the value obtained when the contact resistance is corrected for.

Notably, in distinct contrast to conventional Si MOSFETs, the mobility of the all-2D FET does not decrease at high gate fields, and remains rather constant (Figure 3d). This observation is highly desirable for FET operation since it reduces the  $V_{\rm G}$  dependence of the ON-state device performance (e.g., speed), thus making the eventual circuit design based on the demonstrated device architecture more robust. In conventional Si MOSFETs, the mobility drastically decays at high gate fields as the carriers are moved closer to the device surface, thereby making them more susceptible to surface roughness scattering.<sup>32</sup> In contrast, in the all-2D FET, the impact of surface roughness scattering of carriers is expected to be less severe given the vdW nature of the bonds with atomically uniform thicknesses of the semiconductor channel and the gate dielectric. In addition, given the 2D nature of the thin MoS<sub>2</sub> layers used, the charge centroid of carriers is expected to be near the middle of the MoS<sub>2</sub> thickness with minimal dependence on the gate fields. This was previously observed in ultrathin InAs and WSe<sub>2</sub> FETs.<sup>33,9</sup> These two effects contribute to the lack of gate dependence in mobility at high gate fields, and demonstrate an important advantage of the all-2D FET.

Finally, we demonstrate an all-2D diode using WSe<sub>2</sub> as the hole conducting layer, MoS<sub>2</sub> as the electron conducting layer, and Gr as the contacts (Figure 4a).

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Figure 4. All-2D diode consisting of few-layer  $MoS_2$  and  $WSe_2$  as electron and hole conducting layers, respectively, and monolayer graphene as the electrical contacts. (a) Cross-sectional schematic of the diode (not to scale). (b) Qualitative band diagrams of the diode at equilibrium (V = 0 V), forward bias, and reverse bias. (c) Diode I - V characteristics. The substrate was grounded during measurements.

As noted before, Gr forms a low resistance contact to the conduction band of MoS<sub>2</sub> for electron injection, but a Schottky contact to the WSe<sub>2</sub> valence band for hole injection. Thus, a Gr/WSe<sub>2</sub>/MoS<sub>2</sub>/Gr heterostructure is composed of a Schottky diode between Gr and WSe<sub>2</sub>, and a heterojunction diode between WSe<sub>2</sub> and MoS<sub>2</sub>. The band alignment for a WSe<sub>2</sub>/MoS<sub>2</sub> heterobilayer was previously explored, showing a  $\sim$ 100 meV offset in the conduction band edge of the two materials.<sup>15</sup> Assuming a similar band offset for the multilayer heterojunction explored here, a qualitative band diagram can be drawn as shown in Figure 4b. Under forward bias, electrons from MoS<sub>2</sub> can cross the low barrier into WSe<sub>2</sub> and recombine with the holes that are injected from Gr into  $WSe_2$ . I-V is determined by the MoS<sub>2</sub>/WSe<sub>2</sub> junction, and the parasitic resistances of the Schottky contacts and the MoS<sub>2</sub> and WSe<sub>2</sub> films. Under reverse bias, the applied voltage is dropped at the MoS<sub>2</sub>/WSe<sub>2</sub> junction and the current is limited by the thermally generated electrons and holes. The measured diode characteristic is shown in Figure 4c. The device exhibits clear rectification behavior, with the forward bias current at 3 V being  $\sim 10^5$  times larger than the reverse bias current. The diode ideality factor is extracted to be 1.4. The low reverse bias current and the ideality factor suggest high interface quality between MoS<sub>2</sub> and WSe<sub>2</sub> with minimal interface recombination/generation of carriers. This diode presents yet another example of configuring different layered material components into a functional device through the multistep transfer process.

#### CONCLUSIONS

In summary, we have demonstrated the operation of an all-2D transistor, using a TMDC channel material, h-BN gate dielectric, and graphene source/drain and gate contacts. This work presents a unique platform for utilizing heterostructures of user-defined layered materials with atomically uniform and digitally controlled thicknesses for functional devices. Importantly, the vdW bonding of the interfaces and the use of the multistep transfer process provide pathways for making complex devices based on crystalline layers without the constraints of lattice parameters. Future work involves thickness scaling of individual components down to a monolayer and channel length scaling down to the molecular-scale dimensions.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Characteristics of backgated WSe<sub>2</sub> p-FETs with graphene contacts; contact resistance calculations; Raman spectra of the all-2D FET; optical microscope image of the MoS<sub>2</sub>/WSe<sub>2</sub> diode. This material is available free of charge via the Internet at http://pubs.acs.org.

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#### **REFERENCES AND NOTES**

- 1. Schwierz, F. Graphene Transistors: Status, Prospects, and Problems. *Proc. IEEE* **2013**, *101*, 1567–1584.
- Avouris, P.; Chen, Z.; Perebeinos, V. Carbon-Based Electronics. Nat. Nanotechnol 2007, 2, 605–615.
- Geim, A. K. Graphene: Status and Prospects. Science 2009, 324, 1530–1534.





- Liu, H.; Ye, P. D. MoS2 Dual-Gate MOSFET With Atomic-Layer-Deposited Al<sub>2</sub>O<sub>3</sub> as Top-Gate Dielectric. *IEEE Electron Device Lett.* 2012, 33, 546–548.
- Wang, H.; Yu, L.; Lee, Y.-H.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L.-J.; Dubey, M.; Kong, J.; Palacios, T. Integrated Circuits Based on Bilayer MoS<sub>2</sub> Transistors. *Nano Lett.* **2012**, *12*, 4674– 4680.
- Liu, H.; Xu, K.; Zhang, X.; Ye, P. D. The Integration of High-k Dielectric on Two-Dimensional Crystals by Atomic Layer Deposition. *Appl. Phys. Lett.* **2012**, 100–104.
- Wei, L.; Jiahao, K.; Wei, C.; Sarkar, D.; Khatami, Y.; Jena, D.; Banerjee, K. High-Performance Few-Layer-MoS<sub>2</sub> Field-Effect-Transistor with Record Low Contact-Resistance. *IEEE Int. Electron Devices Meet.* **2013**, 19.4.1–19.4.4.
- Fang, H.; Tosun, M.; Seol, G.; Chang, T. C.; Takei, K.; Guo, J.; Javey, A. Degenerate n-Doping of Few-Layer Transition Metal Dichalcogenides by Potassium. *Nano Lett.* **2013**, *13*, 1991–1995.
- Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A. High-Performance Single Layered WSe<sub>2</sub> p-FETs with Chemically Doped Contacts. *Nano Lett.* **2012**, *12*, 3788–3792.
- 10. Radisavljevic, B.; Whitwick, M. B.; Kis, A. Integrated Circuits and Logic Operations Based on Single-Layer MoS<sub>2</sub>. ACS Nano **2011**, *5*, 9934–9938.
- Chuang, S.; Battaglia, C.; Azcatl, A.; McDonnell, S.; Kang, J. S.; Yin, X.; Tosun, M.; Kapadia, R.; Fang, H.; Wallace, R. M.; Javey, A. MoS<sub>2</sub> P-type Transistors and Diodes Enabled by High Work Function MoOx Contacts. *Nano Lett.* **2014**, *14*, 1337–1342.
- Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS<sub>2</sub> Transistors with Scandium Contacts. *Nano Lett.* **2013**, *13*, 100–105.
- 13. Jena, D. Tunneling Transistors Based on Graphene and 2-D Crystals. *Proc. IEEE* **2013**, *101*, 1585–1602.
- Cheng, R.; Li, D.; Zhou, H.; Wang, C.; Yin, A.; Jiang, S.; Liu, Y.; Chen, Y.; Huang, Y.; Duan, X. Electroluminescence and Photocurrent Generation from Atomically Sharp WSe<sub>2</sub>/MoS<sub>2</sub> Heterojunction p-n Diodes. **2014**, No. arXiv:1403.3447.
- Fang, H.; Battaglia, C.; Carraro, C.; Nemsak, S.; Ozdol, B.; Kang, J. S.; Bechtel, H. A.; Desai, S. B.; Kronast, F.; Unal, A. A.; *et al.* Strong Interlayer Coupling in van der Waals Heterostructures Built from Single-Layer Chalcogenides. *Proc. Natl. Acad. Sci. U.S. A.* **2014**, *111*, 6198–6202.
- Baugher, B. W. H.; Chuchill, H. O. H.; Yang, Y.; Jarillo-Herrero, P. Optoelectronic Devices Based on Electrically Tunable p-n Diodes in a Monolayer Dichalcogenide. *Nat. Nanotechnol.* 2014, *9*, 262–267.
- Yoon, J.; Park, W.; Bae, G.-Y.; Kim, Y.; Jang, H. S.; Hyun, Y.; Lim, S. K.; Kahng, Y. H.; Hong, W.-K.; Lee, B. H.; Ko, H. C. Highly Flexible and Transparent Multilayer MoS<sub>2</sub> Transistors with Graphene Electrodes. *Small* **2013**, *9*, 3295–3300.
- Lee, G.-H.; Yu, Y.-J.; Cui, X.; Petrone, N.; Lee, C.-H.; Choi, M. S.; Lee, D.-Y.; Lee, C.; Yoo, W. J.; Watanabe, K.; Taniguchi, T.; *et al.* Flexible and Transparent MoS<sub>2</sub> Field-Effect Transistors on Hexagonal Boron Nitride-Graphene Heterostructures. *ACS Nano* **2013**, *7*, 7931–7936.
- Bertolazzi, S.; Krasnozhon, D.; Kis, A. Nonvolatile Memory Cells Based on MoS2/Graphene Heterostructures. ACS Nano 2013, 7, 3246–3252.
- Britnell, L.; Gorbachev, R. V.; Jalil, R.; Belle, B. D.; Schedin, F.; Mishchenko, A.; Georgiou, T.; Katsnelson, M. I.; Eaves, L.; Morozov, S. V.; *et al.* Field-Effect Tunneling Transistor Based on Vertical Graphene Heterostructures. *Science* 2012, 335, 947–950.
- Britnell, L.; Gorbachev, R. V.; Geim, A. K.; Ponomarenko, L. A.; Mishchenko, A.; Greenaway, M. T.; Fromhold, T. M.; Novoselov, K. S.; Eaves, L. Resonant Tunnelling and Negative Differential Conductance in Graphene Transistors. *Nat. Commun.* 2013, 4, No. 1794.
- Georgiou, T.; Jalil, R.; Belle, B. D.; Britnell, L.; Gorbachev, R. V.; Morozov, S. V.; Kim, Y.-J.; Gholinia, A.; Haigh, S. J.; Makarovsky, O.; et al. Vertical Field-Effect Transistor Based on graphene-WS<sub>2</sub> Heterostructures for Flexible and Transparent Electronics. *Nat. Nanotechnol* **2013**, *8*, 100–103.

- Chuang, S.; Kapadia, R.; Fang, H.; Chang, T. C.; Yen, W.-C.; Chueh, Y.-L.; Javey, A. Near-ideal Electrical Properties of InAs/WSe<sub>2</sub> van der Waals Heterojunction Diodes. *Appl. Phys. Lett.* **2013**, 102–105.
- Rance, G. A.; Marsh, D. H.; Bourne, S. J.; Reade, T. J.; Khlobystov, A. N. van der Waals Interactions between Nanotubes and Nanoparticles for Controlled Assembly of Composite Nanostructures. ACS Nano 2010, 4, 4920– 4928.
- Ponomarenko, L. A.; Geim, A. K.; Zhukov, A. A.; Jalil, R.; Morozov, S. V.; Novoselov, K. S.; Grigorieva, I. V.; Hill, E. H.; Cheianov, V. V.; Fal'ko, V. I.; *et al.* Tunable Metal-Insulator Transition in Double-Layer Graphene Heterostructures. *Nat. Phys.* **2011**, *7*, 958–961.
- Dean, C. R.; Young, A. F.; Meric, I.; Lee, C.; Wang, L.; Sorgenfrei, S.; Watanabe, K.; Taniguchi, T.; Kim, P.; Shepard, K. L.; *et al.* Boron Nitride Substrates for High-Quality Graphene Electronics. *Nat. Nanotechnol.* **2010**, *5*, 722–726.
- Chan, J.; Venugopal, A.; Pirkle, A.; McDonnell, S.; Hinojos, D.; Magnuson, C. W.; Ruoff, R. S.; Colombo, L.; Wallace, R. M.; Vogel, E. M. Reducing Extrinsic Performance-Limiting Factors in Graphene Grown by Chemical Vapor Deposition. ACS Nano 2012, 6, 3224–3229.
- Suk, J. W.; Kitt, A.; Magnuson, C. W.; Hao, Y.; Ahmed, S.; An, J.; Swan, A. K.; Goldberg, B. B.; Ruoff, R. S. Transfer of CVD-Grown Monolayer Graphene onto Arbitrary Substrates. ACS Nano 2011, 5, 6916–6924.
- Khomyakov, P. A.; Giovannetti, G.; Rusu, P. C.; Brocks, G.; van den Brink, J.; Kelly, P. J. First-Principles Study of the Interaction and Charge Transfer between Graphene and Metals. *Phys. Rev. B* **2009**, *79*, 195425.
- 30. Liu, H.; Liu, Y.; Zhu, D. Chemical Doping of Graphene. *J. Mater. Chem.* **2011**, *21*, 3335–3345.
- Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS<sub>2</sub> Transistors. *Nat. Nanotechnol.* 2011, 6, 147–150.
- Jin, S.; Fischetti, M. V.; Tang, T.-W. Modeling of Surface-Roughness Scattering in Ultrathin-Body SOI MOSFETs. *IEEE Trans. Electron Devices* 2007, 54, 2191–2203.
- Takei, K.; Kapadia, R.; Fang, H.; Plis, E.; Krishna, S.; Javey, A. High Quality Interfaces of InAs-on-Insulator Field-Effect Transistors with ZrO<sub>2</sub> Gate Dielectrics. *Appl. Phys. Lett.* 2013, 102–105.

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# Field-Effect Transistors Built from All Two-Dimensional Material Components

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### **Supporting Information**

#### WSe<sub>2</sub> Schottky-barrier FETs with monolayer graphene contacts

Figure S1 shows the  $I_D$ - $V_{DS}$ , and  $I_D$ - $V_{GS}$  characteristics of a back-gated FET with WSe<sub>2</sub> channel and monolayer graphene contacts. The WSe<sub>2</sub> flake is ~5 nm thick. The length and width of the device are 7 µm and 18 µm, respectively. Graphene forms a Schottky contact with the valence band of WSe<sub>2</sub>, allowing for injection of holes but with a high contact resistance. Here, the p+ Si substrate is used as the back-gate with 260 nm thick SiO<sub>2</sub> as the gate dielectric.



**Figure S1.** Back-gated WSe<sub>2</sub> FET with graphene contacts. (a) Schematic of WSe<sub>2</sub> p-FET with graphene contacts. (b)  $I_D$ - $V_D$  characteristics. (c)  $I_D$ - $V_G$  characteristics.

Figure S2 shows the total resistance,  $R_{tot}$ , vs.  $V_{GS}$  curve, extracted from the *I-V* curves of the all-2D n-FET of Figure 3.  $R_{tot}$  is obtained from  $V_D/I_D$  at  $V_D = 0.08$  V. Since only a limited number of data points were available for gate voltage,  $V_{GS}$ , the  $R_{tot}$  vs.  $V_{GS}$  curve is extrapolated using the polynomial  $b1+b2/x+b3/x^2$ , where the fitting parameters are extracted as:

$$b1 = 29898 = 2R_c$$
  
 $b2 = 4.15895 \times 10^5$   
 $b3 = -4.90489 \times 10^5$ 

As  $V_{GS}$  approaches  $\infty$ ,  $R_{total}$  approached  $2R_c$ , since the channel resistance decreases substantially.  $R_c$  is thus extracted to be ~15 k $\Omega$ .



Figure S2:  $R_{tot}$  vs.  $V_{GS}$  for the all-2D FET of Figure 3 used to extract  $R_c$ .

Raman spectroscopy of layered components in all-2D FET of Fig.1



**Figure S3.** (a) Optical image of the all-2D FET of Fig. 1 of main text, showing the points where Raman scan was performed. (b) Raman spectrum at point (i), as marked in panel (a), where MoS<sub>2</sub>, h-BN and exfoliated graphene are present. (c) Raman spectrum at point (ii), where only h-BN is present. (d) Raman spectrum at point (iii), showing the presence of bilayer graphene. (e) Raman spectrum at point (iv), showing the presence of bilayer graphene.

Optical microscope image of MoS<sub>2</sub>/WSe<sub>2</sub> heterojunction diode with monolayer graphene

contacts of device shown in Fig. 4



Figure S4: Optical microscope image of an all-2D  $MoS_2/WSe_2$  heterojunction diode with monolayer graphene contacts. Scale bar is 7  $\mu$ m.