Parallel Array InAs Nanowire Transistors for Mechanically Bendable, Ultrahigh Frequency Electronics

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ABSTRACT The radio frequency response of InAs nanowire array transistors on mechanically flexible substrates is characterized. For the first time, GHz device operation of nanowire arrays is demonstrated, despite the relatively long channel lengths of ~1.5 μm used in this work. Specifically, the transistors exhibit an impressive maximum frequency of oscillation, f_{max} ~ 1.8 GHz, and a cutoff frequency, f_t ~ 1 GHz. The high-frequency response of the devices is due to the high saturation velocity of electrons in high-mobility InAs nanowires. The work presents a new platform for flexible, ultrahigh frequency devices with potential applications in high-performance digital and analog circuitry.

KEYWORDS: nanowires · flexible electronics · printed · plastic · radio frequency devices

Over the past several years, semiconductor nanowires (NWs) have been extensively explored for electronic and sensor applications[1−8] owing to their unique physical properties with tunable and well-defined atomic composition.[9] In one specific platform, a contact printing technique is utilized for the large-scale assembly of NW parallel arrays on a support substrate, followed by the subsequent device fabrication.[10−13] Since NW arrays are utilized, the stochastic device-to-device variation is drastically reduced, which is of practical importance.[14−16] The performance limits of the enabled devices, however, are still unknown. In this regard, here we characterize the radio frequency (RF) response of InAs NW array transistors on bendable substrates, elucidating an important performance metric for determining their potential application domain. Notably, for the first time, the GHz operation of mechanically flexible, NW parallel array devices is demonstrated. The results demonstrate the potential of NW array devices for ultrahigh frequency (UHF) electronic circuits.

UHF electronics operating in the 0.3−3 GHz regime are highly attractive for various analog and digital circuits.[17,18] The ability to fabricate these devices on mechanically bendable substrates that conform nonplanar surfaces and potentially by printing techniques may further broaden their utility and application domain. In this work, highly aligned InAs NW arrays were utilized as the active channel material of the flexible, UHF field-effect transistors (FETs). InAs NWs are attractive for such applications due to their high electron mobility,[2,4,19] high electron saturation velocity, ease of ohmic metal contact formation,[4,20] and miniaturized diameters that make them mechanically flexible.

InAs NWs used in this study were synthesized on Si/SiO_2 substrates by a physical vapor transport method.[4] The grown NWs had an average diameter and length of ~30 nm and ~10 μm. Subsequently, NW contact printing[10,11,15] was carried out by directionally sliding a growth substrate, consisting of randomly grown InAs NWs, on top of a polyimide (PI) layer (24 μm) spin-coated on a Si/SiO_2 handling wafer. During this process, NWs are directly transferred from the growth substrate to the PI surface as parallel arrays.[10,11,15] To achieve patterned assembly of NWs, the PI surface is first coated with a lithographically patterned resist layer, followed by NW printing and lift-off in a solvent. Nickel (~50 nm) source (S) and drain (D) electrodes were then formed, followed by atomic layer deposition of Al_2O_3 (~8 nm) at 150 °C as the gate dielectric. Finally, Al (40 nm) top-gate (G) electrodes were fabricated. All electrodes were defined by photolithography and lift-off processes. There is ~200 nm of misalignment due to the limitation of contact aligner,

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Received for review July 29, 2010 and accepted September 08, 2010.

Published online September 16, Published online Xxxxxxxxx 00, 0000
10.1021/nn1018329

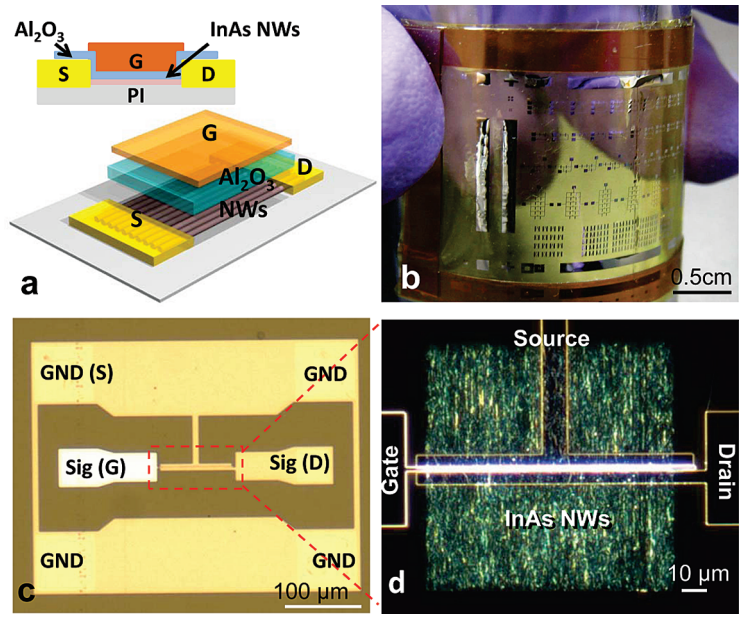

Figure 1. Schematic and optical images of a printed InAs NW array FET fabricated on a flexible PI substrate for GHz operation. (a) Schematic illustration of the NW parallel array FET, illustrating the various layers of the device. The cross-sectional image is shown in the top. (b) Photograph image of the fabricated NW device array on a bendable PI substrate. (c) Bright-field optical image of a NW array FET with ground−signal−ground configuration for the RF measurements. (d) Dark-field optical image, showing the printed InAs NW region.

resulting in the overlap of G with one of the S/D electrodes and underlap with the other, resulting in a parasitic capacitance and series resistance, respectively. The channel length (S/D electrode spacing) is $L \sim 1.5$ μm, and the channel width is $W = 100-200$ μm. The gate electrode length is $L_G \sim 1.4$ μm. The configuration of the electrical pads matches that of the conventional ground−signal−ground (GSG) microwave probes (150 μm pitch). Figure 1a shows the layered schematic of a NW array RF device. The optical microscopy images of a completed device are shown in Figure 1c,d, clearly depicting the active NW array region and the GSG electrode configuration. The printed NW density is ~4 NWs/μm as confirmed by scanning electron microscopy. After the completion of the fabrication process, the PI layer is peeled off from the rigid Si/SiO_2 handling wafer, resulting in mechanically flexible device arrays, as shown in Figure 1b.

Figure 2a shows representative output characteristics of an InAs NW array FET with $W = 100$ μm on a flexible PI substrate. The FET delivers a unit-width normalized ON current of $I_{ON} \sim 23$ μA/μm at $V_{DS} = 2$ V. Individual NWs with comparable lengths and diameters deliver ~10 μA of ON current based on our previous studies.[4] From the current density, we estimate that ~2 NW/μm cross the S/D electrodes, with the rest of the NWs only contacting one electrode and thereby serving as parasitic elements (*i.e.*, they contribute to the gate capacitance but not the transconductance). A respectable ON/OFF current ratio, $I_{ON}/I_{OFF} \sim 100$ is observed at $V_{DS} = 2.5$ V, as shown in the inset of Figure 2b. From the $I_{DS}-V_{GS}$ curve at $V_{DS} = 2.5$ V, the peak transconductance, $g_m = (dI_{DS}/dV_{GS})|_{V_{DS}} \sim 1.1$ mS (*i.e.*, ~11 μS/μm as normalized by W) is measured at $V_{GS} = -0.5$ V (Figure 2b). From the slope of $I_{DS}-V_{DS}$ curve at $V_{DS} = 2.5$ V and $V_{GS} = -0.4$ V, the output resistance, $r_o \sim 8$ kΩ is obtained, which corresponds to a gain of $A_v = r_o g_m \sim 8$. A_v is the intrinsic gain of a transistor with no loading (*i.e.*, transistor is self-loaded), which is an important figure for operation amplifiers, instrumentation amplifiers, and other circuit components where large gains are desirable. Furthermore, the mechanical flex-

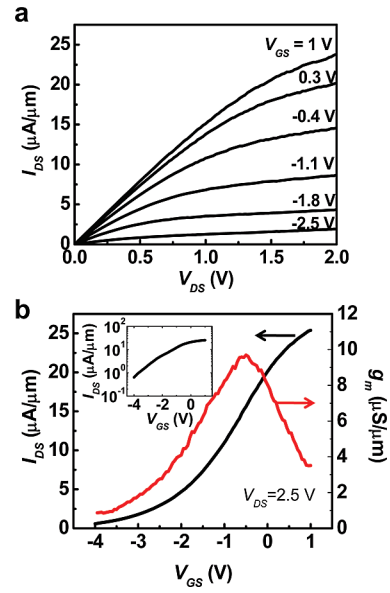

Figure 2. DC characteristics of an InAs NW array FET. (a) Normalized output characteristics of a NW array FET with a channel width, $W \sim 100$ μm, and gate length, $L_G \sim 1.5$ μm. (b) Linear-scale transfer characteristic and the corresponding transconductance as a function of gate bias at $V_{DS} = 2.5$ V. The log-scale $I_{DS}-V_{GS}$ at $V_{DS} = 2.5$ V is shown in the inset.

ibility of the devices was tested by measuring the electrical properties as a function of the radius of curvature. The NW array FETs do not exhibit a significant electrical degradation, even when bent to a radius of ~18 mm with compressive/tensile stress (see Supporting Information, Figure S1), which is attributed to the miniaturized dimensions of NWs. Additionally, since InAs NWs have significantly higher Young's modulus than the supporting PI substrate, the strain is mostly compensated by the substrate, with the strain in the NW being only $\varepsilon_{xx} \sim 0.5\%$, as predicted from mechanical simulations (Figure S1b).

To directly extract the high-frequency behavior, the two-port scattering parameters (*S* parameters) of InAs NW array FETs were measured in the common-source configuration using standard procedures with a vector network analyzer (VNA) over a frequency range from 40 MHz to 10 GHz (Anritsu 37397C). Calibration of the probe tips was performed by employing the short-open-load-thru method (see Supporting Information) on an impedance standard substrate provided by Cascade Microtech (ISS 101-190). On-wafer pad-open and pad-short structures (Figure S2) were used to de-embed the parasitic effects of the contact pads, that is, shunt capacitance/conductance and series inductance/resistance (see Supporting Information for the details). This de-embedding does not correct for the overlap capacitances between the gate and source/drain electrodes. The *S* parameters were then used to analyze the RF performance of the device (Figure 3a). S_{11}, S_{22}, S_{21}, and S_{12} are, respectively, the reflection coefficient of the input, the reflection coefficient of the output, the forward transmission gain, and the reverse transmission gain. Figure 3b shows various RF metrics of a representative device with $W = 200$ μm, all derived from *S* parameters. Specifically, unity transit frequency of the current gain (h_{21}) of a transistor is called f_t and is an important factor for determining the high-frequency limit of the transistor for various analog/RF and digital applications. To obtain f_t from the measurements, *S* parameters are first converted to hybrid parameters (*h* parameters) as described in the Supporting Information. The parameter h_{21} is plotted as a function of frequency (Figure 3b), and f_t occurs at the frequency where h_{21} equals 1, that is, 0 dB. As depicted in Figure 3b, InAs NW array FETs exhibit an impressive $f_t = 1.08$ GHz. Maximum stable gain (MSG), the gain a transistor can provide if suitable input and output matching networks are incorporated for an unconditionally stable amplifier design, is also extracted (see Supporting Information) and plotted as a function of frequency (Figure 3b). At 1 GHz, the MSG of the FET is ~6 dB, which confirms that designing an RF amplifier at the GHz regime is plausible. Finally, maximum unilateral gain (*U*, Mason gain) is extracted (Supporting Information) as a function of frequency (Figure 3b). Mason gain is the maximum unilateral power gain the device can provide at a specific frequency of operation. The maximum frequency of oscillation, f_{max}, is determined by extracting Mason's gain at 0 dB. It is an important figure of merit, and at frequencies beyond f_{max}, a transistor cannot provide any power gain and turns into a passive component. As shown in Figure 3b, the NW array FET has $f_{max} = 1.8$ GHz.

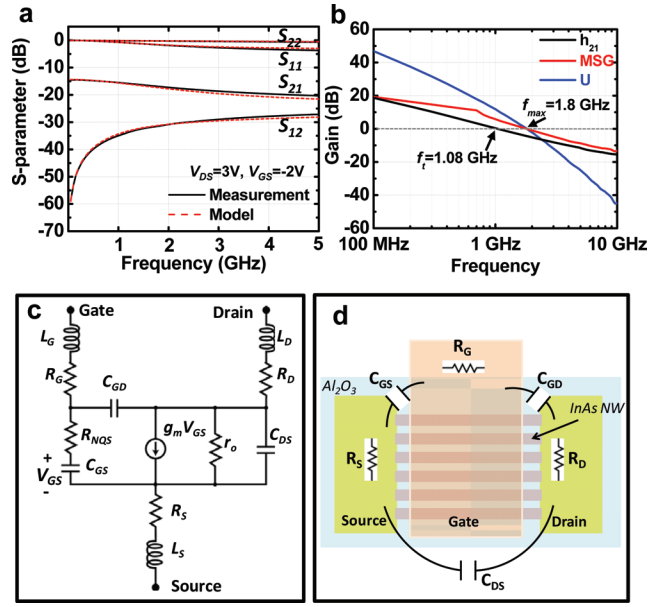

Figure 3. RF characterization of an InAs NW array FET. (a) Measured (black solid line) and modeled (red dashed line) scattering parameters, S_{11}, S_{12}, S_{21}, and S_{22} of an InAs NW array FET with $W \sim 200$ μm after de-embedding for frequencies between 40 MHz and 5 GHz. (b) Current gain (h_{21}), maximum stable gain (MSG), and unilateral power gain (*U*) extracted from measured *S* parameters as a function of frequency. The unity current gain frequency, f_t, and unity power gain frequency, f_{max}, are ~1.08 and 1.8 GHz, respectively. (c) Small signal equivalent circuit model and (d) device schematic, illustrating the various circuit components. R_S, R_D, and R_G are composed of metal sheet resistance and contact resistance.

A small signal model can also be fitted to the *S* parameter data to be used in the future circuit design and optimizations and further extract key device parameters. The small signal equivalent circuit is shown in Figure 3c,d. At the core is the hybrid-π model of the transistor including g_m, r_o, and the capacitances (C_{GS}, C_{GD}, and C_{DS}). Non-quasi-static (NQS) resistance, R_{NQS}, and the series resistance (R_G, R_S, R_D) and inductance (l_G, l_S, l_D) associated with the gate, source, and drain interconnects are added, resulting in the match between measured data and the fitted small signal model data (Figure 3a; see Supporting Information for details). The extracted component values for the small signal model are listed in Table 1.

To further characterize the devices, *S* parameters were measured at different drain and gate voltages with the extracted f_t shown in Figure 4a. As expected, f_t monotonically increases with V_{DS} for the explored bias range due to an increase in g_m. The peak f_t is obtained at $V_{GS} = -2$ V, most likely corresponding to when the Fermi level coincides with the first conduction sub-band edge of the InAs NW channel. Due to the

TABLE 1. Extracted and Fitted Parameters from Small Signal RF Modeling for a NW Array FET with W = 200 μm and L = 1.5 μm

g_m	r_o	C_{GS}	C_{GD}	C_{DS}	R_G	R_S	R_D	R_{NQS}	l_G	l_S	l_D
2.3 mS	13 kΩ	315 fF	35 fF	10 fF	102 Ω	66 Ω	73 Ω	85 Ω	200 pH	92 pH	148 pH

nonparabolicity of the band structure, effective mass increases as the Fermi level goes deeper into the conduction band, thereby lowering the electron mobility and saturation velocity. Since cutoff frequency is proportional to saturation velocity, it follows that as higher positive gate voltages, f_t decreases. Similarly, g_m can be extracted as a function of bias from the RF measurements (Figure 4b). A peak transconductance of $g_m \sim 12$ μS/μm at $V_{DS} = 3$ V and $V_{GS} = -2$ V is obtained from the AC small signal RF characteristics, which is consistent with the value obtained from the DC measurements (Figure 2b). Note that the devices in Figures 2 and 4 are not the same. Due to the device-to-device variations, the threshold voltage is slightly different.

Next, we examine the theoretical performance limit of InAs NW array FETs. The cutoff frequency is projected from the relation, $f_t = g_m/(2\pi(C_{GS} + C_{GD}))$. In the high field operation regime (*e.g.*, high V_{DS} and/or short L_G, as is the case in this work), the carriers propagate at the saturation velocity, v_{sat}, with the transconductance given as $g_m = v_{sat}(C_{ox}/L_G)$. Here C_{ox} is the gate oxide capacitance and can be obtained from $C_{ox} = C_{ox,1} \times (Wd)$, where $C_{ox,1}$ is the NW gate capacitance for a single NW and d is the NW density. The cutoff frequency is then $f_t = v_{sat}C_{ox}/(2\pi L_G(C_{GS} + C_{GD}))$. Note that the total gate source capacitance is given as $C_{GS} = C_{p,GS} + 2/3C_{ox}$, where $C_{p,GS}$ is the parasitic capacitance between G/S electrodes. The exact velocity-field curve for InAs NWs is unknown, so we use the bulk curve for the purpose of this analysis. The cutoff frequency is then calculated by using the extracted capacitances for the explored device geometry (Table 1) and $v_{sat} \sim 1.3 \times 10^7$ cm/s at a field of 16 kV/cm (corresponding to $V_{DS} = 2.5$ V and $L_G = 1.5$ μm).[21] From this analysis, $f_t \sim 7$ GHz is projected for $d = 2$ NWs/μm (Figure S4, Supporting Information) and $L_g = 1.5$ μm, which is ~7 times higher than the experimental f_t for the same NW density. This may be attributed to the dominant rote of surface scattering in the electron transport properties of unoptimized InAs NWs used in this work. In the future, exploration of surface passivation layers may help to further enhance the measured frequency response of NW RF-FETs. Additionally, by increasing the printed NW density to 20 NWs/μm (50 nm pitch), the theoretical f_t increases to ~13 GHz. Finally, in the absence of all parasitic elements, an ultimate theoretical f_t of ~14 GHz is projected, presenting the "intrinsic" cutoff frequency of the InAs transistors at the explored length scales. Further gate length miniaturization can also enhance the RF performance.

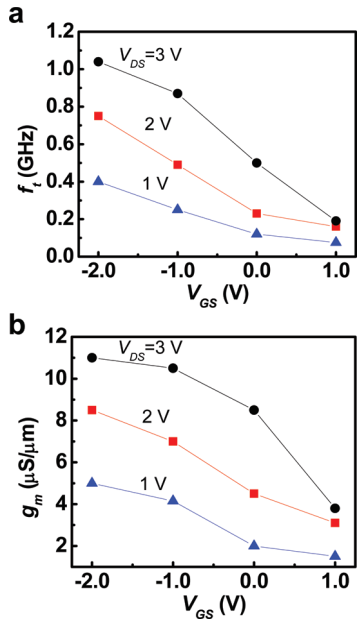

Figure 4. Bias dependence of the RF response. (a,b) Measured unity current gain frequency and transconductance as a function of V_{GS} and V_{DS} for a NW array FET with W = 200 μm.

The GHz operation of our FETs compares favorably with the other previously explored flexible device concepts. For example, hydrogen-terminated amorphous silicon or silicon films with various degrees of crystallinity have been widely utilized for applications in large-scale electronics with the highest reported f_t of ~250 MHz on plastic substrates.[22] Organic transistors have been limited to f_t of ~10 MHz[23] due to their low carrier mobilities. Several groups have achieved GHz operation using carbon nanotube arrays on either a plastic or rigid substrate[17,24−27] and graphene on a rigid substrate.[28] However, these devices exhibit poor I_{ON}/I_{OFF} due to the mixture of metallic nanotubes in the arrays and the small band gap of graphene. Previous work utilizing NWs for flexible electronics resulted in devices operating at 10−100 MHz,[29−31] although higher frequencies have been reported for single NWs with short channels on rigid Si substrates.[32] Egard *et al.*[33] recently reported GHz devices with $f_t > 7$ GHz and $f_{max} > 20$ GHz based on vertical InAs NW arrays grown epitaxially on InP wafers with a gate length of ~100 nm. This works shows the potential of InAs NWs for high-frequency transistors; however, the explored structure and geometry are not compatible with flexible electronics. Recently, promising flexible devices[34] are reported using inorganic single-crystalline flakes such as Si ($f_t \sim 0.5-3$ GHz for $L_G \sim 2$ μm)[35,36] and GaAs ($f_t \sim 1.5$ GHz for $L_G \sim 2$ μm).[37] These devices are fabricated *via* top-down etching and subsequent transfer method. The RF NW

device concept presented here has the advantage of potentially utilizing an all-printed fabrication scheme, without the need for complex lithographic processes.

The presented results show the potential of NW array FETs for future microwave applications on nonconventional substrates as enabled by (i) the uniform and dense assembly of NW parallel arrays, (ii) the inherently high saturation velocity of InAs, and (iii) the appropriate device design. This technology is of particular interest given the recent rapid growth of signal communication over the UHF bands. Notably, the explored device dimensions are within the resolution limit of advanced printing processes,[38] thereby making the presented platform potentially compatible with continuous roll-to-roll fabrication processes. In the future, further miniaturization of the device dimensions, improved printed NW array densities, and the use of surface passivation layers through process optimization are projected to enhance the cutoff frequency of the devices by an additional ~10-fold. This projected performance cap is comparable to that of the state-of-the-art nanoscale Si devices but uniquely is attainable on nonrigid substrates and with all-printed fabrication processes.

Acknowledgment. This work was partially funded by MARCO/MSD Focus Center Research Program, Berkeley Sensors and Actuator Center, and NSF CAREER Award. The synthesis part of this work was supported by a LDRD from Lawrence Berkeley National Laboratory. A.J. acknowledges a support from the World Class University program at Sunchon National University. We acknowledge Paul Leu for help with the mechanical simulations.

Supporting Information Available: Mechanical bendability of NW array FETs; details of de-embedding pad parasitic; extraction of h_{21}, MSG, and U from the S parameters; hybrid-π model; the effect of NW density on extrinsic cutoff frequency. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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Supporting Information

Mechanical bending of parallel array InAs NW FETs

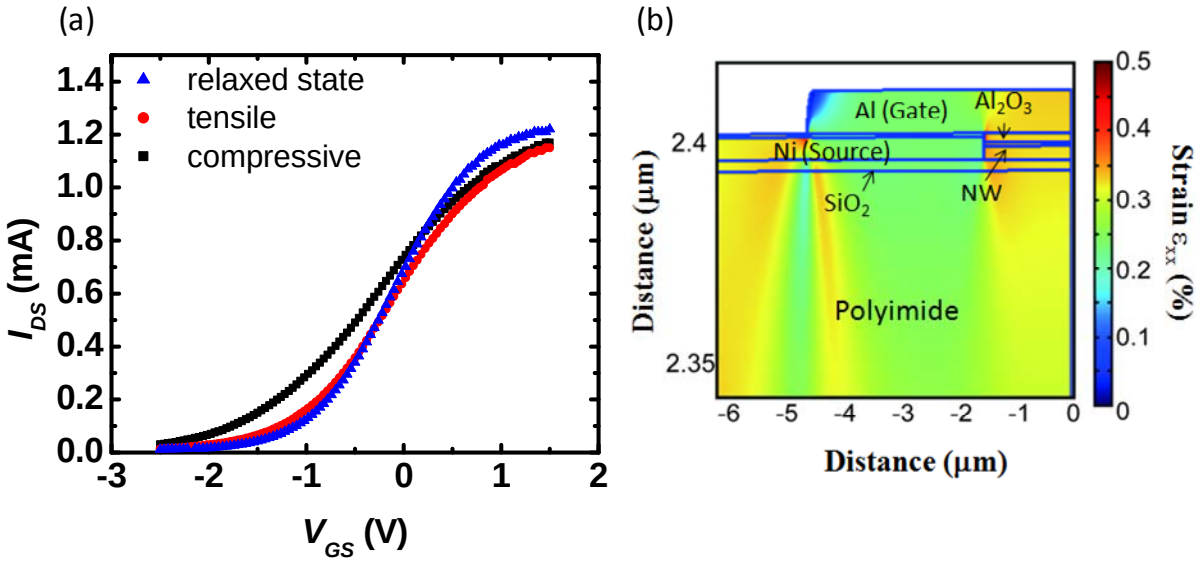

Figure S1: Mechanical bendability of NW-array FETs, Transfer characteristics of an InAs NW-array FET with W = 200 μm measured at V_{DS} = 1V as a function of the imposed bending condition. The device is first measured at the relaxed state, (bending radius, r = infinity), and under a tensile and compressive strain (r = 18 mm) conditions. **b**, Mechanical simulation of the strain for a NW device when bent to 18 mm curvature radius. Only half of the device is shown, depicting the various layers and their strain.

Short-open-load-thru (SOLT) calibration method

Electrical cables and probes are used to connect a vector network analyzer (VNA) ports to on-chip pads in order to measure a DUT (device under test). The raw data measured by the VNA is not accurate and contains the added parasitic effects of the cables/connectors and probes at the input and output. To de-embed the effect of these interconnections and calibrate the setup down to probe-tips, firstly a known set of terminations are measured (standard impedance substrate). By measuring these terminations in different configurations, the added parasitic effects of the cable/connectors and probes are obtained and subtracted from the raw measured data and hence the calibrated data, which is only due to the DUT and not the interconnections, is extracted.

On-wafer pad-open and pad-short for de-embedding pad parasitics

Calibration of the setup through the SOLT procedure (explained above) removes all the off-chip interconnection effects and yields to the measured data of the on-chip structures, which includes input/output pads and the transistor. Since we are only interested in the inherent characteristic of the transistor, the effects of the input/output pads should be removed. One approach is to repeat the SOLT procedure with pad-open, pad-short, pad-loaded, pads-thru structures and de-embed the added parasitic effects of the pads. Since fabricating an accurate and broadband on-chip 50-ohm termination and transmission lines are challenging, and furthermore, since the total structure is small relative to the wavelength of interest, we use a lumped element pad-open and pad-short configurations to de-embed the pad effects (Fig. S2). Pad-open gives the shunt capacitance and its associated conductance of the pad structure, and pad-short gives the series inductance and resistance of the pad/interconnect. Pad-only structures in open and short configurations were placed on the same die. These parasitic effects were then subtracted from the

total pad and transistor structure, and the S-parameters of the intrinsic transistor were obtained. In Figure S3, the measured current gain (h_{21}), the maximum stable gain (MSG), and maximum unilateral gain (U) before and after de-embedding are shown.

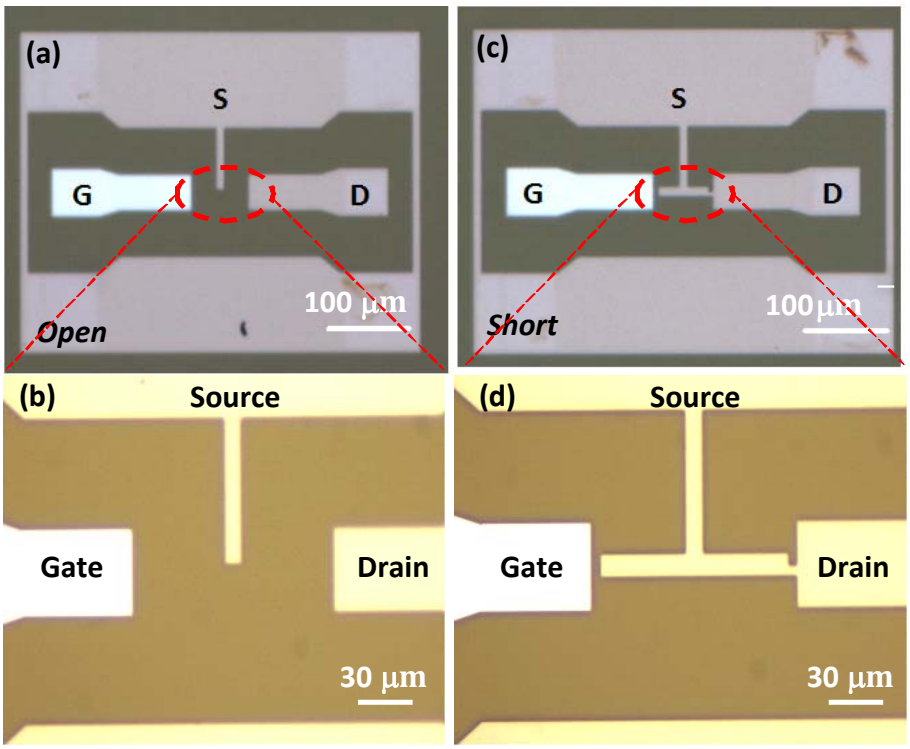

Figure S2: (a), (b) Pad-open and (c), (d) pad-short device configurations for de-embedding the pad effects.

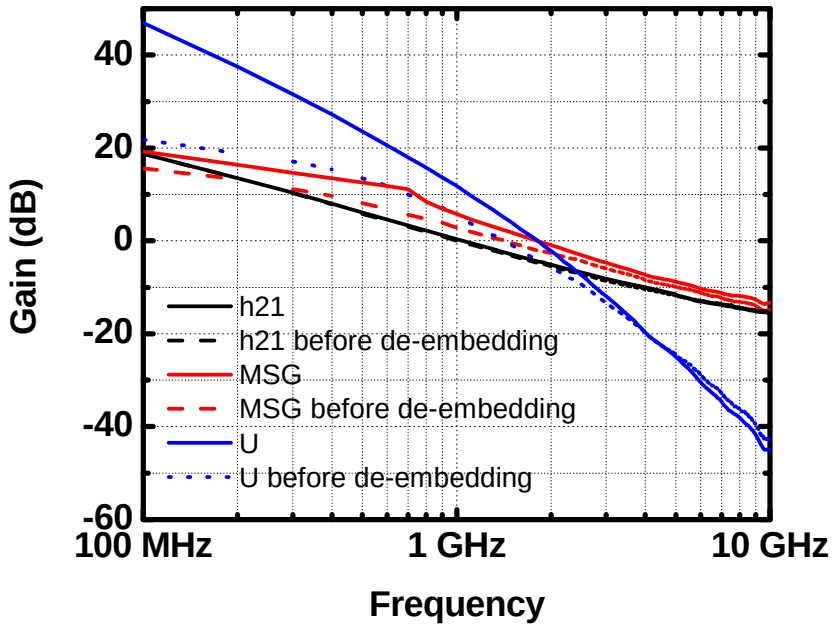

Figure S3: The effect of de-embedding on the measured current gain (h_{21}), Maximum stable gain (MSG), and maximum unilateral gain (U).

Extraction of h_{21}, MSG and U from the S-parameters

S-parameters can be converted to h-parameters and hence h_{21} can be plotted, so f_t (which is the frequency where h_{21}=1=0 dB) can be directly extracted. Maximum stable gain (MSG) is the theoretical gain a transistor can provide if suitable lossless input and output matching networks are incorporated, and is extracted as following:

$$MSG = \left(K - \sqrt{K^2 - 1}\right)\frac{|S_{21}|}{|S_{12}|}$$ for K > 1 (after 700 MHz)

$$MSG = \frac{|S_{21}|}{|S_{12}|}$$ for K < 1 (before 700 MHz)

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|}, \Delta = S_{11}S_{22} - S_{12}S_{21}$$

Maximum unilateral gain (U, Mason gain) is the maximum unilateral power gain the device can provide and is calculated from Y or Z (admittance or impedance) parameters as following

$$U = \frac{|Y_{21} - Y_{12}|^2}{4 \times (Re[Y_{11}] \times Re[Y_{22}] - Re[Y_{12}] \times Re[Y_{21}])}$$

The maximum power gain of a device is defined as the power gain delivered by a device when both input and output ports are matched to the impedance of the source and load, respectively. For a MOS device *MSG* is approximately given as: $MSG \approx \frac{f_t}{8\pi R_G C_{GD} f^2}$ for K > 1. As can be seen from this equation, *MSG* vs frequency, *f*, has a relation of *MSG* ~ $1/f^2$, or *MSG* drops by 20 dB/decade as frequency increases. In this equation, the frequency effects up to the second order are considered and higher order effects are neglected.

Hybrid-π model

Transistors are nonlinear devices (nonlinear output (i_d)/input (v_g) characteristics). To design an amplifier, suitable gate and drain voltages with respect to the source should be applied to the transistor to bias it at a desired operating point. After biasing, we assume the input voltage applied to the gate is small and hence the device can be assumed linear with respect to that. Hence we can derive a small signal linear model of the transistor at that certain bias point and use that for amplifier design. This model is called the hybrid- π model of the transistor. At the core there is a voltage controlled current source, which transforms the input voltage to the output current (i_2=-g_m.v_1), g_m being the transconductance of the device. Since the drain current of the

transistor (i_2) changes with the drain voltage (v_2), a shunt resistor (r_o) is added to the output (port-2) to emulate that effect. Parasitic capacitances, being present between source/gate/drain terminals, are added to the model through C_{GD}, C_{GS}, and C_{DS}. Series inductance and resistance due to the gate/source and drain interconnects can also be added to the model to make it more accurate. Finally a series non-quasi static (NQS) resistor can be added in series with C_{GS} to capture the effect of a frequency response. NQS resistance of the channel accounts for the fact that channel charge cannot respond instantaneously to the variation of gate-source voltage. NQS resistance is a distributed effect along the channel length. Electronic carriers (e.g., electrons) at any particular point within the channel of a MOSFET see a resistive element that "points" toward the source and a capacitive element that "points" toward the gate. A direct expression has been obtained for the channel charging resistance $R_{NQS} = \frac{1}{5g_m}$ in reference [1].

Calculation of parameters in Table 1

To obtain the small signal model of a transistor, the measured two-port S-parameter data were exploited. The core hybrid-π core model of the transistor is realized by calculating impedance and admittance parameters (Z and Y matrixes) and using the following equations:

$$g_m = -\mathrm{Re}(Y_{21})$$

$$r_o = 1/\mathrm{Re}(Y_{22})$$

$$C_{DS} + C_{GD} = \mathrm{Im}(Y_{22})/(2\pi f)$$

$$C_{GS} + C_{GD} = \mathrm{Im}(Y_{11})/(2\pi f)$$

$$C_{GS} + g_m r_o C_{GD} = 1/\mathrm{Im}(Z_{11})/(2\pi f)$$

$$R_{NQS} = 1/(5g_m)$$

To fit the model to the measured data beyond the activity region of the transistor, series resistance and inductance associated with the gate, source and drain interconnects can be added and their values can be obtained by simulating gate, source and drain lines embedded in the oxide and substrate in an electromagnetic modeling and simulation software tool (such as Agilent Momentum). The component values calculated for the small signal model are listed in Table 1.

The effect of NW density on extrinsic cutoff frequency

To explore the performance limit of InAs NW parallel array FETs, extrinsic cutoff frequency is calculated as a function of NW density using the formula described in the main text. The capacitance per NW is assumed to be independent of NW density. A previously reported saturation velocity for bulk InAs, v_{sat} ~1.3×10^7 cm/s at a field of 16 kV/cm (corresponding to V_{DS} = 2.5 V and L_G = 1.5 μm) was used for this analysis.[2]

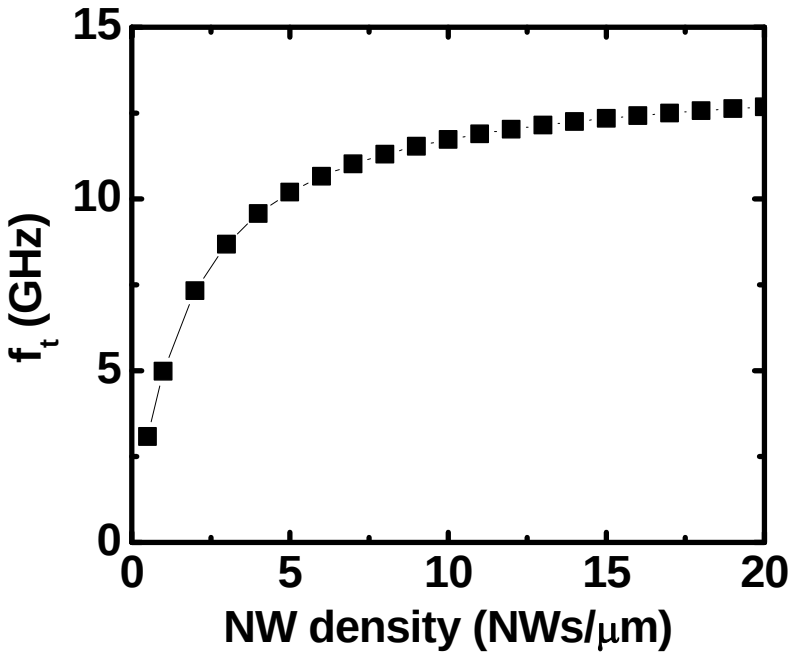

Figure S4: The calculated cutoff frequency as a function of NW density for L_g=1.5 μm. Note that the parasitic capacitances are assumed to be the same as the experimental devices (Table 1). The dominant effect of increase the NW density is to reduce the $C_{p,GS}/C_{ox}$ ratio per unit width, thereby increasing the cutoff frequency.

References

1. Baheri, M., Tsividis, Y. A small signal dc-to-high-frequency nonquasi-static model for four-terminal MOSFET valid in all regions of operation, *IEEE Trans. Electron Devices* **32**, 2383–2391 (1985).
2. Brennan, K., Hess, K. High field transport in GaAs, InP and InAs. *Solid State Electron*. **27**, 347-357 (1984).