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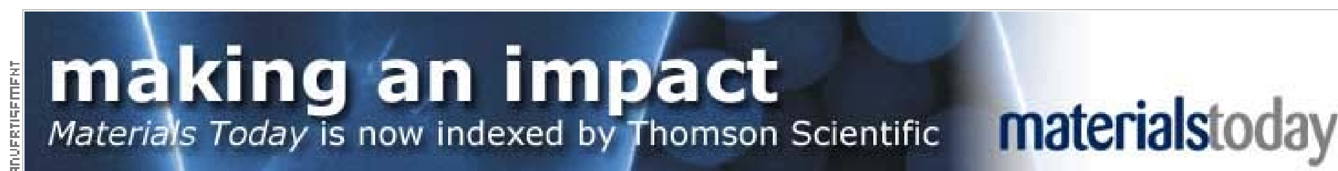

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NEWS

Surface layers allow accurate doping

Electronic materials

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A novel process for implanting dopant atoms in semiconductor materials with nanometer precision could be an enabling technology for the continued miniaturization of Si microelectronics [Ho *et al.*, *Nat. Mater.* (2007) doi:10.1038/nmat2058].

As transistors shrink in size, it becomes increasingly important to control their doping reliably, particularly for ultrashallow source and drain regions.

Ion implantation and solid source diffusion are the standard methods for implanting dopants in semiconductors, but at small scales these methods are not sufficiently precise to put dopants exactly where they are needed. In addition, ion implantation induces significant crystal damage.

Now a team of electrical engineers led by Ali Javey at the University of California, Berkeley, has developed an alternative doping method based on surface chemistry.

“We have developed a novel and generic approach for controlled nanoscale doping of semiconductors by utilizing the rich surface chemistry of crystalline materials combined with a self-limiting monolayer formation reaction,” explains Javey.

They use dopant-containing reagent molecules that form well-ordered, covalently-bonded thin films on the surface of Si. The molecules are then driven into the Si by rapidly annealing the samples at high temperature.

By controlling the heat treatment conditions, it is possible to control the depth to which the dopants penetrate.

“The process is highly generic for both planar and nonplanar (such as nanowire) structures with the dopant dose and profile being well controlled through molecular precursor design and the thermal annealing conditions,” says Javey.

The new approach addresses a critical need for a robust nanoscale doping technique that can avoid the limitations of conventional methods, claim the researchers.

“The method was demonstrated for standard Si substrates as well as Si-on-insulator and bottom-up nanowire materials, and can be readily implemented to other types of semiconductor substrate with the appropriate surface chemistry,” says Javey.

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